CMOS Analog VLSI Design
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Lecture – 12
Differential Amplifier

Good morning to all of you, we were looking last time a single ended DIFFAMP. And we were trying to show that this single ended OPAMP sorry DIFFAMP one of the great inputs of a P channel device gate of that is connected to one of the output which is V out 1 and that is makes it single ended, we also have derived from this by variety of ways that this V p remains constant. So, A C for A C that can be treated as ground. So, this is what we did last time I will just show the last equivalent circuit which are drew what we said last time that since V out 1 is an A C output, for M 4 that is the acting like an input because connected since it is connected this will act like an input and say this is equal to of this value.

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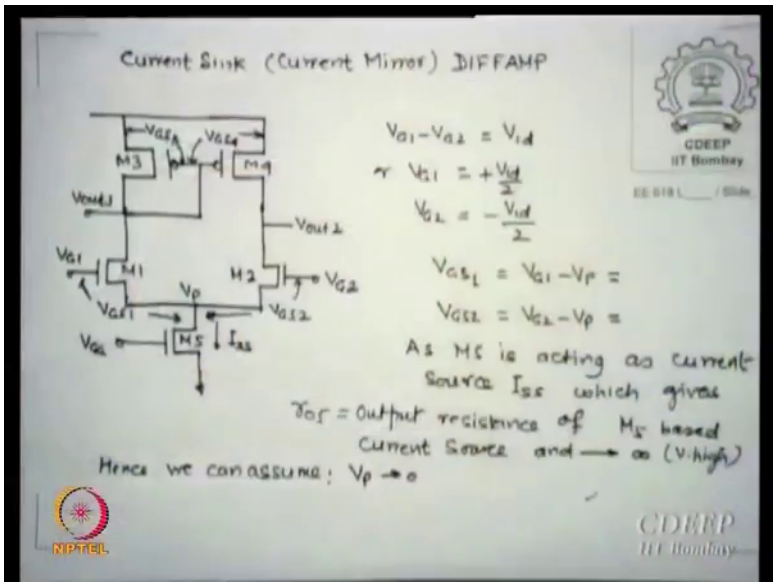

So, there is an input signal for M 4 and there is an input signal for M 2 and we say since both have the same res output resistance this R o parallel this or this parallel this for this output, at the node both transistors are give R o parallels and therefore, R o parallel R o n is always at the output resistance in independent whether you drive from here or you drive from here and if you super impose on them the output net V out can be obtained.

That is what we discussed last time and we derived finally, equivalence circuit which I just re want to do it again show you again.

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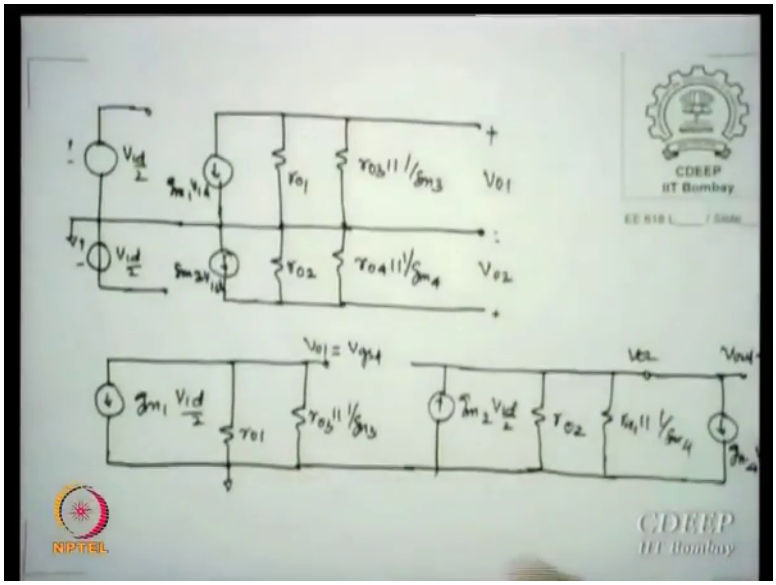

That for the M 1 M 3 side you have a g m V I d by 2 R o 1, R o 3 parallel g m 3 and this is g m 3 may dominant because it is a diode connections there and therefore, this may actually dominate over R o 3.

Ah however, they said V o 1 output is V G S 4 and that is further used here the M 2 M 4 site and we say that g m 2 V d I b y 2 R o 2, R o parallel again I said it, but this again g M 4 will be neglected because this will dominant, and then this is the next source coming from the other input at the M 4 and yeah M 4 and then if I since I use the same R o s both. So, I can directly add also plug the currents and then put across this resistance to get the output voltage which is essentially doing superposition resistance you stop this get a drop stop this get a drop add up.

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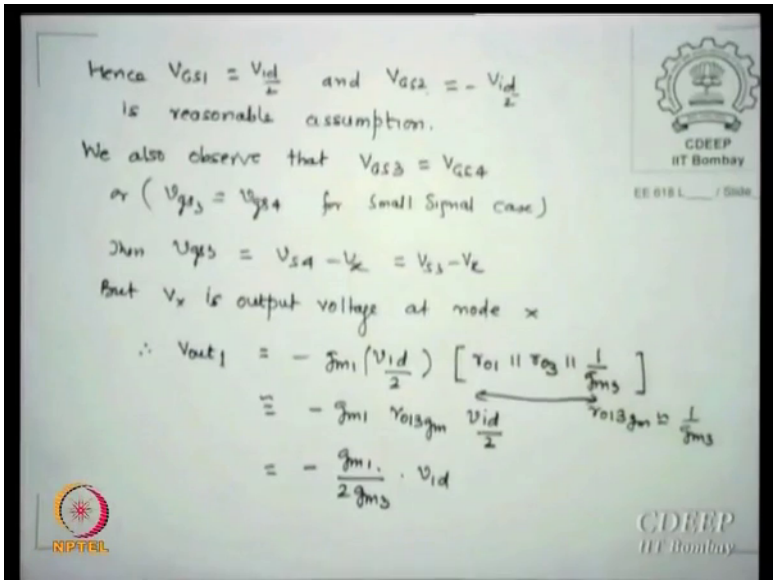

So this was what last time we did. So, let us look at the actual values actual expressions ah. Since V G S 1 is V I d by 2 and V G S 2 is minus V I d by 2 is reasonable assumption we also observed that V G S 3 is V G S 4 or V G S 3 if you are small single you look at as I say some books may show you. So, essentially if the V x is the output at node voltage which is our V out 1 then it is g m V I d, combination of R o 1 parallel R o 3 parallel g m 3 whichever will be smaller will be dominating. So, I just right now kept all three in parallel in reality whichever comes smaller among the three will take care 1 upon R plus 1 upon R 1 plus.

So, whichever is smaller his the dominant term. So, I just write now for the sake of simplicity or generality I put R o 1 3 g m as the this resistance output and then g m times this is there. So, g m 1 by and if finally, if that becomes g m 3 dependent which is the smallest among them or g m 3 is very large compared to R o 1 upon R o s. So, g m 3 will dominant. So, you get g m 1 upon 2 g m 3 times V I d. Now this fact that this is the output of the first stage that is M 2 M 1 M 3 is going to be the input for M 4 this is what is going to be utilized to get the final V o value.

So, this derivation is necessary simply because this is going to be an input to the M 4 at the other side. So, that. So, this is what we did last time. So, for may be this expression I just showed you. So, from here you can get if you see a value of this if you are holding the current constant as the I S S then you can see from here it is only a function of W by L and mu, because 3 is P channel device. So, it is essentially governed by the ratio of W by L and also mu 1 by mu p all under roots. So, we can we always know roughly you

how much is the size of the transistors and we can get the alternately what will be given to us given some final gains will have to come back and figure out what is the size of w 1 by l 1 and w 3 by l 3.

But typical design since all circuits are kept symmetric in most cases except for these ah perturbations they have one can always say g 1 will be equal to g m 2 and g m 3 will be equal to g m 4 or to say size of 3 and 4 will be same and 1 and 2 will also be same except that they may have some variation even if we feel that we are done in the same technology zone. So, that essentially is why C M R R comes finite otherwise it could have been infinite. So, this is the only correct criteria you should look that this is the size dependent gain, it only depends on the sizes of the root transistor at the designer my only interest is in getting the surface sizing because these are called mask in fabrication.

So, for each layer what should be the channel length, what should be the channel width that must which will have create at then for the gate is going to decide my performance. So, please member my output is only sizes given is circuit for specification, I must arrive at the sizes of every transistor because when I translate them into a Circuit for fabrication I will have to generate layout that layout will be depending on W by L which I have create and those will be then transferred on silicon during fab and hopefully chip may work ok.

Normally it may larger the technology node more guarantee it will wok you will see today time permitting if short channel happens what is the major worry with us there are many worries, but one of the major worries I may show you. So, is that ok so I can calculate the input to be M 4 or to say output of the first stage which is V o 1.

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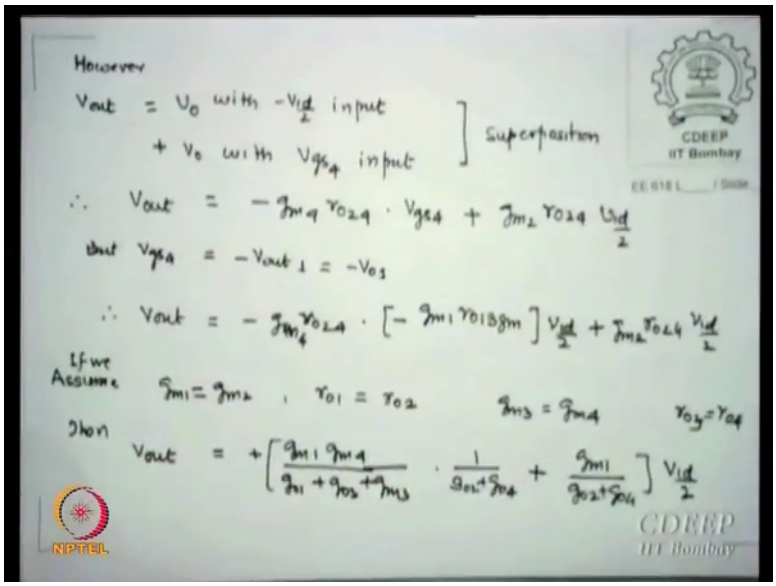

Now, looking at the output side the second part of the circuit we know V out is output voltage with minus V I d input and V o with V G S 4 at the another input. So, we just super pools them for as I just now said the method is open A Current source use the only one of them open the other one and start looking for the other currents here.

So, if I do that by substituting all this it will become V out will be g m 4 R o 2 4 where R o 2 4 is R o comb parallel combination of R o 2 and R o 4 is that clear, this is a short end writing [laugher] R o 2 4 is nothing, but parallel combination of R o 2 and R o 4 that is at the output side, what is the impedance you are seeing output impedance parallel combination of output resistance of 2 and 4. I repeat what I said if you see the circuit these are the only output resistance is arrange parallel R o due to this, R o due to this which are at this node are parallel these at R o here R o here at the output both are in parallel because this is ground for A C, this is ground for A C this is ground for A C.

So, these two resistance is r n parallel for this node is that correct for this node as I said since g m 4 is not a diode connected R o s will dominate g m 4 is almost infinite kind of thing it will it is it will not be see I have kept it there because in case tomorrow you do something else they are that term may they are and automatically it will get cancelled if it is larger or smaller corresponding in general I kept it, but I such it will not there because it is node diode can for this it is g m 3 is appearing for this there is no diode connection is that is a normal transistor whose output resistance is just the R o.

Semi is true for true semi is true for true unless there is a diode connection the g m will not dominate is that correct, we are done that case for a diode connecting load and that is what we proved that time. So, the idea as substitute all these values once again V G S 4 is V out 1 minus this and by substituting finally, I get V out is equal to g m 1 g m 4, I am assuming right now g m 1 is g m 2 g m 3 is g m 4 all p channels are identical or n channels are identical that means, what are identical, the w by alpha is identical the thresholds are identical is that correct the identical what mean the mu c o x is constant mu 1 c o x same for both V T are same for both and W by L s are same.

This is essentially means identical, as I said I repeatedly saying perturbations will take care only in the case of C M R R, because that is hurting a plan alright which was infinite value otherwise you can always assume them for equivalence of this say if I substitute all this you can see of course, this is not exactly what is given in the book, but you can write down V out is g m 1 g m 4 upon g o 1 plus g o 3 plus g m 3 many a times instead of using R o in parallel it is much easier for us if we use g o because then you can directly add is that correct many a times for the circuit people you should realize that if there in parallel R is the parallel it is much easier to add g s rather than putting 1 upon R plus 1 upon R plus 1 upon R.

So, I will normally certainly covert a times. So, please do not feel anything wrong this is just the way of solving simplicity and using simple solutions. So, g m 1 by g m 2 upon g o 1 plus g o 3 plus g n 3 plus 1 upon g o 2 g o 4 in plus the second term which is for the V I d by 2 is g m 1 by g o 2 plus g o 4 into V I d by 2. So, once I get the relationship V out and V I d by 2, I can always calculate V out by V I d which is essentially the gain of this single ended differential amplifier in difference mode is that correct this is not the common mode gain it is difference mode gain A V D M this is essentially A V D M case.

So please write down if you wish because I not sure whether this is given in (Refer Time:12:42) because I did not cheat may be there at least they do not use g's the way I use of course, I also when I see that book then I see oh there using different term, but I feel it is much easier instead of R o writing write g's is which is easy to add of course, this method or writing g's have come from you know my other colleague mister Sharma who has very fond of conductance rather than resistance, things which can conduct is what all electrical engineering is about if it is (Refer Time:13:18) then it is not good na. So, I think I also once I have will take this q and I use g's because I see and almost all is

analysis he rarely use r's he always write given of g or g. So, I figured out that I should also follow after so many years of my friendship 35 years.

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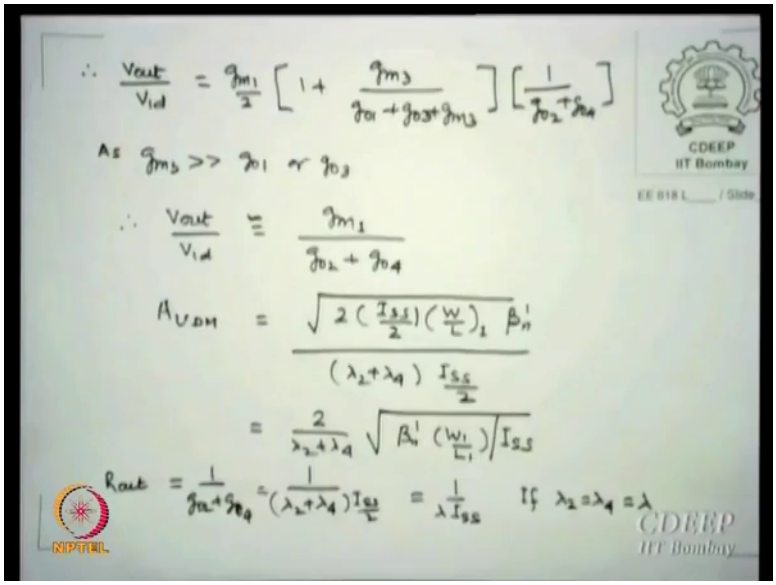

So, I am just make a fun of it nothing very serious is that. So, I divide this V I 2 by V I d and then I get this expressions and then I start putting g m 3 is much larger then g o 1 or g o 3 and therefore, I neglect those terms. So, I got V out by V I d which is g m 1 upon g o 2 plus g o 4 and if I sub is that clear, if I neglect these two terms this becomes 1, g m 3 by g m 3 this becomes 2 this 2 cancels. So, g m 1 upon g o 2 plus g o 4 is essentially your difference gain maybe I should write A V D M.

So, which is what is g m 1 why I wrote this expression is relevant for us because from a designers point of you, let us say what is g m 1 g m 1 substituted at 2 times current in the each arm is I S S by 2 W by L, 1 into beta and dash divided by lambda 2 plus lambda 4 into I S S by 2, lambda 2 and lambda 4 are not same why 2 is n channel device, 4 is the p channel device. So, lambda is not identical for n channel of course, you can make this in process forcibily, but in normal circumstances lambda 2 will not be equal to lambda 4 they may not differ drastically, but since the mobilities in P channels are lower than n channels normally resistances are higher in P channels once I have think of it.

So, it may be better to use P channel as loads is that correct because it will give larger resistance per see now issue here is lambda 2 by lambda 4 I S S by 2 I took it up. So, it is beta and l W by L one by I S S and what is the output resistance I said you do not have to

put a source and measure because obviously visible in calculations. So, it is one upon g o 2 plus g o 4 maybe I should write g o 4 which is like this and case which is what I say normally may not be, but in case you make lambda 2 equal to lambda 4 lambda this will become lambda I say which is same as what we have derived earlier lambda point lambda I D S. So, once we get output resistance we get the gain the two major specification for DIFFAMP have been found out and they are functions of what the bias current and the W by L's is that correct the bias current and the W by L's.

So, you have either design parameter with you they are only two parameters governing the gain one is the size of the M 1 M 2 and which is same, which is which is essentially governed is governing g m 1 and the bias current I S S which is also controllable externally is that correct either by the transistor which I will put for source I S S, either the size of that transistor or the bias of that transistor or a mirror it from other some source which actually will 4 exactly the current which I wish I will show you mirror 1 once later when I calculate. So, essentially I am trying to tell you that the designer I now have related the ok if you want so much gains 10 to power 4, 10 to power whatever number you say.

Also in many cases in books which you should know this the gains are always specify voltage gains will be specify specified as voltage by voltage now it does not mean because it essentially is trying to tell that it is both the dimensions are same, but it is written V by V by because it is trying to show it is a voltage amplifier is that correct. So, you also should get (Refer Time:17:52) this because there are four kinds of amplifiers which we can use we all of you have gone through this earlier output current input voltage output voltage input current input voltage input currents and output input voltage input output voltage.

So, four process is called conduct trans, conductance trans resistance current amplifier voltage amplifier all four is that clear. So, this is essentially what we are doing and therefore, we say that this V by V only tells input is voltage and output is also voltage. So, I mean I did not write, but I just thought you should know many books or many places the data sheets give V by V. So, what is V by V is time to tell you it is the voltage gain dependent terms which I have been specified sometime then may V by I, I by V, I by I. So, these are the methods of representing the amplifier outputs or gains.

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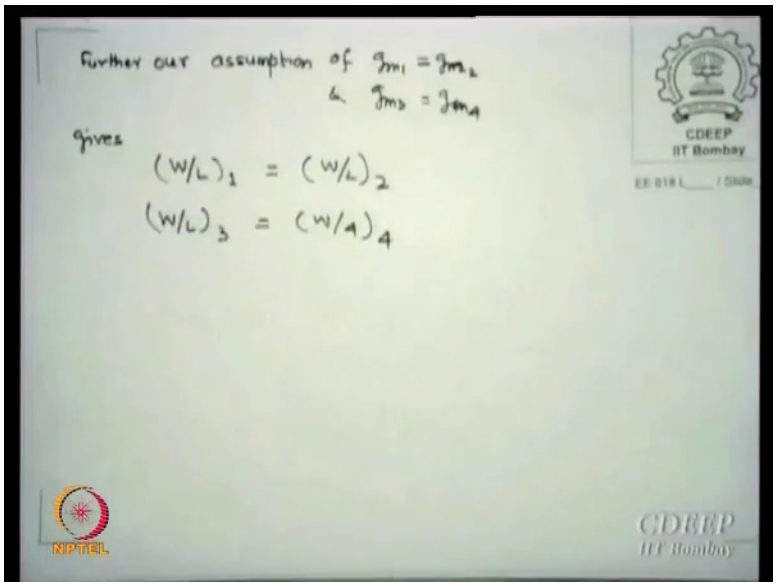

If we further make an assumption ah which we will we know that the P channel devices have same and n channel devices are also identical to each other which they will be in most cases we are now saying V n W by L 1 is equal to W by L 2 and W by L 3 is equal to W by L 4.

This is not a necessity, but it is much easier to lay out much easier to derive if these are available to you, but that is not a necessity expression does not require anything equivalence of that if they are different we can calculate with all different R o different g m. So, what I mean there is nothing very seriously problem problemistic for getting all difference, but in normal case DIFFAMP design on an integrated circuit will give you this g m 1 very much same as g m 2 and g m 3 is very much same as g m 4 in which case one of these sizes if you figure out 1 and 3 out 2 and 4 we will be able to why I am telling you this word 2 and 4 is related to output resistance. So, someway if I am giving you a I D S and actually giving you some way W by L's indirectly 2 n 4, but if a note 2 n 4 I know I will 1 and 3 is well ok.

So, this is the design issue from what data is given to you and what specs are given to you and what is expected out of you then you can figure out which term is, I will show it today at the end some few expressions when I design think something. So, is that ok but I repeat this is not a necessity this is just for the heck of it and in general I see people believe that it sold be symmetric as much as possible the try, but that does not mean it is

a necessity as for as the gain or any of the parts are concerned there is a problem why it is normally kept which I did not say. So, for is there is an issue of stability of an amplifier if they are not equal the capacitances will not be equal and there is a possibility of two stage amplifier oscillating having done this small signal analysis all through let us look at little bit carefully other 2 or 3 parameters which are essentially large signal parameters.

What does that large signal means if the input voltage is not only restricted to be V I d by 2 n minus V I d by 2 if they exceed what would happen, one of the major worry of any amplifier is and that question was the ask and I think most of you must have written correctly that we are looking for large linearity that is V o V n relation should have stand unity or whatever number for a larger input voltage swing is that correct if that happens when we say we have input swing can be larger. So, larger inputs can be amplified that is called larger large linearities we also want as I said we do not want linear mode because transistor within linear mode is in non saturation. So, square lot terms will not be possible and it will give lot of distortions. So, that question which was asked is large linearity, but device is still remain in saturation in linear mode means it is a non saturation, we already show in V o V I Characteristics if V n is outside the slow part the V o is not even some time governed by V n it may become constant that is exactly what the saturation part appears there.

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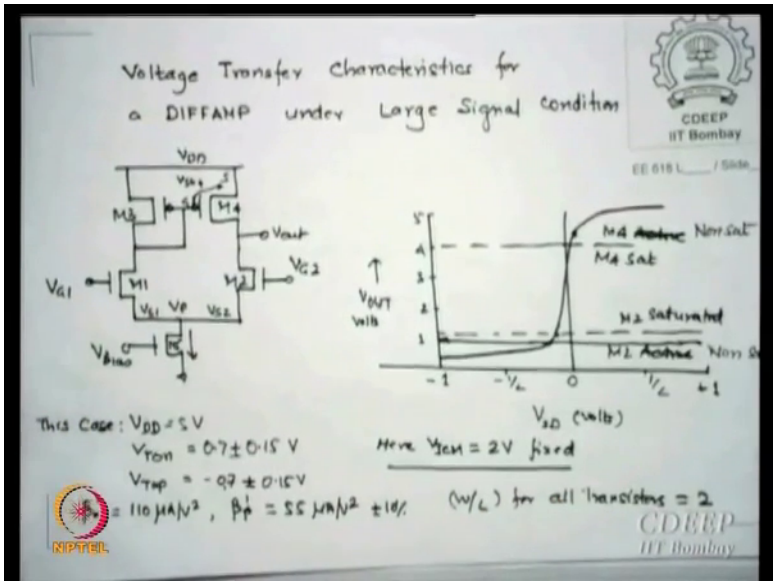

So, this issue we look into this again we want to see the limits ok. So, these are called limits or ranges, 2 ranges of interest to me one is at the input the other is at the output the output voltage maximum to minimum what I can get is called the output swing. So, one of the spec of a difference amplifier for that matter OPAMP is the output swing how much output maximum you can you can achieve from a given circuit which you design the other of course, is how much maximum to minimum input I can vary which will still give me gain is that correct. So, what does that mean the device still remains in saturation for those inputs beyond that they may not? So, I will figure out where they turn over from non saturation and then say this is the limit for me now in some cases that limit may still had distortion because the linearity may not be as good, but does not matter you may actually tune of the restorations or you may tolerate some of those distortions ok.

Which distortion is most important third harmonic distortion think of it why T H D is most dominant distortion problem, then the second harmonic which is most people first derive, but it is the third harmonic which essentially is the trouble creator. So, linearity is we such that the third harmonic distortion is small. So, we will see that when the gain comes. So, here an amplifier against same thing which I showed, now let us say case I just tell you how the data Can be given to you there is this is not being used specifically here, but just to show you for the let us say I have 5 volt supply this 5 volt has supply has come from .35 micron process ok, we use to use 5 micron. So, all the books whenever you see borrowing the let us once which may probably have 1.2 volt supply otherwise this is the data given by everyone. So, I thought if it all someday you are going to read the book you should have the this ok.

The V D D is 5 volt V T O of n channel O means stand for without substitute bias typically it will be point seen volt let us say plus minus this is the tolerance you will get actually. Similarly V T O P will be assuming right now we are using the same in many technology is allow that minus .7 plus minus .15 and for this 3.2 micron, .35 micron technology you can use beta and dash which is mu 1 c o x this data of course, I will provide you whichever technology file I will use the data will be coming from that technology file, but as far as we are right now concerned it is the numbers are only numbers we are not saying that this is specific to a technology may say this is the data are this is the spec, in realties spice will not allow you random numbers for a given node

they will specify each of them because there oxide thickness are known their capacitance are known they know everyone they are ok.

So, they will specify automatically these values which you do not have to even worry, but if you want to read you they will show you also what are the values they have being using in this. So, typically beta n dash is used hundred 10 micro amp per volt square, please take it units should be correct in every sense because this is something I do not like people do not putting any units sometimes I also forget, but if I do I have right because I am a teacher you are a student you have no rights. So, this is micro amps per volt square beta p dash is chosen 55 what is that means, half of that means, the ratio of mobility is chosen as 2 mu 1 by mu p is 2 if they specify something else obviously, this numbers will also change there is another number which what you are going to use is called input common mode voltage which is defined as V I C M and typically for this apply.

We will come back this v I this is what one of the thing which you want to calculate right now the evaluate, but right now assume it for this is roughly 2 volts which is fixed W by L for all transistors chosen here are 2 now reason let us that is that. So, if I use this I mean this is a data probably I mean use in my problems. So, that is why I give you data is not that this data is really relevant data or something, this is typically for .35 micron most people believe this is values in reality the table from spice will be made available to you whatever specs they get it they will specify. So, those values are only arbitrary from my side, but they will give a exact values.

Many books actually gives you data files if you see a book they will for given technology they will give tables or all parameters p ox everything what are variations everything will specify all C G S C G D every capacity everything there is specified for you, of course per micron there is specified because width will change the net capacitance, but they will specify all data file data file will gave every detail of that. So, please if you have already done n g's spice or whatever spice see a technology file then you will see all this things are provided by them, the there are of course, in spectral or (Refer Time:28:39) also. So, much easily, but there is a model card in the spice which you can write yourself.

So, it is not that what their default values are there you have to only work with it you can change your model parameters and still work on it if you have use model card of your own. So, do not come and say [FL] you can always change your spec of your choice by putting another model card there I am not sure with n g's spice or spice 2 g 3.3 has that, but just figure it out the modern car allows you to specify all mu's t o x everything of your choice. So, please take it these are some issues of interest this figure is very important I think this is what we are going to explain once again, if I plot the V out versus input V I d as figure it out from here this is my V I d by 2 somewhere if you look at it very even up to minus V I d point there is some slope beyond that it becomes almost constant is that clear. So, we say what should be up to this or up to this what should be the range up to which device can be treated in saturation.

So, here is the figure we which we have plot this need not be exact numbers, but just show you if I see from V I d minus somewhere close to V out of 1 volt for example, for V T of these values around point 2 V I d or something it is starts climbing at this value device enters saturation, below that devices in non saturation now linear mode this active word is used by analogue people very much in a wrong fashion because active essentially saturated mode in M O S transistors because that is the time where device as amplifier is active. So, I think this active word is not very true, but you should may be you should write non saturated because that may create some bias.

So, as you go beyond some 0 towards plus V I d somewhere close to this value of .2 or something V I d, I figure it out at around 4 volt of output lease device enters non saturation from where this values again V G S minus V T exceeds V I d V D S as longs as (Refer Time: 31:40).

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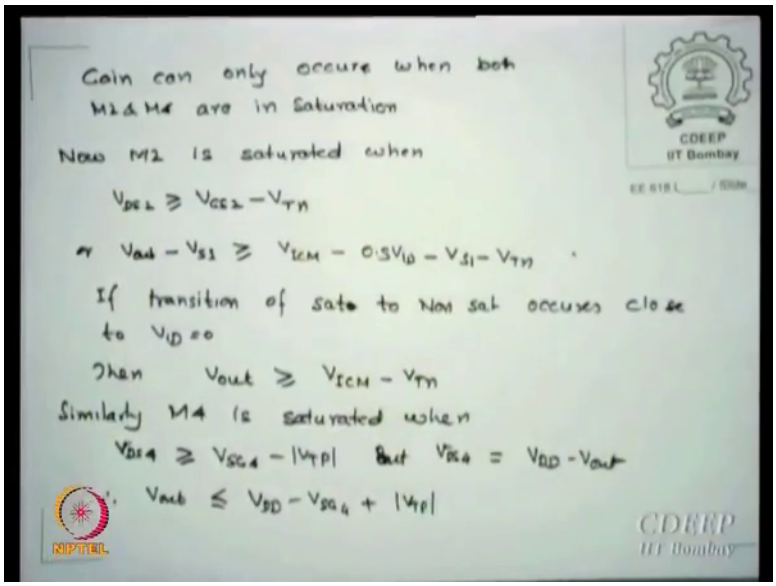

So, we have now said gain can only occur when both M 2 and M 4 are in saturation, at the output M 2 and M 4 are the two transistors. So, if they are not in saturation these R o parallel this will not be there g m's will not be there and therefore, by the way you calculate g m linear and it figure it out why I keep saying it is much lower there are you say why [FL], but that is much smaller than g m's add and therefore, this is the gain.

So, we say now we start looking into the please keep your figure up there I will keep figure for myself here we would say if V D S further M 2 transistor to be in saturation V D S 2 which is the gain to source voltage of the transistor should be larger than or equal to V G S 2 minus V T N is that V G S 2 minus V T N this is straight forward transistor theory, however if you look at the V D S 2 it is nothing, but this voltage minus V S call it this you call V S 2 those are equal, but these are voltage at the source which are grounded, but let us put them there. So, I say then it is V out minus V S 1 is my V D S 2 which should be greater than now this is very interesting.

The V G this V G 2 part is essentially the maximum input available and from where saturation is guarantee the V I d by 2.

So, that is the swing available for you V I C M if the end of that and V I d by 2 are going to put. So, what is the range which the because we are finding bound. So, what is the maximum available to you is this much. So, if I do that analysis. So, I will say V I C M

minus is actually V G 1 V G 2 minus V S 1 this is V G S 2 minus V T N, but have you yes.

Student: (Refer Time: 34:02).

What is V I C M it is the input common mode range maximum and minimum range. So, if you are away from V I d by 2 up to which transistor remain saturation the test we are giving, but it was still test require 1 V I d by 2 turn it on into have a signal. So, the difference available for mu 2 see whether device still in saturation is V I C M given to you minus V I d by 2.

Since V I d by 2 is this, but essentially the transition occurs very close to 0 itself. So, that term can still be neglected by you, but just to say that it is there I kept it normally books do not put that term they says V I d only V I C M, but I say in case you feel it the reason why they are doing it because the transition if you see is occurring very close to 0 is that clear and that is why they normally neglect that V I d 2 term, but if case you want to keep you can keep, but that is smaller than other values. So, it will automatically we numerically neglected physically may be exit is that now I always try to say people that why people are saying something in the books or otherwise.

So, explanation there is nothing very great I am telling. So, I have wrote that if the transition sat to non sat occurs very close to the 0 V I d value then we can neglect this term anyway. So, we say essentially what we are saying the V out should be greater than V I C M minus V T N, now similarly I can calculate the limit for this was for M 2 is that correct this was for M 2 now I calculate when M 4 will remaining saturation. So, what is the criteria for M 4 then that the V D S 4 should be larger than V G S 4 minus V T P, V T P is the p channel threshold. So, I say and this has to be subtracted by numerically. So, I will put a mod otherwise it is say it may get added you know minus of minus may get added. So, I just put it M 1.

So, if that is so it is V S G 4 minus V T P, but let us look at the game again [FL] [FL] [FL] actually ok. Now, we can see from here V D S 4 this value is how much V D D minus V out. So, as substitute V D S 4 is V D D minus V out it should be less then now because this is minus is that correct change the equality. So, V out source is for a p channel source is power supplying why otherwise holes cannot come down. So, if I write this then V out should be less than equal to V D D minus V S G 4 minus plus V T P, I flip

the in equality if I get this how many V out I got it now first I got it V out from the M 2 side the other I am now getting from M 4 side. Which one you feel will be larger please remember from the vi input side is coming from the ground side look at it this is what input to ground, but this is what output to the ground. So, it goes to ground, but V D D ground is A C ground, but it is V D D. So, always the output side has larger ah value from the V D D side and smaller value from input side or lower side and therefore, M 2 decides the minimum value of the swing and M 4 decides the maximum value of outputs. So, if I do this expressions which you have you written down.

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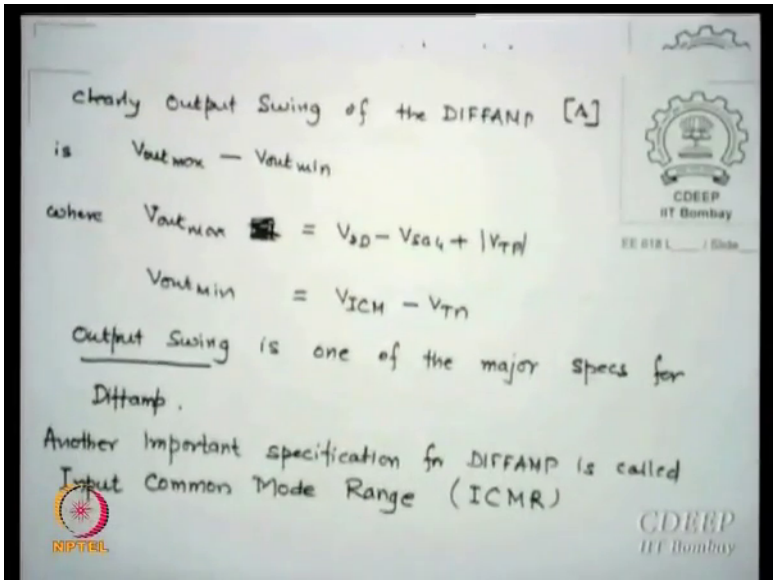

If I do that clearly the output swing of a DIFFAMP is V out max minus V out min which is V out max is V D D minus V S G 4 plus V T P, V out min is equal to V I C M minus V T N and therefore, please take that this is what is the criteria I have A Come from that M 2 M 4 should remain in saturation. So, from there I derived these 2 values and say difference between the image the maximum swing output can have this has some the amplification word was difficult. So, it has an influence on the next deV I Ce input characteristics what voltage it receives ok.

Student: So, in this analysis V in V S G 4 has to be evaluated.

Yeah we will we are not I am not said we cannot evaluate V S G 4 is known to us V out 1.

Student: (Refer Time: 39:20).

[FL] you are right I am not denying, but why I have left this because some what will be given to me and what will be right now I do not know. So, I am keeping expressions as they are, when I evaluate I will figure out what is given to me and I will come back to the evaluate this value from whichever either they may give me this or they may give me something else. So, I will arrive at this value from please take it what is V G S essentially can be written as in terms of I D S is equal to V T plus under root of this I terms you can always right. So, whichever may I am provided V G S I will be able to calculate anyway has the occurs the right now I do not want to say what is that.

You are perfectly justify in asking, but I have did not evaluate earlier because I will see which value evaluate is that correct if I know that is this current I will say I know how much is because this current will be output current is decided by something which will see now. So, that also may decide V S G 4.

Student: I am calculating this swing we are not concentrating (Refer Time: 40:34).

Gain is essentially is very small because the end we are looking at the end of the gains linearity just going out of linearity. So, they are gains are anyway very small is that clear if you are in this range then only is you D V 0 by D N is very large, but if you are here you are anyway very small gains. So, we did not consider assuming unit gains which is not true, but to some extent it is that (Refer Rime: 41:00), but these are bounds we are not saying these are the value these are the bounds up to which this swing can be of please remember I have put larger or less than I never said equal to equal is the better possibility, but may not they should actually satisfy the inequality is that correct. So, one swing one parameter offer one specification of DIFFAMP we are seen gain, other we have seen the output resistance third we have seen swing and the forth we will now see which is what is called a input that V I C M I used. So, now, I will derive that I C M R another important specification of a DIFFAMP is called input common mode range .Is that. So, should we is go ahead A was the output swing. So, B is named as input common mode range.

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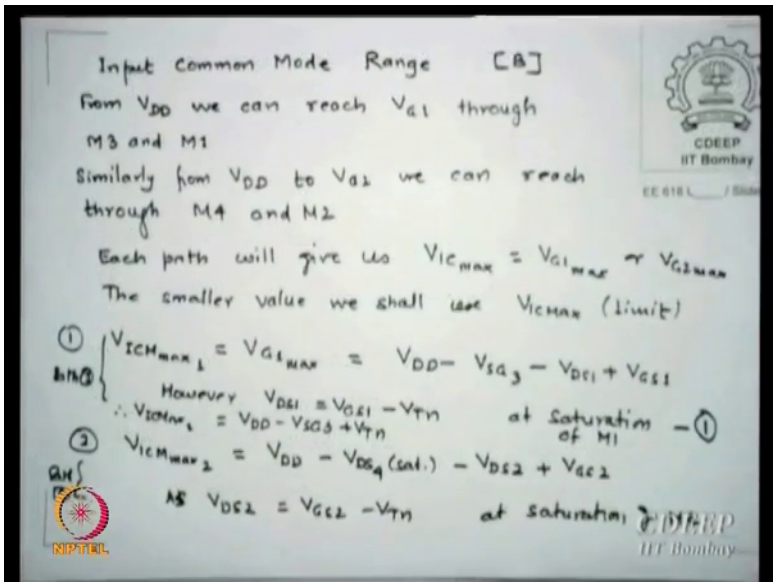

So, what is the input variations you can have from V D D to V G 1 is one possibility and from V G 1 to V S S or ground is the other possibility that is how input will vary is that correct please take it input will vary from source to the V G, V P to this or from V G to V D D as we did for output same way we now do it for input side is that raj from V D D we can reach V G 1 through M 3 and M 1 please look at it the figure again if I have to reach here I can say drop across this, drop across this and subtract here or as whatever signs properly I get.

So, one path is like this which is the other path other is to come here and you directly write from here if you do this. So, there are possibility of either this, but for if you reach this value you can also reach from here to hear. So, V G 1 can be attained through this way or through this way or through this will be which is actually these two are identity because this V D S will be (Refer Time:43:34) to V G D. So, either I comes from here or I come from here I have the excess to reach V G 1 and same is true for V G D . So, if this is what I am saying I have two paths. So, I said same way I said there is similar there will be two paths for V G 2 we can reach through M 4 and M 2 will that correct it is identical [FL].

Each path will give us V I C max and we will figure out which one is lesser that will be my range, because lesser why I should chose because I am finding the limit up to which device will remain in saturation is that correct. So, I will figure out 2 V I C m's and then

I will say which one is smaller then I will use. So, here are the two way of doing it path one which is V I C maximum 1 is V G 1 max, please remember what is the input common mode value which is the input maximum value available to you which allows device to remain in saturation. So, it is V G 1 max how much is V G 1 from the figure this value minus this value. So, you reach here that means you reach here minus this value minus this value.

So, not minus why we are claiming up. So, it is minus that is plus. So, V D D minus V S G 3 minus V D S 1 plus V G 1 is V G G 1 max however at this edge of saturation what is V D S 1 when this translation and this V D S minus V T of V G S minus V T is equal to V D S that is the edge the least value of that. So, I write V D S one is V G S one minus V T N at the age of saturation. So, I write V I C max 1 is V D D minus V S G and I replace this V D S 1 by this substitute here. So, I get this V D D minus V S G by 3 plus V T N is the value which I am going to get what is that clear to you what did I say I have substituted V D S 1 in terms of V G S 1 minus V T and then that V G S 1 canceled and only this minus this cancels and V T became positive. So, in terms so it is V I C maximum one is V D D minus V S G 3 plus V T A the other path which is path 2 which is V D D minus V D S 4 this minus this drop.

So, reach this output minus V D S please look at it, what is the other path I come here V D S 4 V D D minus V D S 4 minus V D S 2 once I have reach here I just add V G S 2 to come here or V G S 1 to come to the other side is that correct. So, if that is. So, I have solved now the other one V I C maximum 2 is V D D minus V D S 4 saturation minus V D S 2 plus V G S 2 is V I C max, but what is V D S 2 at the age of saturation V G S 2 minus V T N. So, substitute this here is that correct at the edge of saturation which is the liming point for then saturation will go. So, that is the value I want max I am looking at. So, the edge I am looking. So, we are substitute this V D S 2 here magnitude wise you are right substract V S D by 2, but it does not matter as for as the p channel device everything is in opposite sense. So, it does not matter ok.

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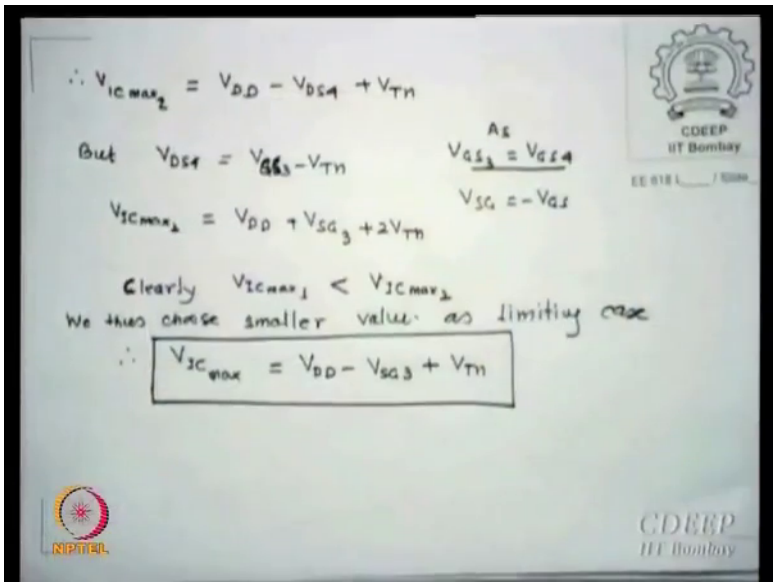

See if I substitute now this I get V I C maximum 2 is V D D minus V D S 4 plus V D N V T N and, but V D S 4 is V G S 4 minus V T N, but V G S 4 is V G S 3 we have connected them. So, I write V D S 4 is V G S 3 minus V T N and substitute that again here oh yeah sorry no, but V T P is equal to V T N. So, it does not matter [FL]. So, V I C maximum is V D D plus V I G 3 plus 2 V T N is the value of V I C maximum 2, which one is smaller among the two expressions I derived one is what was the value I have derived first one [FL] V I C maximum is V D D minus V S G 3 plus V T N and this other one is V D D plus V S G by 3. So, what I am trying to say V I C max 1 is smaller than V I C max 2. So, what is the V I C max we should use is lower one which is V D D minus V S G 3 plus V T N is the value we are using for V I C maximum.

Input common mode range which will allow the transistors to get the output both sides and still remain in saturation is this value one of this value which is the other value I will going to get from the ground side or from the source side is that method. So, please take it in all analysis of amplifier the max value come from V D D side and min value come from ground side or V S S side. So, let us derive the V I C minimum part. So, what is the path of V I C minimum for either transistor this drop please look at it from ground or V S S this drop plus this is that clear this plus, this plus this. So, that is the only V I C available to e to reach to the V G 1 or V G 2 ok.

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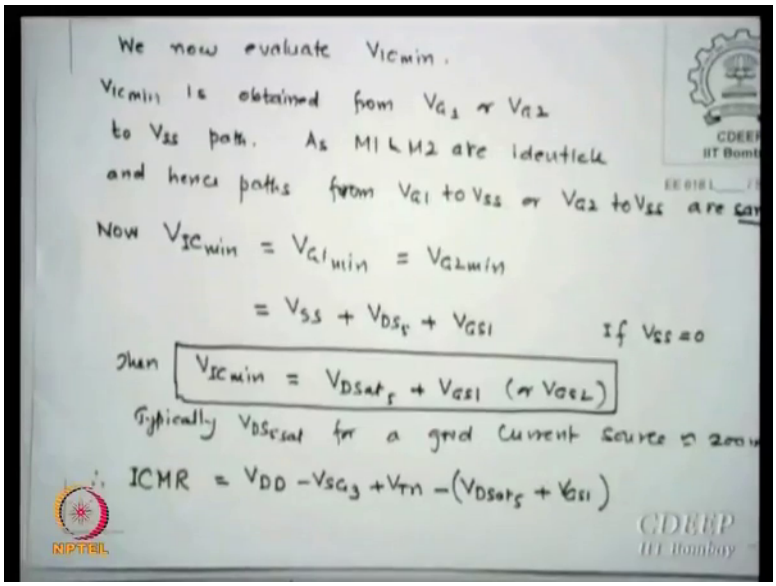

So, if I will use this and we do not have to be since we have V I C minimum is V G 1 or V G 2 to V S S path we derived V I C minimum is V G minimum or V G 2 minimum which is V S S plus V D S 5 plus V G 1 or V G 2 because we are assuming V S S 2 be 0 anyway drop at the p point is0. So, I get this value which is V D S at 5 plus if V S S is taken 0 then V D S at 5 plus V G S 1 or V G S 2 whichever very typically V D S at please take it, V G S minus V T further data given to you is typically the value which you get at the edge is around 200 millivolts, but this is the gain what the point 7 volt supply. So, one should not use the .7 volt V D S if you have another technology this 200 millivolt is not true, this 200 millivolts I just want to show you order in which this numbers appear. So, V D S that is typically for 200 millivolt for the source which is used current source.

So, we now define input common mode range as V I C max minus V I C min and this is the value which please remember this normally will be specified by us how much is the drop across the current source that is V D S 5 is normally specifiable these will be given to use technology parameters this will have to calculate from currents or voltages through which your you come this is given to you. So, everything is given to you. So, you know I C M R, if I give you I C M R one of the parameters which is missing can be in valid typically V D D V T and this will not be only thing you will be able to evaluate is V S G 3 or equal to V S G 4 if I have specified you input common mode range is that correct this is the range.

So, I am essentially specifying to great extent this value is that clear [FL]. So, we can always get V S G 3 is that point clear this is the trick in designs which spec is given and which you have to evaluate, please remember this V S S is 0 is not a normal case in most OPAMP's you will always they have dual drain. So, you will have V D D 2.5 and V S S minus 2.5 swing still will may be 5, why there is a necessity of putting a minus apply instead of why not single supply 0 to 5 or 0 to 3.3, why people in analogue is specific always want to run dual ranges there are many other four reasons, but the major reason why we did was reduced noise considerations ok is that expression. So, I C M R is V D D minus V S G 3 plus V T N minus V D S at 5 plus V G S 1. So, let us do the next parameter of my interest I have done. So, many I am now giving one by one all this spec for a given DIFFAMP. And whatever I am giving from DIFFAMP I have almost true for everyone of them for OPAMP with q more with OPAMP.

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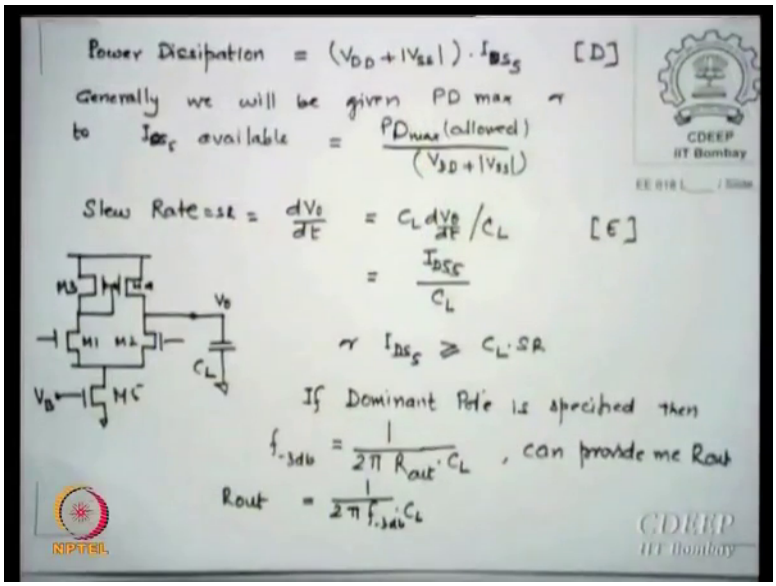

The next important parameter for me is this power dissipation of this also will be specified from where this gets specified why should I specify power dissipation we know from where this power is actually getting limited to can say power supply yeah that is a great issue, but there is now the only within temperature . So, essentially which is decided by the change in temperature of the device and we know around 150 plus the junction loses is junction property and because of that no junction will remain as junction versus the leakage current will go. So, high it will be higher than the we what we call diffusion current will be dominated by diff currents. So, we want to wide that situation.

So what do we do then how do I decide that I say how much is this sink heat sink I am providing for the chip that is called the thermal resistance available for to the ambient from the source of heat. So, I solve a thermal conductivity equation continuity equation and figure out for given thermal time constraints that is the conductivity of the materials I am going to have in series of them and I have figure out how much heat I can dissipate. So, that I mean temperature does not exceed this delta t by delta p is called thermal resistance delta t by delta p is called thermal resistance. So, I must know that for a given temperature raised with the available day thermal resistance of the path I know how much is delta p positive that is possible.

So, power is limited by the heat saying and not anything else is that correct if can remove the heat you can guess from this your laptops or now a days i-PADs or whatever android based any other android system, they have been very low in power for variety of reasons, but where not only have power supply is low, but they are the method they have used the materials much better heat sinking materials whereas, then the desktop system huge fans are put because a simply is at least [FL] power supply [FL] do you know the mother board is fixed with the S M P S used, if your S M P S goes your mother board also has to be changed because the voltage we are using so high for speed let me do not bother heat generation, but then heat has to be removed that is the reason why power is essentially decided by the thermal gradients you create of course, in real chip there are another problem if thermal source away from the actual ground this and they are huge transistors at difference sources they themselves conduct across and then there is a huge thermal pattern comes.

So, all device property that different at different point of time and one does not know what characteristic you will go. So, this called thermal simulations. So, one of the major simulation we do first in real chip design is to do thermally simulation where the pattern thermal patterns are microprocessor may [FL]. So, power dissipation is the power supply multiply by these source current which is I D S 5 in our case generally we will be given P D max or we may say given P D max divided by the supply for the technology node we will decide maximum current available to you is that correct what is the source maximum current given to you is decided by the power dissipation for you [FL].

Please remember this is for one arm. In fact, if they have 5 farms we have to divide by 5 that is power in each arm we have to get and then find the I D S 5, because that any time

gradient should not be created. So, this is one term which is limiting currents please remember if I change the current what change as everything changes. So, for whatever terms I derive everything is related to I D S, I S S which means any change their will affect all other parameters. So, we must go that the set 4 the fifth or sixth whatever number I have made the next parameter of interest to me is the slew rate now if you see a simple circuit shown here this DIFFAMP is driving a load capacitance of C L. So, one can say slew rate is defined as how fast the output raises to be maximum or change from 0 higher to lower or lower to higher.

So, essentially it is defined as d V 0 by d t rate if I multiplied by capacitance and divide by capacitance I get C L d V 0 by d t by cl which is same as the rate, but what is C L d V 0 by d t is the capacitive current and the maximum current available to you is I D S 5 which shows you why that is the maximum current in the capacitance which share you the right now which is not so visible but. So, I D S 5 by C L is the slew rate. So, what does not I am going to get it if I am given a specified slew rate. So, many micro volt per micro second 10 20 100 whatever number as specify as soon as I specify slew rate to you and in the load is given to you I am also now giving you limit for I D S 5. So,[FL] [FL].

So, which one I should use optimal which satisfy most of them is that correct not all of them exactly, but close to that if you can get. So, I D S 5 is at design parameter and that is why say normally I have prefer g m by I D S design because I D S is now your design parameter is that clear is that point clear, I D S design of a that is source current decides how much is everything going to be and therefore, you must actually look for this value from variety of specification given to you [FL] if you look at the frequency response the bandwidth part let us say for this all other capacitance are not where irrelevant which may not be true and this is the dominant pole. So, the 3 d b value which is my bandwidth this 2 pi R out C L. So, R out is this one upon 2 pi 3 d b 1 upon lambda I what is lambda what is the R 1 upon lambda I [FL].

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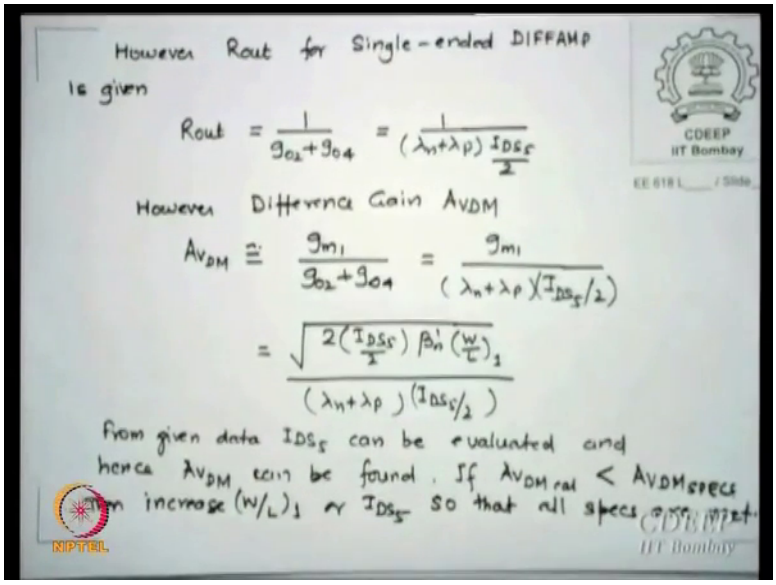

So, it is one upon g o 2 plus g o 4 or lambda p I D S 5 by 2 how are the difference gain if I now substitute g m this like this which I have derived now I can see from here I D S 5 can be evaluated from power supply requirements that is power requirement, slew rate requirement I may choose one I D S 5 and then start looking for the gains at power dissipation the slew rates is that clear, once I fix this then I will compare with my specs given then I will tweak change this that is what and that is why I am keep saying no where are the gains will be specified as 1000 greater then equal to 1000. So, you have play enough slew rate will be also said not less than so many micro volt per micro second not less than is that clear same way power dissipation maximum allowed is this.

It does not mean you cannot have lower power dissipation it does not say gain should not be more than what you specified it says it is the bound which I am giving the designer should chose values which should therefore, all specs as much as possible is that clear to you. So, I D S 5 being my design parameter let us see if you fix something and your gain does not come what is being specified. So, increase W by 1, L 1 is 1 possibility or increase the I D S 5 itself, if you increase W by L 1 indirectly are also increasing I D S 1 which is connected to g m 1. So, please verify which term game by I D S I have to you na please take it g m by I D S I am looking into this will decide my g m part I D S will be decided by the other thing. So, I am I design parameter therefore is g m by I D S not g m not I D S though I can independently look for them, but the ratio should be use by me as my design specification is that clear to you.

G m is W by L 1 related. So, [FL], but I D S. So, that you get the gain you get the slew rate you get the power dissipation you get every spec which you want to attain to this that is the minimum value which is allow.

Student: greater than (Refer Time: 64:36).

They ha. So, he is wrong it should be higher than that anything which is higher slew rate I am not worried about this is the minimum value I must attain to think of it slew rate is always specified not less than. So, much the minimum value of slew rate is 40 millivolt microvolt per microsecond. So, is that point clear as a designers what is the criteria and saying g m and I D S ratio is I am adjusting is that clear to you and that decides me almost all specifications. So, either designer I keep watching what parameter I should tweak. So, that I get whatever specification final amplifier is specified is that clear. So, difference between analysis and design is clear in analysis we are desired the expressions, but we never look back and say why what should I do now here we says that go back and see oh if I change this what will happen and if I do this what will happen.

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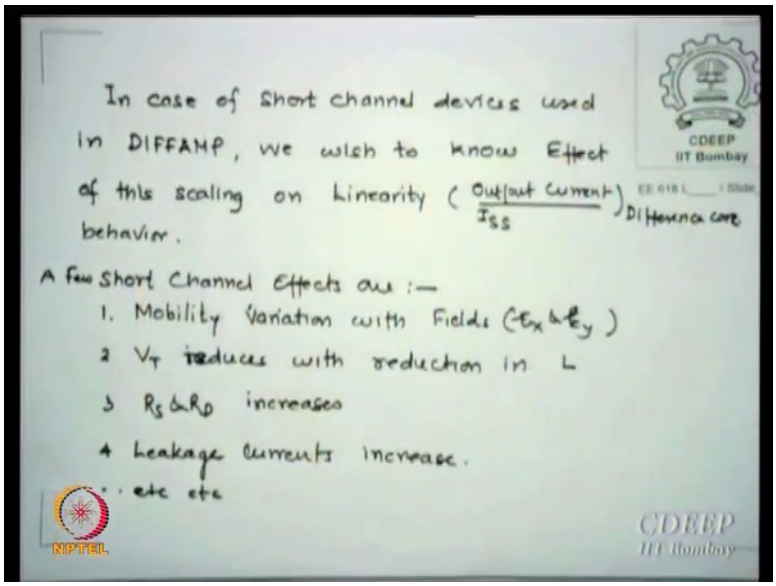

So, I design only on 2 such things and I will be Satisfy before we quite for the day we will solve one problem at least expressions I will give again. Since we are now going to even. 35 is a short channel device, but 90 nanometers below is certainly very short channel device and the current technology of R F and digital is around 45 down. So, many worries are there, but one of the major circuit worries is what I am looking into of

course, there are variation in mobilities because of mobility becomes functions of fields both E x and E y the gradual channel of progression is no more valid repletion approximation is also a pseudo approximation.

V T reduces with reduction in channel lengths, please remember higher the channel length V T is nearly constant has channel length goes down V T case following then the worry which is most me is the third one which is increase of R s and R d source with distance and drain with distance of this source drain areas as everything shrinks well by 8 actually increases is that clear because that increases that series resistances of source and drain is one of the major of course, there are huge problems in leakage currents, but that will see later is that clear. So, there are of course, there are many more short channel effects right now as specified this from the circuit point of view I know even if it reduces I know how much mobility changes I know for that how much.

So, I am not worried too much on that I will designing with this, but this something I have not earlier calculated now I may have to see remember mobility and V T's are still difficult values they will be specified for a node. So, which is not in my hand, but I know how to work with this leakage current is also technology dependent of course, is circuit dependent also to great extent, but in that case at least we have designing from the process itself to minimize the leakages, this something is not care taken care in long channel and this is the only one which I am going to show you please do not think there is no influence of others everyone is influencing badly, but the one which I can immediately see my worry is this.

Do you believe short channel device will be better or a long channel device ok the criteria is the linearity because amplifier what is important the linearity do you believe at the short channel device will be more linear or larger linearity then the long channel what is your idea Concept ok.

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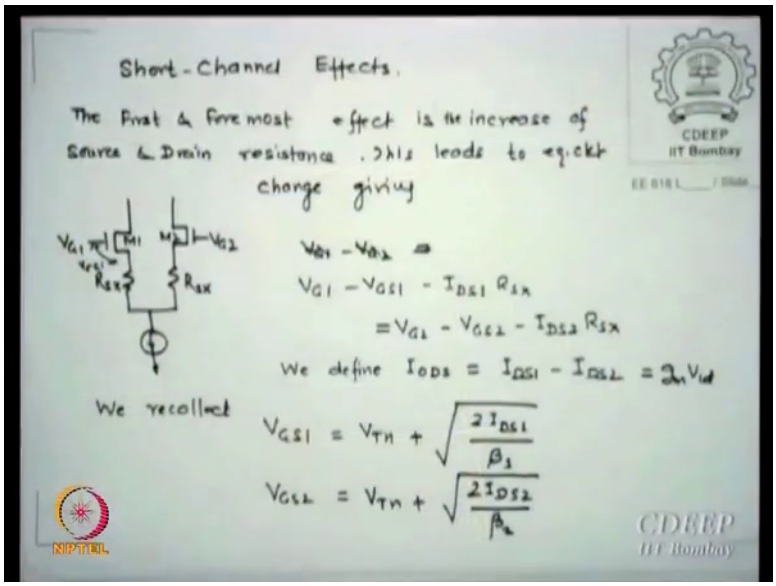

The drain resistance anyway adds up to the drain value R o plus something that that is small we do not worry too much, but if the source side had the resistance this R S X is the source resistance of the M 1 and M 2 what do they act like source degeneration is that correct great things happen. So, let us do for a normal this device we have done it V G S 1 is V T N plus 2 I D S 1 by beta 1, no R S X use right now, but V G anyway V G S 2 is V T N this.

However V G 1 minus V G S 1 minus I D S R S X is the value now this value as not there earlier in short channel this value appeared and that of course, in the otherwise V G 2 minus V G S 2 I D S 2 R S X now we define a term I O D S which is output current difference of output currents I D S 1 minus I D S 2 and which we know is g m V I d we know this we have already calculated. So, what is the major of linearity whatever is the input current change how much is the output current change if that is better I say yeah we have better linearity F naught I would say it is less linearity.

We want I O D proportional to I in. So, if they are larger then I say or we have better linear is that expression all of you because g m V I d is the current the transistors converts voltage into current. So, I will see linearity is only coming become of the current available if current reduces that is the V I d term na we said the length I C M R beyond that it is not linear, we are looking for where up to which this relation is valid. Please remember these expression we will use of10 V G S V T N plus under root 2 I d by

beta is a very standard we have replacing I D S into V G S or V G S into I D S this is a very standard technique.

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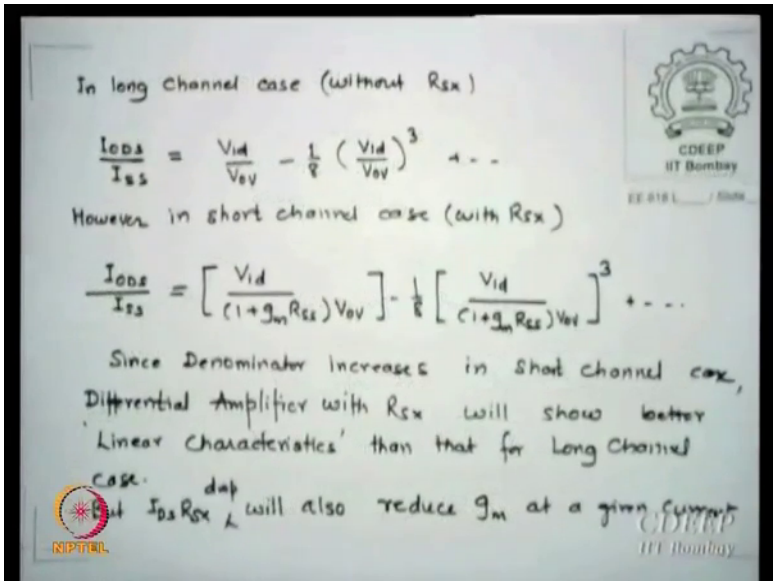

In a long channel device please remember what is non-linearity of I V character I O characteristics or V o V n characteristic is can be done by taylor expansion taylor series expansions, if I do taylor series expansion the I O D S by I S S if you want you can give read some papers I have just copied from some paper. So, you just check it I O D S by I S S, V I d by V O V Say I am plotting the ratio of output current with V I d is that trans conductance were clear output is the current input is the voltage. So, I am just doing that this is current which is actually getting at the output I S S is the normalize current and V I d is your voltages. So, I O D S by I S S V I d by V O V minus half 1 8 th V I d plus higher terms is to are going to enough cubic term is equal to enough.

So, if you have long channel device this is the expression is that I O D by I S S V I d by V O V minus 1 8 th V I d by V O V cube however, in the short channel device what should I replace now this V O V will then become because of the V Generation 1 plus g m R S times V O V we are done it earlier and I just replacing source de generation value. So, the new value of V O V will be 1 plus g m R S time V O V, R S S this sources just current source is the distance minus 1 8 th of this is now do you see the denominator is increasing in the this since the denominator is cube here and increasing short channel

case different amplifier with rs is actually show a better linear characteristics can be long channel device ah.

Student: Naming for the (Refer Time: 72:48).

What.

Student: Naming (Refer Time: 72:51).

That is true, see what is deriving it is virtual something a lose something, but this is get the point this was something which many people then relies that short channel device everything goes wrong here is something can do good the linearity may improve and that is something why we then a new design I start I should look into whether which technology and using and what linearity addition I got through that has the advantage on output swings because some application may help you with that is that you said na someone said in the last line [FL] if I D R X drop will also reduce g m equivalently. So, I am not saying that there is no penalty is a penalty, but at the gain of linearity.