CMOS Analog VLSI Design
Prof. A N Chandorkar
Department of Electrical Engineering
Indian Institute of Technology, Bombay

Lecture – 11
Differential Amplifier

I think we have done this much part.

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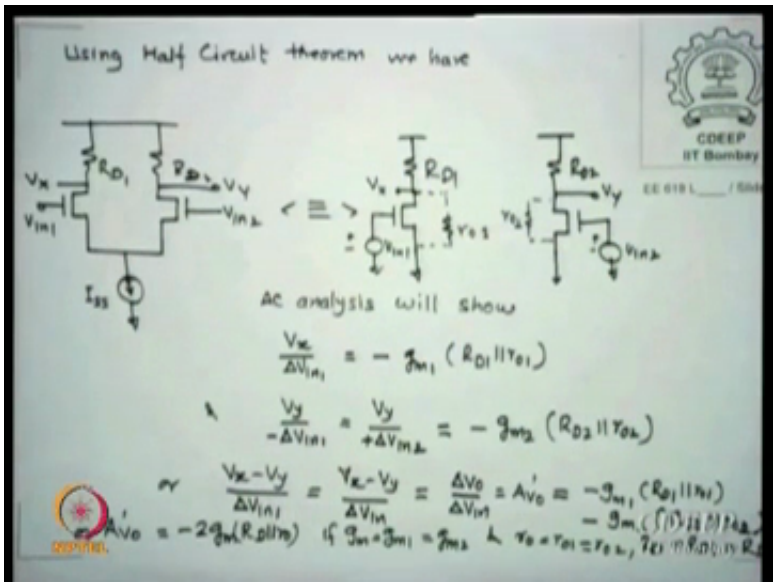

So we say DIFFAMP can be solved using a half circuit method, and the condition we said that the system should be symmetric across some vertical line, and then left side and right side can be independently handled. And we are shown last time some theorem which is given in (Refer Time: 00:46) book, and using the same method and across this, there is a symmetry. Please remember here one of the thing I assume that it is a differential system what did I say V in 1 V in 2 are such that one rises by delta, the other decreases by delta, but this is not a really a condition, we will prove that. This is not necessary, but initially we assume that should be necessary part.

Now, I will show you that is not really necessary, but first let us do. If it is assumed that typically this OPAMP can be converted into half parts, and you solve output voltage at this by simple amplifier minus gm 1 RD parallel r 1. Similarly you do for the other side which is V y by minus delta V in 1, which is V y upon this minus gm 2 RD 1 or D 2. And if I subtract or add whatever it is, I will get gm 1 RD 1 parallel r o 1. Now this idea that

A V dash 0, which is essentially when I say r o equal to r o 2 is equal to RD 1 equal to RD 2 gm 1 is equal to can be reduced to 2 gm RD, and RD's are smaller normally than r 0, then it is same 2 gm r o, nothing very great appears ok

We can do it analysis which is much more rigorous, which we have been doing all the time. So, there is a second method which I am not showing you read from the (Refer Time: 02:24) book which is actually a circuit technique, what essentially they will do. For example, they will assume that one of the input is grounded way into, and then see that a performance influence of V in 1 on V o 1 and V o 2. Then they will figure it out what is the V in 1 is 0, and then they superpose the results to get the net gains. So, that is the very standard technique of super positions.

So, lead that other technique which is more popular circuit technique, this was shown to you, because DIFFAMP shows symmetry and therefore, it is much easier to solve this, this method. It is not that this is the method or something, but if you see something simpler, you probably go through it. Please remember in that case, if you are using this, this will be driving this. So, some kind of a source follower outputs are given to the common gate or common source system vice versa. And then you have to do some real analysis to get the normal analysis done, which probably you can read in case some of you did not find that or not understood come to me individually, I will solve for it; that is nothing very big, but this method I liked it very much, because for a DIFFAMP case at least this is very good and simple.

Student: (Refer Time: 03:47) similarly.

In the region of V o V n, circuit is linear, devices are in saturation, you are right; however, there is an issue.

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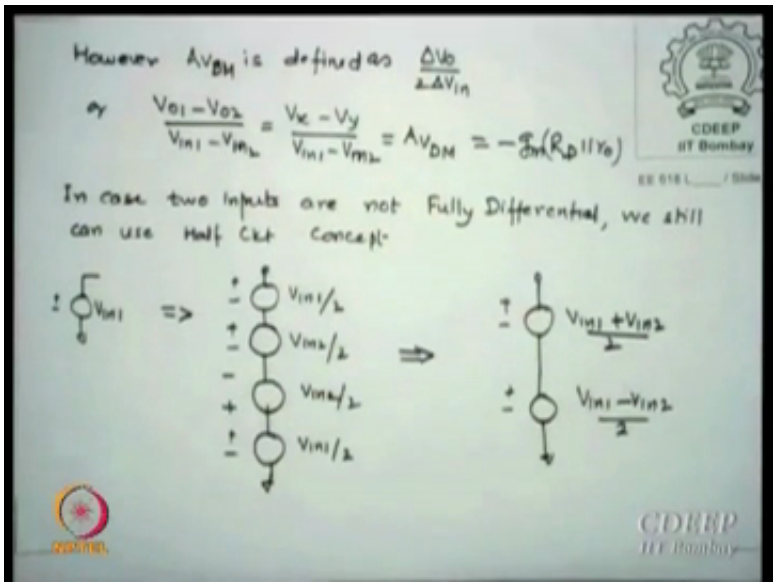

If you are looking a difference gain as V o 1 minus V n 2 upon V in 1 minus V in 2, which is called A V difference mode, then if this will become gm RD parallel r 0, that 2 will go away; that is only thing; however, the point which we actually took care in all our definitions so, far we said the V in 1 V in 2 are such that they are differential. What does that mean? Mean said if one changes by plus delta V n, the other must go down by delta, but that is not very necessary, as I show you later. This is a good condition to start with and we still say it can be still doable, even if they are not fully different. We can see that it del V n 1 can be broken into V in 1 by 2 plus V in 1 by 2.

Then we can add half V in 2 by 2, and subtract half V in by 2. In series power supply four in series; such that V in 2 cancels. Otherwise V in 1 adds. So, this is still V in 1 is that V in 1 2 V in 1 2, they are in series. So, V in 1 this is opposite, V in 2 are opposite in polarities equal. So, they cancel. So, this can be written as 4 supplying count series V in by 2 plus V in by 2 minus V in by 2 plus V in by 2. Keep doing this any number if you have this now, this is 4. Similarly I can say if this is, show that I can write then I V in 1 plus V in 2 by 2 and V in 1 minus V in 2 by 2. So, the statement that this can be represented by 2, such series; power supplies or supplies or signal supplies.

Now, you can see from here what is this value could look be, looking for V in 1 plus V in 2 by 2, its defined as common mode voltage, which essentially can occur, because if V in 1 is equal to V in 2. So, V in 1 plus V in 2 by 2 is V in 1. So, it is essentially saying it is a

common mode voltage whereas, subtraction is difference. So, any signal therefore, can be represented as common mode signal plus difference mode signal, because it, then why I said DIFFAMP, what is the important characteristic of DIFFAMP? That it rejects all common mode signals as much as possible.

So, now we are representing this into series combination of common mode signal, and this. Similarly I can do it for V in 2 on the other side. And I am not saying it should be this. I repeat this is that ok so.

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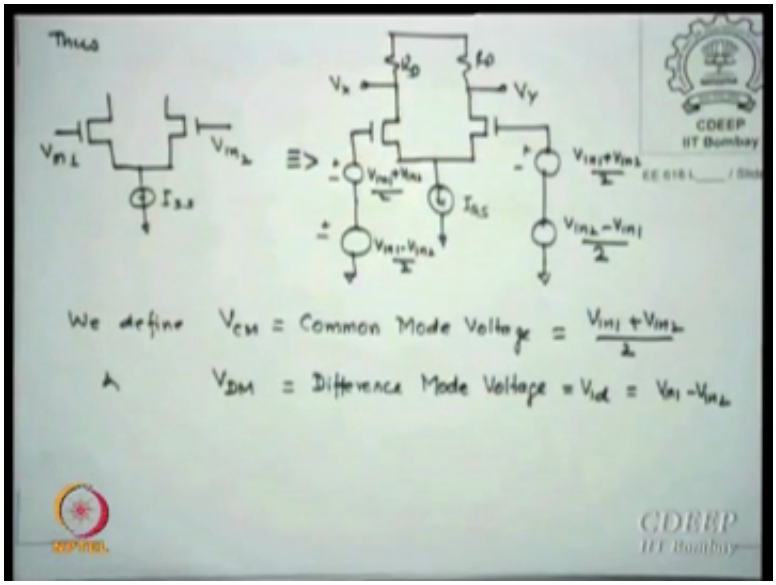

Equivalently saying I have a two sources, any something like this, and only thing is you can see here V in 2 minus V n 1 here V in 1 minus V in 2, because that is what the values you had, and correspondingly you wrote this, and then we define as I say a common mode voltage V c n is V in 1 by V in 2 and difference mode signal is V in 1 minus V in 2 is that. So, this representation of the. So, now, I am not saying that it goes delta, this my. I am not saying I said whichever it is, I will do break into equivalently this, which will always give me some common mode signal and some difference mode signal ok.

Now, the idea behind all this gain was, that what is the gain with for this, and what is the gain for V c this, since there are two sources. Now, So, we say what is the method we will use. We will figure out the gain for difference, and we are get the sec gain for common mode, and check it whether one is much higher than the other or vice versa. Whatever happens, we will see what is and if it so happens, that the. Of course, there is

another term which you should know; that is called common mode gain converted to differential mode. So, it is called A V c m dash dm which will calculate is that, this is only a definition, everyone knows for last so many years, and not figured out any other thing. I have not got anything great new things in this. I repeat I just broken the signals into common mode and difference mode signals.

You can see this is plus Vi d by 2, this is minus Vi d by 2 V c m is same that makes my job much easier, because if V c m is same on both cases, then the circuit will become even simpler. So, I have now two signals.

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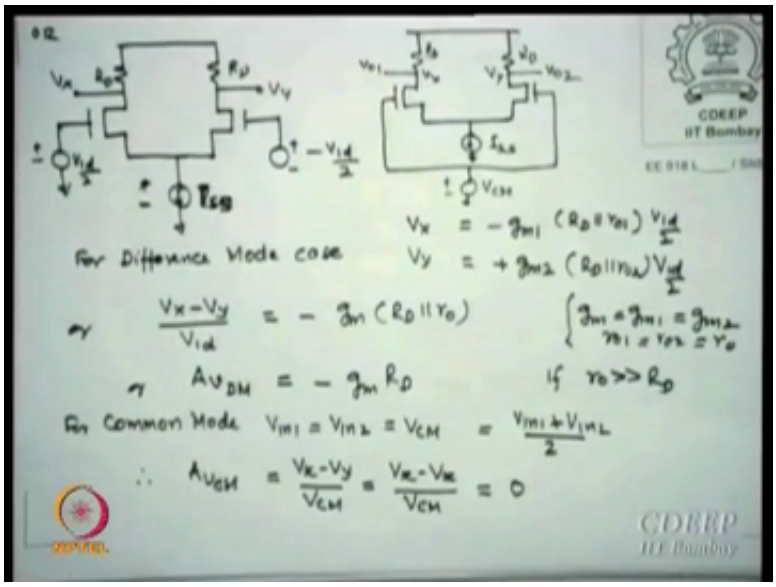

One is plus V i d by 2 minus V i d power for the difference mode. And for the common mode I another equivalent circuit we say, where it is common to both V c V n c m, individually putting is as much saying common to both. So, I had to circuit to solve, and if I can solve these two circuits, then we know. Just now we did V x is minus g m 1, already parallel r o 1 into V i d by 2 at this point output just now we calculated.

The other side is P y g m 2. This is says it is minus Vi d by 2, I put this plus. So, it becomes g m 2 already parallel r o 2 Vi d by 2. So, I calculate differencing again which is V x minus V y divided by V id. So, which is nothing, but g m 1 g m and let us say g m 1 is gm 2 equal to gm and ro 1 equal to ro 2 is r 0. What does that mean? The two transistors are identical, we will get rid of this also, and say if they are not what will happen. So, if they are identical the gain becomes just gm RD, which we just now

calculated there, nothing great happens; however, if you look at for the second circuit, and do similar analysis V x minus V r, this gives me. Since Vx is equal to V y, then both input will give same voltages outputs. So, the difference being 0, the gain is 0.

So, if I now take a ratio of A V d m to A V c m it is finite; that means, at no time common mode signal will actually get amplified, is that. This is what essentially is the main feature of differential amplifier. The assumption in all this was, I repeatedly say that why this cancellation we said, is important, because in real life when believes these two transistor will not be too far. There may be two input signal lines or sometimes one ground in one other line, in which case the noise may not over put separately for different places. So, assumption is, if noise it is on this something, same noise will put something on this. And if that happens, the common mode noise will actually get rejected. So, that is the feature this DIFFAMPs provide. So, whenever you are looking for rejection of noise, you better try with a differential amplifier system in which you can reject common modes. Of course, in real life we know Vcm is not 0 ok.

It is some finite quantity. So, the ratio of A V d m to A V c m is not infinite, but large enough infinite numbers, and that value will, call it as common mode rejection ratio. The slightly different way will explain that, but that is what we are looking for is that. So, what is the DIFFAMP property. It will only amplify differential signals, but not amplify, or actually we will be not amplify anything or output will go to zeroes difference if they are common modes. Please remember individually you will still can get outputs single stage kinds, but difference of them is 0. Please remember V x is same as V y, it does not mean V x is 0 and V y 0 is that. So, this issue has to be clear that transistor is amplifying. It is not leaving its job, still amplifying, but both side being identical output. So, each identical, and therefore, the difference of the two is 0 that is the reason one, we say it is rejected.

So, if you only pick up output here, say oh there is a noise reading, noise is riding on it and amplified noise is riding on it in fact, but the other side is also riding the same way. So, if they take difference, the common part will cancel, and that is how we say noise gets cancelled. So, please remember that if I make some time wrong statement which you are very smart to catch immediately, what I again say that I am never saying that V x is 0 or Vi 0. I am saying V x and V y are equal; that is the statement I make, even if there is some issue. Please come back is that these issues are actually. All of you have done

this earlier. I am just trying to see how do we use them in DIFFAMP design today. We of course, will not be able to design. We are going to design a DIFFAMP at the end, and there are certain other parameters of interest other than SMRR.

One of course, is the difference gain, how much you have. The other is, we will like to know what is the common mode gain you get in reality, and we also will like to have more specification for a given DIFFAMP, two of the specification. Maybe I will tell today, one is called output swing, at the end of the day how much output is available to you from minimum to maximum is very crucial for the next stage. Therefore, I will like to know what is the output swing, and the most important among them is, what is the possibility of device remain in saturation for any kind of Vi d; that is minus or plus. So, what is the minimum and maximum input which is possible for keeping devices in saturation, this is called input common mode range ICMR.

So, these two, the another two more parameters which will look into later, not today, possibly is the power dissipation, because for any design that may finally, limit all your performance. If I say this is one milliwatt; that means, we did is so much. The maximum current given to you is so much, I d d into V d d is the power. So, once I say one milliwatt 3 volt 2 volt you divide, and that is the maximum current drawable from the power supply. So, now, you have to assign how much here, how much here, how much here. The net current flowing from the power supply cannot exceed the given value for the given power decision and the last, but not the least.

Ah after all in a mass transistors base any circuit there are hardly. I mean, though I am using RD's, but they are generally not there, we will like to have outputs driven driving next stages, and what will be the next stage input impedances capacity. So, they will be actually driving a capacitance. So, when you give input change, how much the output takes time to change, is called the slew rate. How fast that is c d V by d 0, how much current is available at the output for capacitor to charge or discharge is very crucial, because that decides the speed of this circuit or some way related to next stage, how will little respond. So, another term which will actually like these are terms. Why I am using same term, because this is what OPAMP specs are, by the way the circuit which we are just shown which will show now, is the first stage of OPAMP ok.

The first stage of OPAMP is the difference DIFFAMP. So, I am trying to use, but the final specs also are same for either OPAMP or DIFFAMP. So, I repeat I am looking for power dissipation. I am looking for slew rate, I am looking for output swings, I am looking for ICMR's, and I am also looking for different scheme, and also looking for CMRR. There is another term which will come at particularly in the case of this, which is PSRR. We will see if power supply has some changes, what it influences to at the end at the output. So, we will also have another parameter at least not in the fm. I will say I will put it finally, to OPAMP which is identical stage. So, I will solve all of them for OPAMP. So, PSRR, so that also is another important issue which you will have to address to. So, these are the specification.

So, normally what they will give you another thing which I did not say; the bandwidth. So, far I am not putting capacitances. So, I am, has you thinking there is no and there finally, it will come from the bandwidth, and bandwidth is something to do with, not only the rc time constants you get, but also on the ft value, which the device is able to give you. And I repeatedly saying you that typically tenth is what you should be able to use safely, if your device has to operate in proper mode of operations. Now that is something we will talk about in a frequency response part, that what is the bandwidth relations. We already solved one small problem which is, say bandwidth, and these are some way related, because its first pole or dominant pole, is essentially related to bandwidth. If many cases we saw, assuming this is the dominant pole.

But in fact, we will show you later those who have done my earlier device course. I use that method zero time constant method instead of using normal (Refer Time: 18:37) technique. We show you that we can figure out at least quickly. If not very quickly, what is there which is the dominant pole, and if you get the dominant pole that is your bandwidth. If you want to plot full bode plot; that is all poles on zeros for stability purpose. You will have to go through all transfer functions, get all poles and zeros and plot it, and find phase which is another terminology, which we will use later, how much is the phase margin ok. So, there are other parameters will come in OPAMP. So, wait for that, till then we will only look for DIFFAMP characteristics, which is the first stage of an OPAMP ok.

So, is that. So, these are some issues we must address now. So, that at the time of OPAMP design I in my mind, what I am designing at, let me look into common mode again.

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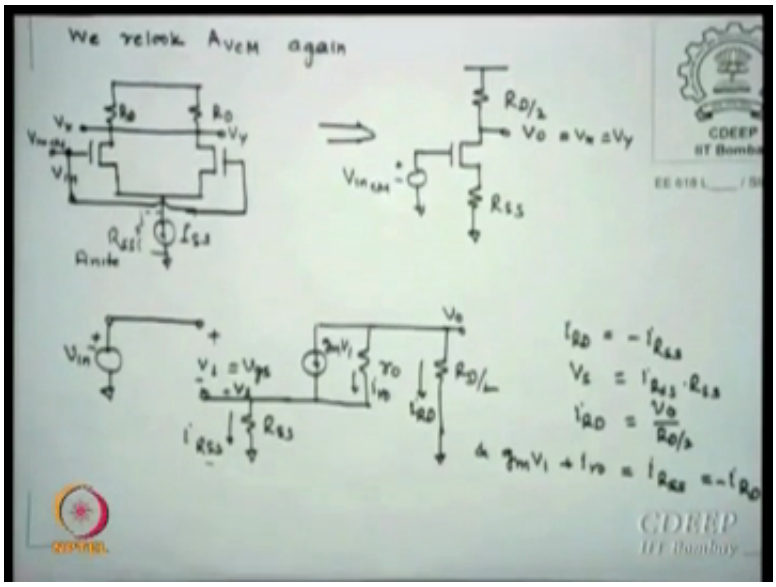

If you say V x is V y, I join them, and I there is a common mode signal which is being c m. Sorry this is here, this is V in cm both are both sides same. So, I shown like this RD's are this. So, if you see it is essentially equivalently same, and let us say this current source is not really ideal current source, which will never be actually in reality, there is nothing called ideal current source. So, there will be some resistance associated with, and that resistance is Rss. So, what I am saying is. So, if I say equivalent circuit for ac, of course, this V cc 1, but that is actually going to ground.

I RD by 2 other combination, and this is less with signal of V in cm equivalently, this is a very simple amplifier, which is this amplifier, this is a common source amplifier with source degeneration, though I have solved it, I inadvertently did not realize that I should not solve. So, I kept solving, and then I realized that I already solved this problem. So, I need not resolve all again, but just for the heck of it, the equivalent circuit is as shown here, this is the I Rs s, this is I RD I RD is minus I R ss, because sign is taken down. In fact, I should have taken sign up. So, that would have been same, but does not matter the voltages would have change in the sign, then this would have been plus, and that would have been minus. So, it is saying the same.

I RD which is V 0 by RD by 2m then V s which is the source voltage here is, I r s times r s s, but I R s s I r d. So, this is this I R s s is minus I RD which is gm V 1 plus current in this, you can see the current here plus current here must be equal to current here, which is I r s, which is minus I R d. So, this method which we have earlier applied, I am just rewriting, you need not even rewrite. this is exactly what we did earlier and just as I say in advertently I forgot that I had done, I keep solving thing, then I realize why I am doing it, I already done once.

Student: Sir.

Yes.

Student here body for the gm V is not take.

Is not taken. Normally what we will do in the most cases in DIFFAMPs or something. We will source and bulk. We are connecting most cases specifically, but if not given sgmv must, you can even now add gmb's non circuit. We already solved with gmv. So, it is not that we cannot, but for the first take we always say the I c circuit will be allowing us of course, in a long channel devices we always did that, but in a short channel, we cannot neglect gmv which is then after, when I say if I scale down what I should, I will get hurt and how will I get out of it so that maybe after all, that I say from here to here. What is the my problem, which is your problem my time, it was very straightforward, I worked. well nothing went wrong, but now everything goes wrong. So, how to get out of it. So, this analysis, please I mean those who wish to write, figure it now, but I do not think, there is nothing great I had done. Just see the last expression.

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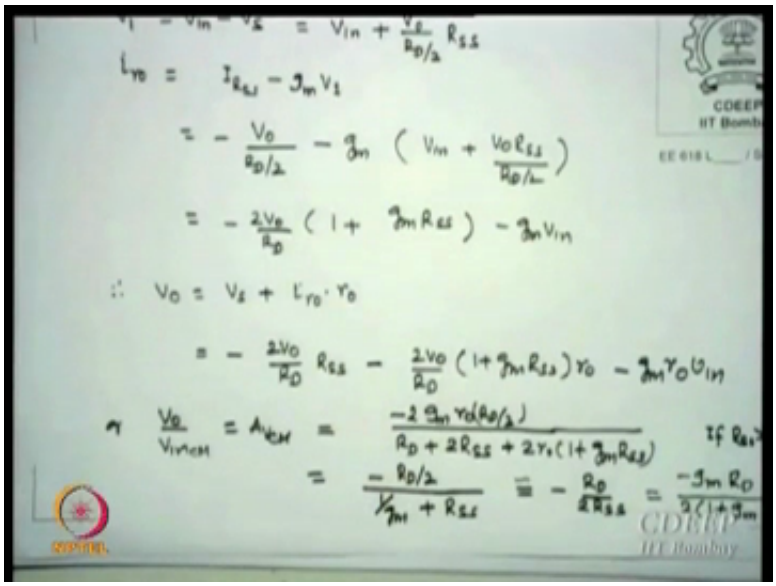

All this is given by me earlier. So, finally, V 0 by V in same which we call A V c m is minus gm ro parallel RD by 2 r o into RD by 2 upon RD plus 2 r. This is expression as we derived. And if we say Rss is much larger than gm 1 upon gm, which will be Rss is the current source output resistance. It is very large. So, this may reduce to. Firstly, you may say minus gm RD upon 2 1 plus gm Rss, or if you say this is also true, then it is minus RD by 2 R s s. This is same thing. What we derived for source degeneration load resistance divided by source resistance; that is exactly what we get; however, why we actually derived this, because now we say that this A V c m is not 0. Is that point clear. We are now saying at this, the a at one end, at least the voltages are is g RD by Rss, because Rss is not infinite ok.

This is the most important part which I want to explain Rss is finite, and therefore, one must say that the V 0 by V m c m will be finite, and it will be minus RD by this is RD by 2. So, this two is only coming, because of that. So, RD by 2 by Rss, this is essentially. We still assume that g m 1 is gm 2 Ro 1 is Ro 2 or something like this, but in case they are not there, which is what is, why it can need not be there, what is the cause you are anyway doing technology course. You are doing other design course, what will be the cause in which two transistors may not be identical, what could cause it anyone. The reason why this mismatch occurs of variety of reasons, the dopings on different transistors in the, what we call channel implants are not correct. There is a special

problem, there are many issues boron depletion is another issue, and there is issue of different w bias, actually during lithography's ok.

So, these are called mismatches edge effects, and mismatches they will be there. Do what you, how small they will be is, what is important. We will prefer them to be almost identical, but never identical as close as possible. If that happens that the device, two device normally m 1 m 2 being so close, this difference will be very small, but ideally this is only a statement in real life, the issues are different, there is, may not the only one DIFFAMP. There will be n DIFFAMPs, each will have different variations in real life variations may cause on chip variation, chip to chip variation, and wafer to wafer variations. So, there are huge problems at the end of the days called variability issues, and one has to take care in design. Now variability issues I like threshold may variable plus minus 10 percent, then what do we do ok.

Our assumption is, it is constant. So, everything is fine w by l is constant. All that issues are temperature is constant, all these issues are not true in real life. So, at least we should look at least some of those variations, and see what will it influence, and that is what designers should know apprising, is that the issues are related to technology and they must be brought in your thinking, because at the end device would be fabricated on silicon. Our circuit to DIFFAMPs silicon does not listen what you want to tell she. It does what it wants, and then you are left with thinking why did the other way I wanted this, he is not doing. So, what should I do now, that probably he will do, what I wanted that some gain you can play ok.

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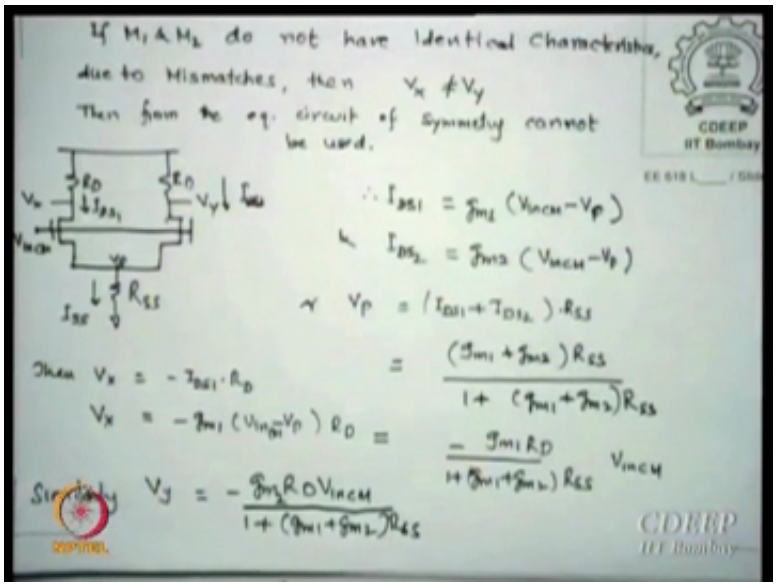

So, here is the case which is of relevance in their life. Let us say m 1 m 2 do not have identical characteristics, which is very true in fact. So, that, then the V x is not equal to V 1 that is, but for sure, because then if they are different, they will not have the same values, even if signal is common mode. If gm's are not same, how can you have same drops across the RD's? And therefore, firstly, even RD's are not same if the delta RD goes with that some plus some minus. So, there are issues, and issues mismatches are very difficult to handle. Then of course, the symmetry things should not be really used, because they are not really symmetric essentially.

We can, but I do not think we should use that, then we just calculate the currents as simple. I have one input common mode, and let us say this voltage node is V p, now if we say. So, ideas one is gm 1 V in cm cvp, and ideas to gm 2 V n c n minus V p. Then V p from this solution can get gm 1 plus gm 2 by R s s 1 plus gm 1 plus gm 2 into R s s, and then V x is something like this, where this one. Sorry if that is. So, that is true. I am sorry I made, I think will lower down many corrected [FL] there is fine, thank you.

So, if I find V x and V y it is minus gm 1 V in cm minus V p into RD [FL], and then I solved this is minus gm 1 RD 1 plus gm 1 gm to R s s into V n cm. Similarly I can calculate P y drop nothing else drop across RD. So, I can calculate V x, and I can calculate V y. What is the gain we are now looking for? That is what is called conversion of common mode into difference mode, because we are going to get a signal difference

gain, which is V x minus V i with reference to what? V in cm. So, gain which is of more relevance is not just the way I showed you earlier. It is essentially this V x minus V y divided by V in c n; that is the gain which is many times is called A V cm dash. Have you written down, then I can show you next slide.

Fine. So, as I said I am interested in the difference gain for common mode signal, which is V x minus V y divided by a, and then I subtract g m 1 minus g m 2 delta.

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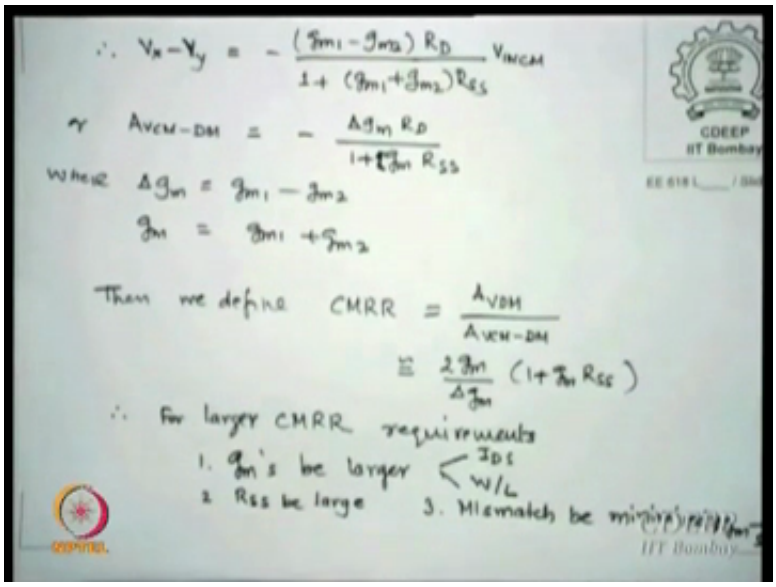

This into V n cm, and that, and then I defined the gain. It is A V c m dash dm, is that clear. The new definition is A V c m dash dm, which is V x minus V y by pcm. So, if I divide this, here I get gm, then I define g m 1 minus gm 2 is delta gm normally how my. Ideally how much it will be? Delta gm will be 0, if we say gm ones are equal to gm twos or what it is, and we also define a term gm, which is gm 1 plus gm 2. Sometimes they define half of it, I have defined as it is.

So, in some book if you say divided by 2. So, 2 gm will turn appear in replacing this term. So, that two sometimes if you see, do not think [FL], because I realize, I figure it out in the book, they are used to I think, but I was solving and I had to define something. So, I kept it. So, please remember this is my definition. Generally it is half, they will put it average, there this say, but since I have not used it, my value may not those tools somewhere, and then we define the term A V d m divided by A V c m dash dm is essentially what we called as common mode rejection ratio. And if you now divide that,

it can be figured out. It is 2 gm, because gm are, they will cancel from there. So, 2 gm upon 2 delta gm into 1 plus gm r s s. So, since we said we are one of the main feature of a DIFFAMP is what. What did I say. It should be able to reject on mode.

So, if I want larger CMRR'S, typically what is CMRR in db's for a OPAMPS, which is used in the lab, typically like 7 4 1, how much is good. So, 7 4 1 has at based 80 d b's, 80 d b's kind. Normally we would prefer a good families. How much 120 db. So, if you have to design a 120 db OPAMP, you will figure it out. It will create hell of a problem for other parameters, particularly the phase margins. So, there is an issue how much CMRR I should be allowed. So, that I should get the other performance also, as good as I want that, is the design issue, is that clear CMRR is therefore, kept flexible term. They say minimum CMRR should be 80 db. So, you are not saying 120 db, because; otherwise you cannot design it. So, issues are always clear, same way we will never say power supply power dissipation should be so much.

It is very difficult, it should not be more than so much or the slew rate should be at least this much, gain should be greater than so much. These are the bars or the upper and lower bars. We must decide, because then only design is possible at any time you put rigid specs, nothing is designable. So, one cannot design a chip with very rigid specification. You must say more than, less than, whatever the bounds you can give, please give it, because then the designer has something to play on [FL] that has to be understood. So, if I want larger CMRR from, this expression has got the two transistors, better is CMRR delta G and [FL] that is transistor in a larger gm. Means what is larger gm. Means either it is driven by larger currents or they have large size transistors.

Please take it this, large size word should be taken with a pinch of salt, why, because large size means that, generally lengths are very rarely changed. So, it is the widths which are changed. If bits are changed what will change. Capacitance, because capacitance are normally needed proportional to W all parasitics. So, essentially you change the W by L. You will be actually talking about increase in capacitor in change the W to higher value, yeah ideas will increase, everything will go nice, be gm will be higher, but then the bandwidth will be affected. Is that clear. And therefore, one must not say increase W by L, but one catch. I may say, I might have said also any time you are worried about device to be in saturation, put larger W boils for given currents. It will always enter saturation. Think of it, what did they say. If I make particular current which

is curl autumn, then see to it, your W by L's are much larger comparatively then it will always remain in saturation.

The other possibility of improving Rss and CMRR, is to make this Rss very large, which is what we will try, because current source as good a current source I will give for bias, that will be better, and if you can do this; obviously, your CMRR will be larger. So, now, you can see there are parameters which you are governing CMRR. So, if you change something somewhere to get other spec, this also will get affected, and therefore, do not CCMR will not respect, it is respect, which is to great extent variable greater than. I cannot tolerate less than 80 db fair, and fair enough, but do not say it has to be 80, it can be 85 90 or whatever it is what.

Student: Typically.

Typically 80 db, all OPAMPS general purpose OPAMPS at 80 db special OPAMPS, like Lm 2 3 2 3 or 3 2 1 or 85 76, which is another device. They are same or as that 120 db. They are low noise amplifiers, and they specifically try to improve CMRR'S, but their bandwidths are not very high. So, there is an issue; that is what I keep saying there are gains, different applications require different OPAMPS, or different amplifications, and there are different specs. So, you have to choose, if you are doing board design, then you have to choose from the data sheets, which one is it fit in chip. We do not have a data sheet we are to design. So, we actually solve it and figure out what is the, and another thing I keep saying, when I design something and I convert to layout, which is what one of the major output of any course of design.

Then, the first thing we will do is, we will, that layout which I had drawn for the poly for every region, then I will extract the circuit back from the layout, and then I will re stimulate that circuit, and you will be surprised that whatever initially specs with which you are drawn, the layout they do not match. So, you have to redraw or re stimulate change, something redraw it re extract till they are closed by assuming things are, because this layout is for a given technology rules, which come like you are working on 90 nano umc 9 nanometer technology. So, they are their layout extraction. Tool will actually follow them. So, you are very close to foundry. Is that clear, but even then there is no 100 percent guarantee that silicon will show you same performance, but it will still be closed to what you were looking for. Is that clear.

So, at the end of the day this is some turn around should be required, as many turnaround is cheaper or costlier, larger the turnaround cost increases the 1 fab you go through, you have spent already lakhs of rupees, typical cost for a 90 nanometer process for a 2 mm by 2 mm chip, or per mm square you can say is around 80 lakhs these days for academic. This can discounted price on a say 12 inch vapors, the cost is 2 mm 1 mm per mm square, it 8 lakhs on 90 and 65 nanometers for 2.2 5.35 it is 2 and half lakh. So, most of the designs which we do in the lab is only for the sake of money, because otherwise the money is too high DIFFAMP with.

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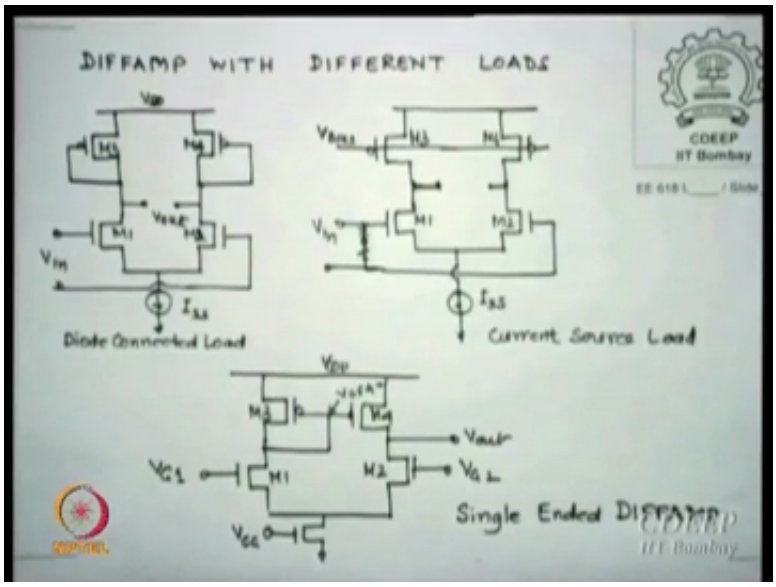

Now let us see DIFFAMP designs or at least DIFFAMP analysis once again, and there are three DIFFAMP shown here you can draw each of them.

Instead of showing V in by 2 n minus V in by 2, I am showing you one together as mean, that is the only difference from what I said earlier, the most important part which I did not say these are all CMOS DIFFAMP [FL] will not use any n channels. Now P channels other than together [FL]. So, these are all TMOS DIFFAMPs which probably are the ones which we will design, whenever gate is connected to the drain. Then it is called diode connected; say P channel, the source is at the power supply side, because you need negative supply VGS, as just to be at higher voltage. So, positive higher voltage so that VGS is minus the gate is connected to drain. So, device acts like a actual diode. What is

the difference between this diode? This is also a diode, and a normal diode they know, what is the difference the diode has IV characteristic, which is exponential is that correct.

So, in all technologies in CMOS there is no real diode made actually diode is this site change [FL], sometimes thicker oxide [FL] characteristics change [FL], but diode is this. This is how diodes are made is it last, but not the least. So, the first one is a diode connected load, which I just now said this is standard n channel, two devices which is forming a DIFFAMP pair which is biased through a I s s source and this is my input. The second one is these are current sources, you can bias it properly through some standard biasing system, which will show later, and this can remain as a constant current source. It is called current source loads. Please remember these are P channel devices, and we are all the time feeling as if only n channel devices can be DIFFAMP pair. You can now inverse, you can have a P channel DIFFAMP pair, and you are n channel loads as well ok.

The third and the foremost of all these; these are very specific ones, and not often used in. Most of the OPAMPS, the advantage of these two are essentially, I did not draw it here also. These are double ended outputs, these are double ended outputs. Whereas, the third one which is the most common DIFFAMP used in operation amplifier in the first stage, is a single ended output stage, which is shown here. The feature is very interesting here, because here the two P channel, gates are connected to one of the drain of this side. At time if the divergent you can do other side also, then the output will be the other end. There is nothing asymmetric. So, it does not matter, but normally shown this everywhere. So, I am also, you can as well do here, and then take out for from there. it is only question of mirror ok.

The only thing which I did not say very specific here, this I s s; there in most cases will come from either applying a bias; such that this device always remain in current source mode, or actually it will be mirrored. The current will come from a current mirror. So, if the gate of this is connected to current mirror gate, then same current which you are passing in, that will pass in the this transistor and this will act like a current bias circuits. So, it is either putting a bias which sometimes good. If you have a ref, good reference bias voltage. I mean like band gap reference, or then you do it normally with current mirrors. This is what the single ended DIFFAMP essentially is most popular DIFFAMP,

which is as I say most popular simply, because all first input stages of OPAMPS are these ok.

But there as I said other it, there is a fully differential DIFFAMPs or fully differential OPAMPS. Then you do not need both outputs, fully differential and at though time. This cannot be useful, either of them will be used in that. So, to inputs to outputs oka is that called fully differential. So, in those cases, only will require first two; otherwise most general OPAMPS for stages simple one, single ended DIFFAMP. Now before we solve the case for the third one, which is most important quickly will repeat for the diode, we already solve this. So, diode connected load in load resistance is essentially the gm pal 1 upon gm parallel R o p g m, is normally very large compared to 1 upon R o.

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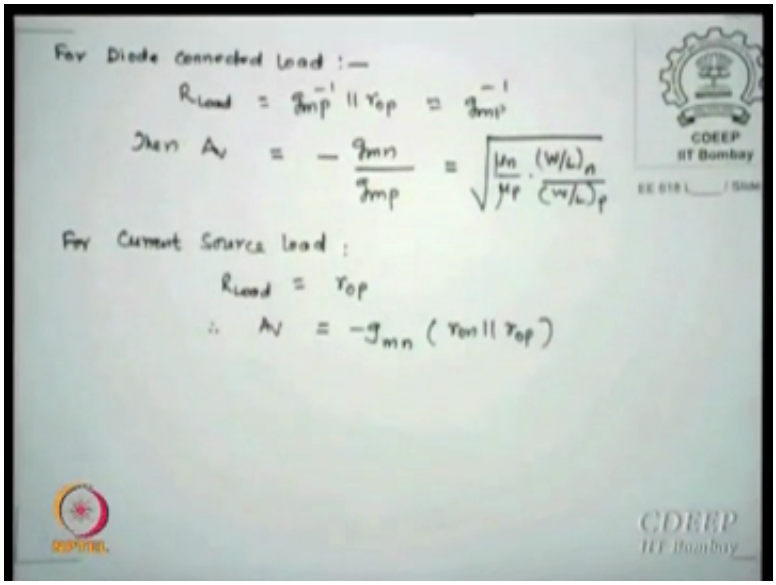

And therefore, it is normally 1 by gm p, and therefore, the gain is gm n by gm p, which is now you see the difference. It is mu 1 by mu p into W L by n by W L by p ok.

So, for a diode connected this the load for diode connected loads, the gain of a DIFFAMP is already its, if mu 1 by mu p ratio is 2. So, you have already got little extra gain out of using p channels. Then what is the advantage, if they are same, they could have been same, then this will have a cancel, then they increase the ratio allowed to increase more size of n channel compared to p side to here, already mu 1 by mu p ratio is giving additional boost. So, still n channel device will be larger than p channel. Is that the current source load, the load is only r o p, then A V is gm r n r o in parallel r o p, the

two r o s of the n channel and p channel at the output of parallel. So, they are parallel if they are equal, they will not be equal, because of the mobilities.

But many times they may be equal also, because you may adjust sizes. Therefore, you may have gm n r o n parallel r o p. So, these are standard difference gains for two of this, but what we are interested in, to the end of the day, is the third one, which is what we are going to design. Therefore, we should look into it little more carefully, is that these are trivials standard. This you can have already done earlier. These two we are just repeating the results there again. Only difference in earlier case, and this is the here this n channel p channel device. So, mu n by mu p will also a beta. So, mu n is one time mu n c ox the other is mu p c ox mu 1 by mu p ratio will appear, and that you must take care. Typically how much is the ratio of mu 1 by mu p in the actual semiconductors silicon.

Student: (Refer Time: 46:14).

I am not saying what.

Student: (Refer Time: 46:16).

What is the typical value of mu n by mu p in a normal semiconductor bulk.

Student: (Refer Time: 46:23).

3, it is almost 3 482 1400 something; however, in most transistors this can never be attained, because that the surface mobility is not as high as the bulk mobilities. So, the best of ratios you may get 2.0 to 2.3 and therefore, most of our designs are for 2. Now you may not get 2.3. So, you may say 2. So, generally if you are not given any value, assume mu 1 by mu p as 2. I may specify beta n dash and beta p dash. So, there is nothing you have to worry, but in case I do not specify. You can always use this as 2, because that is the most likely value, the best of mu n. You may get a 600 centimeter square per volt second, and best of that you may get it 300 centimeter square per volt second for holes in most mass technologies.

Higher technology even it is worse. So, it is becoming very difficult now to maintain even 2, but that is the game we play enough. So, that the interest rates are very much in control. So, that the mobility is roughly two in these are called surface mobilities. These are not bulk mobilities.

Student: (Refer Time: 47:40).

Very good normal diode [FL].

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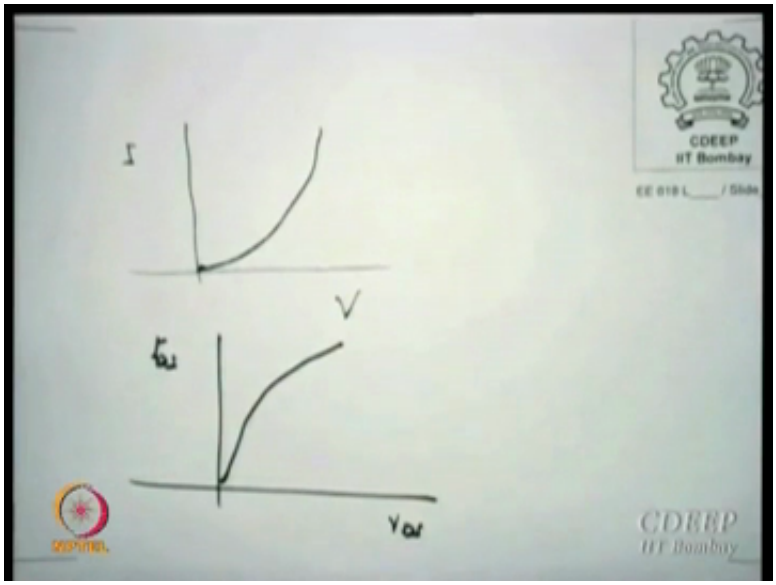

IV characteristics [FL] diode [FL] I d s V d s [FL], but if you adjust your sizes and V d s, they look closer to that. So, they those, they are not square lots, but they look similar and therefore, it is called diode. I said they are not diode, is that clear. Essentially this is the difference, this is a square law term is that, but this is good enough in most characteristics requirement. The major reason is in either case the current here also, is very small, and here also a also diode blocking is still possible. In the other case therefore, one says it is like a diode.

Let's look for the third one, which is the one which is of great interest to us, which is the first stage of OPAMP which is called current mirror DIFFAMP, current sink or current.

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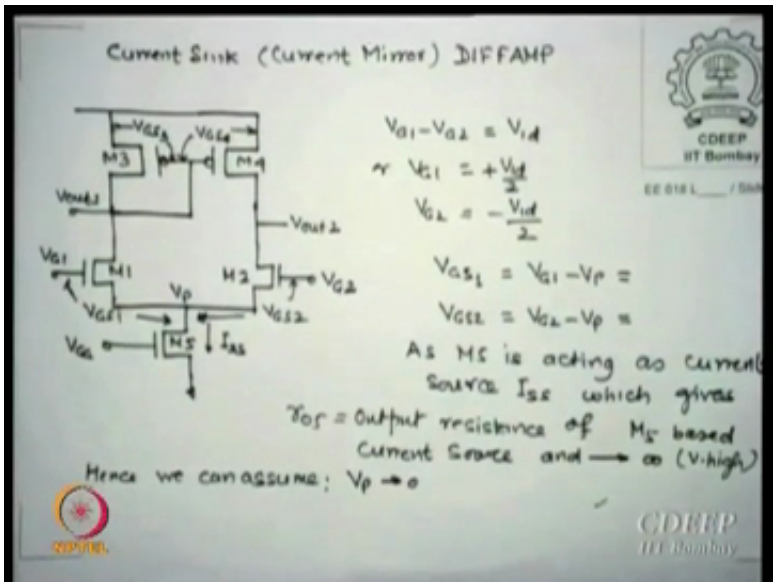

It can be called what are the difference between source and sink, whenever current starts from power supply, it is called sourced. Whenever the current goes to the ground, it is called sink. So, definition wise I just thought I should tell you it is actually sink source, current is sinking into the ground ok. So, in some books if you say sink. So, I thought I must like that, they may also call it sink source, still source of a current, but called sink is ground to be ground. So, it is normally derived out of a transistor m 5, and normally this Vgg either has to be controlled or a mirror can be brought, mirror current can be brought to pass in this this.

Now, we will like to first try to find out before we do it gains of this. Quickly look into it, there are some voltages of interest, this is VGS 3. Please look at it [FL]. first you draw figure, and then do not write this right, when I see. Let us draw the figure; that is most important and you draw on the figure first, then I will start talking, and then you can write. I repeatedly saying that capital and small and everything should not be unless stated. Otherwise by me please do not worry too much about it. There is a voltage VGS 3 for m 3. There is the voltage gate to source voltage VGS 4 4 m 4, both are p channel device. The gate is connected to the drain off m 1, or drain off m 3, both are drains. So, that is our output one V out 1 which we are not very keen to know ok.

What we are interested in the output at this end, which is called the actual output of the amplifier VG 1 and VG 2 are the input signals, then this is VG s 1. This is VG s 2 or to

say VG 1 minus VG 2 is the difference signal Vi d VG 1 is therefore, vi d by 2 VG 2 is minus vi divided. As we did earlier equivalently saying then VG s 1 is essentially this voltage minus Vp VG minus Vp VG minus Vp. Now here are the catch, this is the dc current flowing in this I s s, and normally it is a good current source whose output resistance r o 5 is very large; that is what the good current source is about. So, I am postulate. Now if it is a excellent current source, the change in Vp 0. Is that clear. V p does not move or ac wise, it is 0 delta V p 0 means ac.

So, essentially VG s 1 is VG 1 and VG s 2 is VG 2. This is my statement. I may prove now that V p has an mood anyway. So, that I did for earlier lemma I am doing. Now for real circuit, the consumption now I am saying. Please remember this is the statement I am making and based on this statement, I am going to make a this statement to you that I can show V p to be grounded as far as ac is concerned. Is that clear? If this is not large, some current will flow that is the problem. So, we will say right now r o 5 is extremely large, even if not very large is still doable, but at least we assumes. So, is that statement clear? Here is an equivalent circuit of the system, please see it very, I have done it very intentionally, a different way of drawing the circuit, this may help you to appreciate what I am saying.

So, look at the input side.

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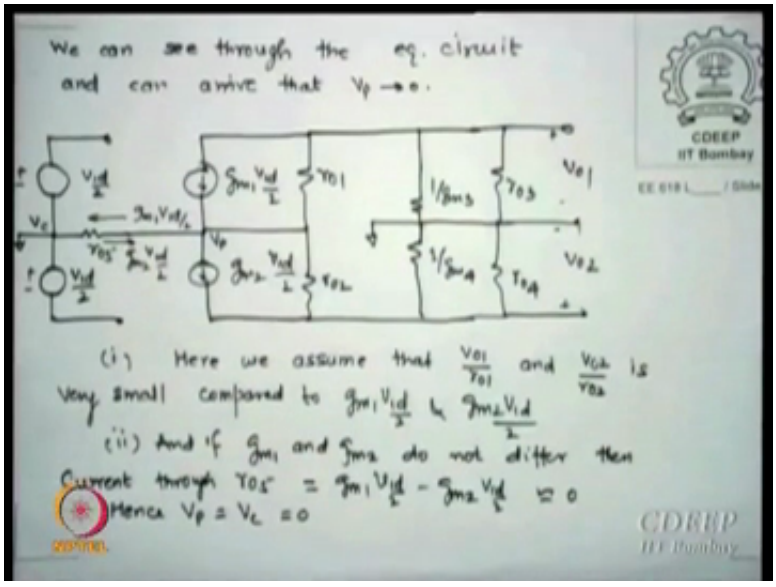

One is Vi d by 2, other is minus Vi d by 2, and this is that common point, where we say the output is. I mean this is grounded physically signal which is that point I am saying. I am actually saying from the ground this to the ground [FL] a minus Vi d by 2 [FL] plus Vi d 2 [FL] plus minus [FL] if you see the m 1 m 2 transistors, then it is gm Vi d by 2 into parallel r o 1, is the equivalent circuit for this. Please remember this is your V p, the other side is, please see the sign now, because of this V i d sign gm to Vi d is shown down going from source to this. This is ac signal. Please take it, this is ac signal across which there is a r o 2 is that.

So, m 1 m 2 have an equivalent circuit. This is common point V p. This is gm 1 V id. This is gm Vi 2, same way if we go ahead for 3 and 4 1 1 upon gm 3 r o 3. Now whichever, if it is diode this will dominate, if not this will dominant gm 4 r o 4. Now there is something which I am right now not showing. Here another source I will bring it little later, but right now I just, as if see, I see that is the equivalent I see now, while show you why I have not down then, and now I will show. Now the idea is something like this. If you see r o 5 register this side is ground say V p. Now we say the current in V o 1 by r o 1 or V o 2 by r o 2 are very small. Why we are, they are very small where r o's are very high.

So, we believe that those currents are extremely small. If that is so, this current, and this current does pass through r o 5 to the ground is that, this current and this current passes through r of 5 is that. Now the direction if you see, it is gm Vi d by 2 goes like this, gm 2 Vi d by 2 comes out of it, if you. Now say gm ones are very close to gm 2, and that the r o 5. If it is x, what is the current through r o 5 gm 1 Vi d by 2 minus gm 2 Vi d by 2, and that is very close to 0, is that in which case we may say the potential here is equal to potential here. So, if the V c is ground V p is equally grounded is that clear. So, that delta V p does not move by lemma is what I had used, but I now showed with do a circuit point of view that V p remains constant.

So, no ac current that voltage for ac is same as V c. So, this idea that in circuit hope it will use that sometime you know, because they may not show you this. They may suddenly put a ground there. So, you must know from where this theory has come that V p can be treated for ac as ground is that point clear, because in a book if you see they may not show all this. They may only show this, and show ground. Then you must not feel why this is grounded, this is how it is looks to be grounded, this is what you say in a

between the lines, what they do not write and what I can tell you from where they derive this, if that case will be [FL] a current sources [FL] current subtraction [FL] plus minus [FL] same way roughly, which is what I am assuming g m ones are very close to g m 2. Then we say this, there is no current in this a floating [FL] point with the ground [FL] ground [FL] register low [FL] potential [FL] that layer that is why you say V p is as much as ground.

As much as is a very important one, it is not really ground, but as much as it is ground which.

Student: (Refer Time: 57:45).

The reason why I did it was, because I figured out in the books they just draw circuits, without telling you any great thing. So, I just thought.

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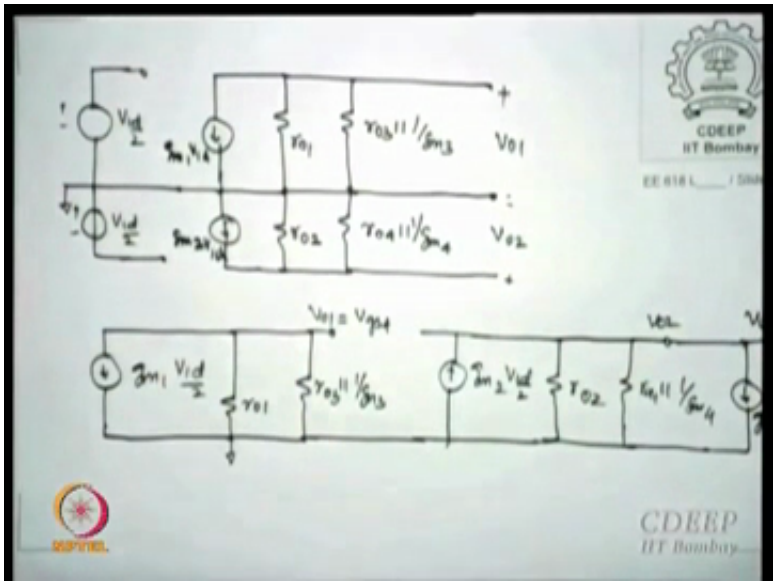

So, this is your input, this is your gm 1 Vi d 1 this is g m 2 V id r o 1 parallel [FL]. Please just a minute you can see if this is grounded, this is grounded. I can connect them. Is that correct. This is grounded, this is grounded. So, I connect them. So, if I connect them. Now there is some catch word is going on. Again this equivalent circuit is not accurate [FL]. I mean then what I did, I used this as a one common line ground, then [FL] this is what normally the figure in the class books, will be this kind. This have come from this. So, this is a technique which I should given [FL]. Now we see from here if it is g m 1 V

id r o 1 parallel this. Of course, it may, you may keep gn 3 or not, is up to g o, because the values will decide, but in real life we can keep them whichever is not there will go away.

Now, this fact is most important. Have you drawn the circuit, then I will explain that is the issue, which I am now telling. So, the output of the first stage m 1 m 3 can be figured out by a current source of g m V I drew shunted by r o 1 shunted by r o 3 parallel g m 3 is that have you drawn all of you. So, look at it this is the first stage m 1 m 3 stage, I repeat now you should, I put this figure. So, I have figured out, I first solved this m 1 m 3 and got V out 1, but now look at this V out and varied it gate connected to the gate here. This voltage is same as this voltage for ac, this is ground. So, this voltage is same as this voltage, they are connected all through. Is that correct? Now there is an issue started and that is what you [FL].

Now, you can see the output at this second stage which is m 2 m 4 stage. One input is coming from this Vi d by 2 minus V i d by 2, but the other, there is another input coming from here [FL] VG s [FL] m 4 [FL] input [FL] VGS 4 [FL] output [FL]. So, when I see output. Now I see I have two inputs; one at m 4, the other at m 1 m 2. So, I must now actually superpose the two, I must get the voltage due to the VGS 4, and also should get output due to VG s. I mean VG 2 or VG Vi divided 2. So, I need both sources to be now used in evaluating the V out that is the interesting part. Is that clear [FL], obvious [FL] is that clear to you, and why this this term which I am now showing, there are two sources for this output one is, if I will input here, if I give input here ok.

So, there are two transistors are receiving inputs now. So, what is the method I used, initially do not treat. This treat with this, next time treat this or output due to VGS 4, and output due to VG 2 or Vi d by 2. I will add them, superpose them to get my V out, this is the technique which all of us directly or indirectly used. So, I shown you how, from where this method has been chosen. Is that clear? If I do not connect this, this issue will never appear. Is that clear to you, but as I connected to make it single ended, the first time I realized that the output of the first stage is input to one of the transistors of the second stage. Is that clear, and that must be now taken care in solving is that. So, if I do that, which is what it is relevant for in my opinion. Now you can see what Raju was saying I am hiding.

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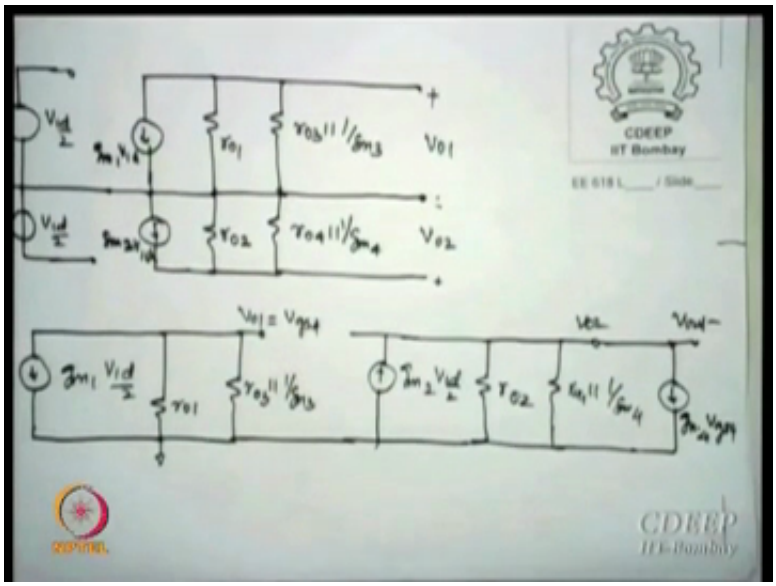

Since V o 1 is VGS 4 is that V o 1 is VGS 4. So, apart from the first m took a current the output [FL] gm 2 Vid by 2 sources [FL] what is the resistance. It is going to see r o 2 parallel [FL] ro portion r 1 upon m 4, but the same resistance is also getting additional voltage, because the output will still seem, it remains same, resistance will remain same, because resistor m 2 m 4 are still same, but then the additional current source sitting here which is, because of m 4 which is gm 4 into VGS 4. Is that clear? There is the additional current source which is gm 4 VGS 4, and there is one normally gm 2 VGS V in is already there.

So, now you have two currents, only interesting part there is ac wise both are a [FL], and that is why they are signals are current sources are shown opposite. Is that clear? This is the crux of DIFFAMP outputs. Is that clear? If I do not show this, then I am making a great error, this is the reason why you see against, as shown in the books, because, but as I say most books do not show this kind of equivalence. So, I thought maybe this is a high time that I show you that, from where they are getting those expressions is that mind cleared to you.

There is an transistor m 4 is also receiving ac input and m 2, you are actually putting an a c input, both contributes to the output of the second stage. They must be superposed the problem was that; one is pushing the, because of VGS is a p channel device, the other is n channel device. So, the direction is opposite. So, they are as, but one of them is minus

sign. So, probably they may still add physically in numbers. Is that ok. Last quickly we will finish up, maybe we will stop here, we will show you next time the gains. So, is that equivalent circuit? Please now remember this is the real equivalent circuit of a single stage DIFFAMP is that, this is the equivalent circuit of single stage DIFFAMP. Now calculation are very easy, output is here substitute back here in that and calculate, we all finally, which is done V out by VGS Vi d by 2 will get us or V i d will get us the difference scheme. Is that clear? So, next time.