CMOS Analog VLSI Design
Prof. A N Chandorkar
Department of Electrical Engineering
Indian Institute of Technology, Bombay

Lecture - 10
Types of MOSFET Amplifier

So let me now continue with the amplifiers, please remember one of the main features of analog design is an amplifier design; that is our major workhorse. So, we want to understand everything what an amplifier can do or how to get to the that spec. So, we have looked into common source, common gate, source followers, normal single stage amplifier, we looked into cos codes. We also have some interesting features about the how analog circuits are important in the current scenario; my first few lectures on PPT, so this is what all that we have so far covered. Today, we start with more details on that; the first thing we will like to know what kind of loads one should use, all this time I was using a resistive load which is essentially a actual register.

The problem with the actual resistor in a circuit; not that we will never put that, but essentially we avoid it. As I discussed earlier sometime, that the sheet resistance available for normal CMOS technology is not very high. So, we said that the load resistance of typically 40 K will be required.

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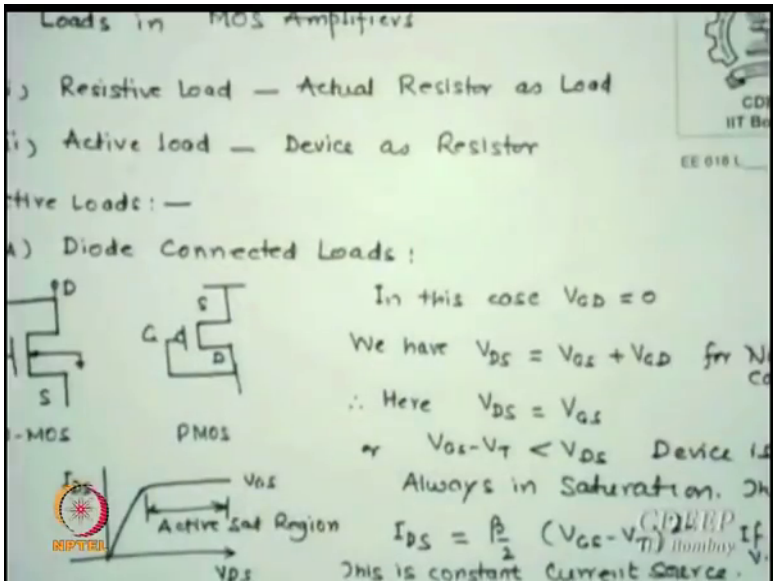

And for that values 10 to the 40 K; the aspect ratio is so high that it will be very very difficult to put more than few registers on chip; that mean it will take more area for resistor than the transistors. So, we said we will not like to use resistors as made out of normal semiconductor, please do not think that I will never use it; I will have to use somewhere I will, but normally I will avoid.

Now replacing a resistor by an transistor itself is called active load and therefore we are saying resistor is now replaced by the device which acts like a resistor. These are called active loads because transistor is an active device. So, one of the most commonly used load in almost all analog and also in digital is called diode connected load. Now what is this diode connection is; I think we are done many times earlier. So, I will not explain why name diode, but think of it there must be something you need to call diode.

In this case, for N channel the gate is; or for P channel gate is connected to the drain permanently. And then if you evaluate the resistance seen, you can see from yours IDS VDS characteristics, if the device remains in saturation throughout; in that case for a given VGS which is what is VGS here? VGD minus VS; VGS is how much? Because VGS connected to drain, VGS is VGD minus VS and if that remains always smaller than VDS or equal to VDS, the device will permanently remain in saturation.

And if it remains, this resistance of the characteristic shown here which has a very large R because of the slope is very low, this will can act like a resistor. The example whatever I said is given in the formulation PDS is VGS plus VGD; since VGD is made 0; VDS is always equal to VGS and therefore, VGS minus VT is always less than VDS and therefore, device is permanently in saturation. And the current characteristics can be written as beta by 2 VGS minus VT square; assuming lambda small. You wish put lambda you can; then you may say if the lambda is 0, then that should show infinite but assume the value is whatever derived.

And this x therefore, acts like a constant current source. So, sometimes it is also called current source loads, the diode connected loads are also sometimes called current source loads because this is the current source. It is only a function of given VGS and therefore, it is constant current source Now I will show you what is the importance for us a good current source that it should have a large.

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Parallel resistance to the current source, as if high as that is the better one, so we will evaluate for this case what is the impedance seen by this device as a load? And that is essentially is the feature, how good is the diode connected load will be? Is that ok for those who are written down now? So, if I wish to figure out R 0; I have put an equivalent circuit as I did earlier.

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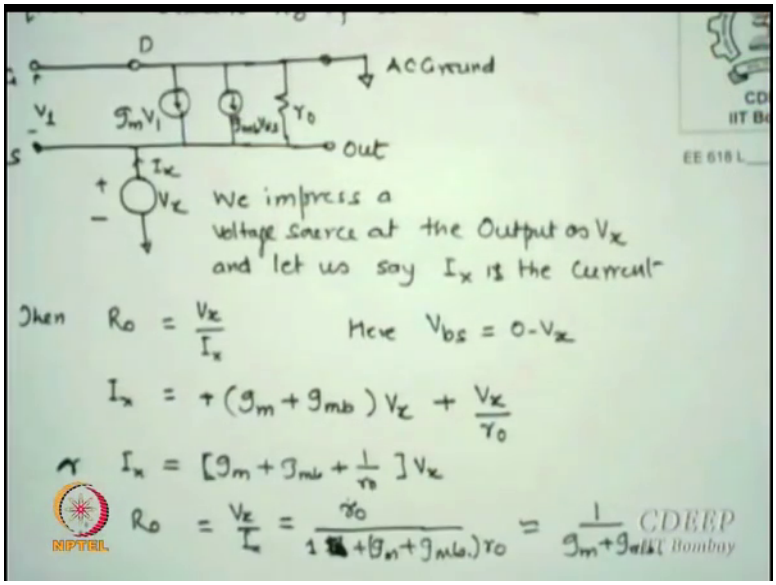

Please remember we say VG and VD are connected gate to drain. So, drain to gate; gate to drain is connected, you have V 1 across gate to source, gm; V 1 is the current source gm; VBB is the current source due to the body back buyers or the these resistance and this drain is also grounded now for AC; for VDD side. Now if you see and then I apply a source V x and find the current there and V x by x will be R 0.

Essentially, if we rewrite the current now; I x which is shown here in this directions, you can choose any direction do not worry sign should be taken care otherwise. This by the V x source are supplied, current leaving the source I used as plus I x going up. So, essentially this current and this current must balance because at this node the net voltage next current must sum to 0.

At source node, this current and some of these current must equal to 0. So, if I rewrite I x equal to gm plus gmb; V x plus V x by R 0 and then I write I x is gm; 1 upon R 0 V x, I get and if I say R 0 is very very large compared to 1 upon gms; R O; which is the resistance seen here for the top device that becomes 1 upon gm plus gmb. In case gmb is

also not given to you; many times I may say there is no back gate bias and in that case, it is only 1 upon gm. Please remember, there is R 0 is sitting there; essentially R 0 is a cross 1 upon gm and whichever is smaller, we will take care since 1 upon gm will be smaller compared to R 0. So, one can say typically diode connected loads gives you a resistance of 1 upon gm and not R 0 as we thought; that is the issue which I wanted to raise; is that point clear?

The resistance seen by the lower device as a load is just 1 upon gm; under diode connections; is that correct? Is that clear? Now, this is an issue whether this is good enough or not is what designers should know; if your gm's are very very low; yes this R O can be as high as possible, alternatively when gms are low; when is the gm low for a normal device?

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Either the current is flowing is low; which may be good in at time for what purpose? Low power, a current is reduced or the W by L is smaller. So, the smallest size transistors if you use, your resistance can be built. Please remember, normally the channel length which you can create is normally a technology parameter; to reduce W by L all that you said do not use the minimum channels, use multiple channel links.

That is if you are working on 90 nanometers; typical channel length is around 60 nanometers. So, you put 120 nanometers as length; instead of L put, instead of 60 you put 120 there; that you can always saw, you cannot go below 60; you can always. So, W cannot be go below 60, so do not increase decrease w, but increase the lengths, whenever you need this.

This is also true in the case of lambda, when we say if you reduce lambda is lambda dash by L and you want to reduce lambda; that is the bias parameter then what do you do? Increase lengths as much as possible. So larger the lengths, smaller is lambda and better is the current source you get. So, that is similar feature is also appearing in this analysis; is that correct? So longer length device is good for good analogs blocks; however, what is the problem? Larger the lengths you put, the size of transistor will be enhance W into 12; which means area penalty you are paying.

Something else I did not say, you will also figure it out the capacitance will vary because of the area variations. So, somewhere bandwidth may also get affected, how much? We will see when we go to frequency response. So, there are issues; so, it is not that you just push it or just reduce it, for a given design you must choose what else you should use? What is possibility available? Otherwise do not use diode connected loads, if that is hurting you so much. Is that clear?

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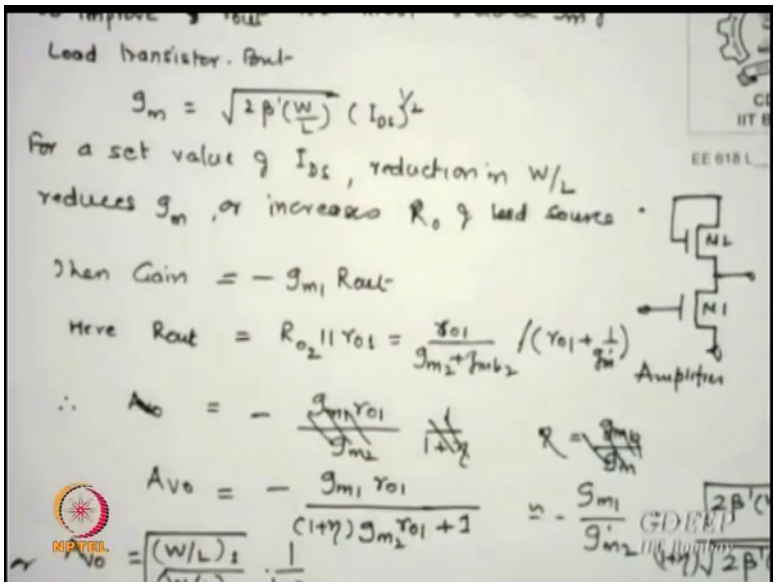

If you look at the gain of an amplifier, which has this diode connected; same thing which I stated is given here, do not rewrite I already said gm is proportioned to W by L and IDS root of IDS; and that is what I say will increase lengths. The gain is gm 1; R O, if R O is the risk; of course, it is also shunted by R O 1 of the driver. Since if R O 2 is smaller than R O 1, then it is only R O 2; if not then you have to figure it out how much it should be parallel curve. So, put parallel and whichever terms is smaller will take care.

So, if I substitute this gm 1 into this into, this figure; I get on and roughly I will say A V 0 is W by L by 1 by W by L 2; divided by 1 plus eta; if eta you do not want to keep, put it 0; you may also use eta 0, if many cases. So, what is this kind of amplifier is suggesting? That by just make a ratio of W by L of the load transistor to the W by L of the driver transistor and you can adjust your gain without any other parameter in question.

So, if you are looking for something constant or variable which should not affect your A V 0 then this is an ideal situation; just sizing. And please remember individual size is not

relevant, the ratio is relevant. So, you can adjust individual sizes to suit something else but still make a ratio of required current gain or voltage gains; that is the strength of diode connected loads for an amplifier.

So, choice is not that you should use or you should not use; choice is when to use? You should be aware of; is that point clear why I showed you that connected loads? Because one wants to know that just by adjusting the ratio, I have a control on the gain itself; am I clear of what I am saying? So, this is something very interesting designs because if I do not have to worry too much about VT's, I do not worry about VDD; if everything is as long as device in saturation, thank you very much; the ratio will take care of my gains and remember to ratio is independent of what?

Temperature, environment any other things and therefore we say just by design parameter; I am controlling the gain and which is the design parameter? Which is on the plan of the wafer or which is the surface area which I am controlling. Nothing to do with in the wafer inside; that something great happens. So, it is inaccurate because we assumed few things, but to a great extent this is reasonable assumptions. So, what is the way I will say when I say I want to design a amplifier of a gain of 1000; I will never say 1000, I will say the minimum gain expected is 1000.

So, this adjustment is still within your hand you will say as long as it is not lower than 1000; any other parameters you wish to control you, you have right to control. Normally gains are never specified 976; kind of thing, there is nothing such things. So, as I say we can also use amplifiers; other loads also, the other loads could be what I said other day?

Just by putting an N channel transistor and biasing it; that means, if this transistor is biased heavily by me such that VGS is minus VT is always greater than VDS. So, transistor will remain in non saturations or linear mode; is a smaller resistance and the value how will I adjust that value? By W by L.

So, again by using a W by L and keeping VGS minus VT larger than VDS for the load device, I can control my smaller value of resistances.

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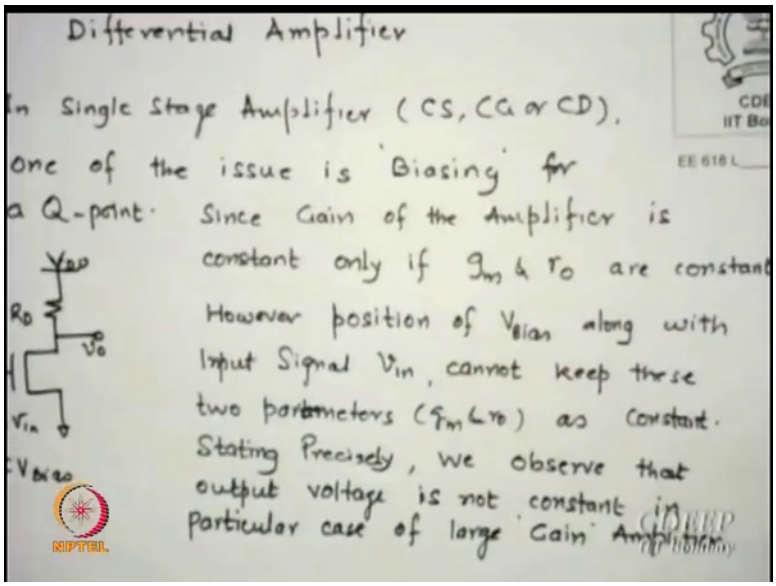

So, next we move to the most important amplifier; which is almost used I will not say excluding to other three, but most times we will use this amplifier for all amplification purposes in analog is a differential amplifier. Now this word is slightly worrisome to me, there are words in the books called difference amplifier. There are words is called fully differential amplifiers, so we should be slightly worried about these statements; right now the difference amplifier and differential amplifier here is the same.

So, if I say diffamp or difference amplifier a differential amplifier I mean the same, but later on in some design I will say it is a fully differential system. So, I will define what I meant then; till then assume that difference amplifier, differential amplifier or a diffamp is same. Now what is the problem in common source, common gate or common drain amplifier? One of the major issue of which we did not discuss very often in earlier designs is, we know that their properties strongly depend on the Q-point, where do you put your biasing?

Now biasing seems to be trivial to many just apply bias and you get it, it does not happen so easily. For example, if I put a V bias in series to the signal, it is going to bias this transistor; keep it wherever you wish, see these non; whichever way and this should work, but this is not working, the way we thought it should.

Since gain of an amplifier is constant only and only if gm and R 0's are constant; however, the value of V bias and the signal over reading on that bias this amplitude of

this; where do bias and how much is the signal sitting on this on a real characteristics may push your device from different R 0 values and therefore, sometimes different gm magnets; which essentially means both the parameters of gm and R 0 are strong functions of not only V bias, but what is the amplitude of the signal and where it is biased?

So, our assumption that the gain is constant; it is not very true because it is now a function of input which is never we wanted because if that happens, the gains will be different at different input sides. Particularly, if this may happen when the gains are extremely high, swings are too high and that time these assumptions are not very good. And therefore, we may worry about how to get good biasing; what is the condition I am saying? That biasing should not influence the outputs; is that clear? That is what I ideally I will like so that I get good current voltage gains.

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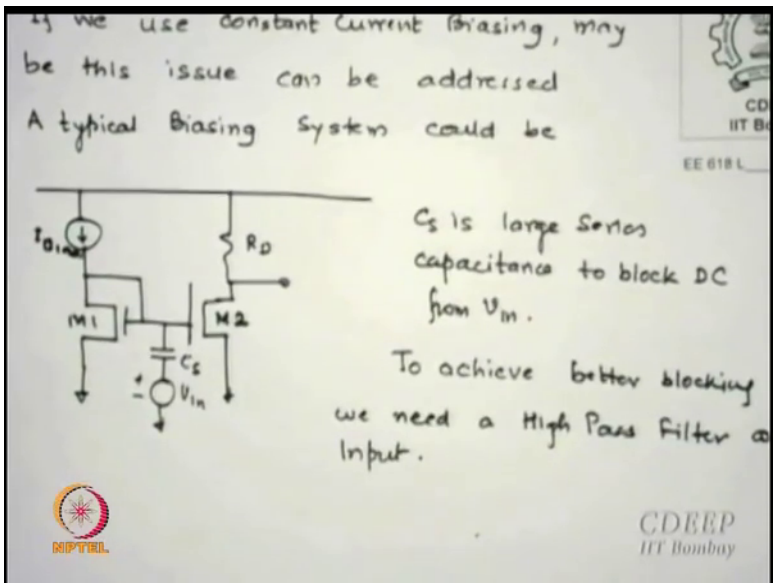

Yes if we use constant current biasing maybe this issue can be addressed, a typical biasing system can be something like this. This is I bias; which is flowing through this transistor and its drain is connected to the gate like a diode essentially, but the same gate is connected to the actual amplifier which you want to bias; this is the precursor of the mirror that is the idea behind mirrors.

Now what we do is; the way we kept these two transistors are identical, their gates are common, their sources are common. So, what is equal for both of them? VGS is equal to;

VGS M or let us say M 1, so VGS for M 1 is same as VGS for M 2. Now, you want to put input signal; so you must put through V In. Now you have to put this value, why you have to put this C? Because you have to isolate AC from DC, I put a series capacitance to the source, which is CS; however, if this capacitance is only left there; it is like an impedance at certain frequencies.

What is my idea is that for a DC at least it should pass everything, all frequencies should it pass. So instead of just CS, I must create, convert it into some kind of a high pass filter whose cut off is very close to 0; little higher than DC, but so where should I put a resistor? And since there is no gate currents, what does that mean? Any resistance will not change any drops across because there is no current in the gate side; is that clear? Because gate is isolated from in by installations.

So, if I use this circuit and convert it slightly modified way; so, what he said and I agreed with him that; I can use current biasing and I can have independent of my actual transistor, I put left side my bias circuit that is what every analog designers will find; that it be biasing block. Of course, that is what learned separately; how to create references both for current references as well as voltage references, which will make this constant.

So, that is another part we should look; so, with that circuit then this whole circuit will be called biasing circuit. Now I am showing you very careful all this is now required and what we call a normal digital hardware, which is called DC to DC converters using constant biasing sources or constant current sources. This is called biasing module now you have to create, to create 1 volt, 1.2 volt, 1.5; there 5 many voltages you need on the digital these days. So, this is one of the way this can be created; change the sizes and you have different values.

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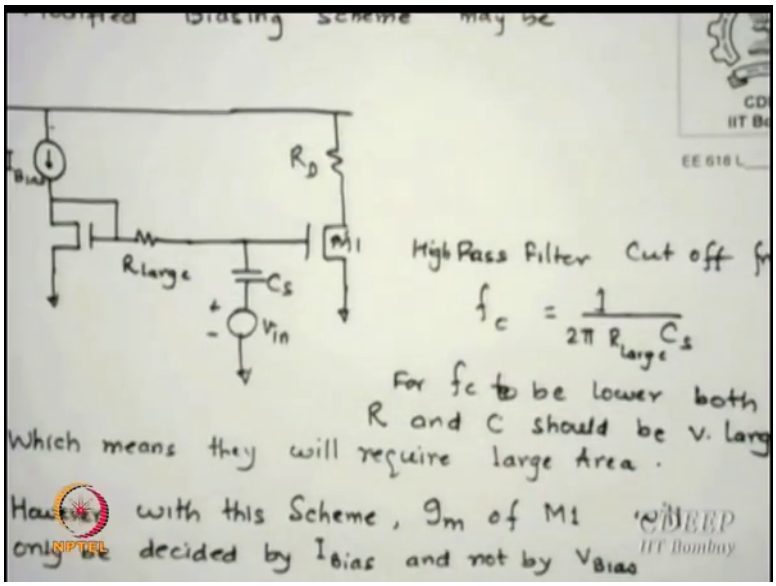

So, I said ok I put a larger resistance this, then this is essentially high pass filter and this has a cut off frequency upon 2 pi R large CS and we want this to be as low as possible good high pass filter.

This means R and C should be very high; now what is the problem with R and C higher both are functions of lengths and widths and you make on its silicon they will be functions of W and else; whatever size you keep there for them. Larger means larger area you are picking up anyway, so you can do; this is a good way of doing it, but it has the feature that it actually increases the addition, it requires additional area to implement; this will do your job guarantee .

Please remember, this is the scheme which we do employ in an RF amp of course, is not going to talk of RF systems, but if I had to; then I say this one of the very common biasing techniques, in the case of RF. So, if you are designing a power amplifier or a low noise amplifier in RF range; probably you may look back and see this was one method I used there in those designs.

So please remember in this scheme, I bias is going to decide the gm of M 2 or whatever nearly my M 1. And therefore, it is independent of B bias; whatever comes here I am not worried, it is only I which is going to decide the gm. So, I have avoided that V bias dependence by making a constant current source there. [FL] biasing [FL] even if

variations occur and if it does not still change anything, then why should we worry so much about it?

And that is what exactly the differential amplifier does, why this was a precursor sheets to show you why differential amplifiers became; apart from many other advantages of different which is making so important. One of the reason was that the biasing became very trivial in the case of different amplifier.

Because even if it is not constant, it takes care of it and that is some fun part in that the differential amplifier gains are normally very stable gains and that is why we prefer differential amplifiers. Apart from many other features which we shall now discuss, the differential amplifier is far superior in many characteristics; over single stage amplifiers, but then why this single stage amplifiers are sitting at all? This in issue you should answer.

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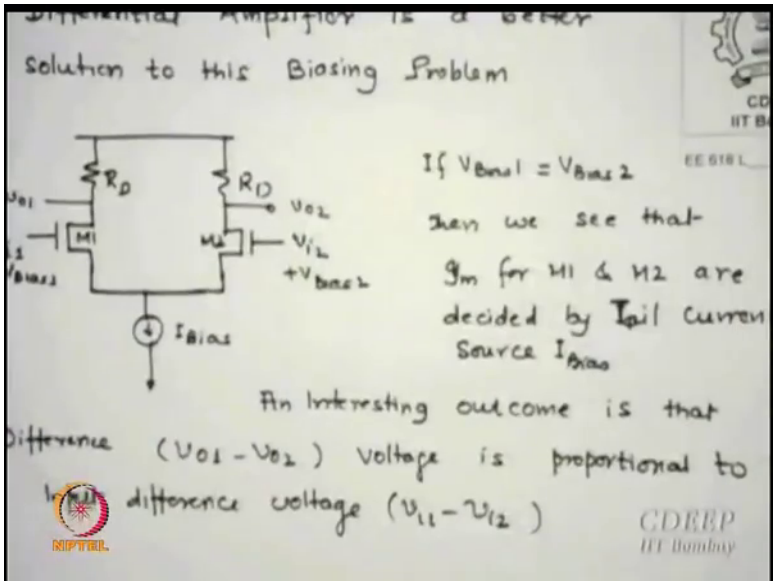

So, you I just want to tell you very clearly; a differential amplifier is a better solution to this biasing problem compared to what I showed for single stage. Let us say I have an input V I; what is the differential amplifier? You have two transistors; M 1 and M 2 which sources are connected and given a common bias current source.

Now, there is also case the same different loads and current sources activate; I can use one of them to create this right now. Right now my assumption is I bias is ideal, but in

real life I bias may not be ideal source. So, what it may give some resistance, so what it will affect us, but as of now for simplicity we start with thing its good thing. Then we have a load RD, they can be R D 1 and R D 2 and they can be same, so it is not a compulsion that they should have same loads. So, we say the gm of both these transistors are decided, but this is sometimes called bias current or tail currents. Some book call it tail, some book will called bias; so, whichever books or book or none whichever you are take it; either it is called tail current or it is called bias current.

So, since this only decide the gm in this; an interesting outcome of this difference is that the difference of output voltage is now only proportional to the difference of input voltage. I repeat the AC part is if I show you VO 1 minus VO 2 is only decided by VI 1 minus VI 2 and nothing else. So, there is no way if this changes; still it will give the difference of that.

What will happen if there is this? Both will get affected and in difference, they may not be available because difference will get cancelled out; this is the idea. So, if the first problem of bias variations or bias dependent variations at the output can be eliminated, if you have, if variation occurs; it should occur together and the difference will cancel it out.

So, this was the one reason as I repeatedly saying this is not the only reason, this was one such a reason why diffamp was preferred. Because they say, this bias issues are partly taken care by. So, even if this is not does not matter; I am not very much worried on that of course, if it changes so much that device goes from saturation to; then I am worried otherwise; swings are not of my interest.

The another part, which all of you are aware for this diffamp of course, is since I said so difference anything which assuming that the any noise is universal and whatever additional noise voltage appears here will also appear here, then VI 1 plus V noise; VI 2 plus V noise and if I have to take a difference; I had leave the noise part anyway.

So, anything the word now which we later come is common mode; which is common to both will get anyway eliminated at the output. So, thus major reason why diffamp was used; that it allows you to remove the noise commonly mode noise from the any circuit. The assumption of course, says in a small area of diffamps; the noise pickups are similar.

Before we go maybe I have another few things; of the another interesting feature as I said first was the bias, the second was the noise; common mode noise as we called.

There were something third which common mode systems, which rejection it occurs the word is that is why there is the famous term we used for diffamps; as common mode rejection ratio; CMRR that is exactly is the baser for that; how much rejection it will do? Ideally it should be infinite, it should in a common mode gain should be 0's preferably, but it will not be. So, there will be some large they show we come which is good enough to say effect of that is very small.

So, the third and very important feature; which, is that ok? Which is not I think; I did not think earlier, but just now I remembered; particularly this is for the people who are working on digital or big signals, there is a huge issue right now going on, where is your digital course right now VLSI design. There are issue or maybe system design courses in next semester? So, one of the issue there we figured out; we have one interconnect and a signal is entering from here.

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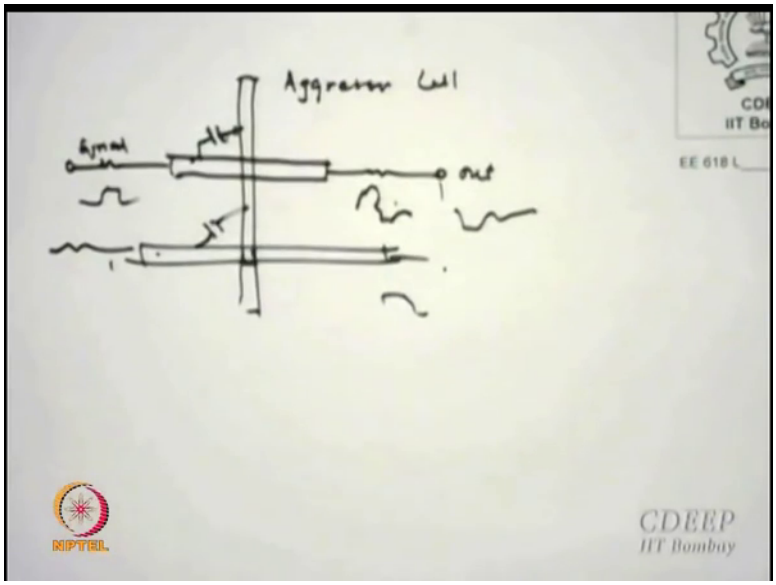

This is your out, through a interconnect; this is your signalling problem which is very important. And let us say there is another V interconnect which is a cross, which is called and this in our terminology there is called a aggressor cell or aggressor cell interconnect.

Now, if you have two such interconnect lines close by; not necessarily orthogonal, but even parallel. There is a capacitance which is associated between the two lines, now since there is a capacitance associated with two lines. So, if whatever signal you are going to put; depending on this coupling it goes, the voltage here may actually be something like this or sometimes like this. Your data transmission will be actually impaired heavily and if they are more than two aggressor lines, it may actually hit you worst; further there is also an issue if the data is flowing in this direction or flowing in this direction in aggressor that may also change the output patterns.

Ideally, I do not want this to influence; so what I say it if you have an aggressor here; I have another interconnect line, I have same signals going to both this and the output I will take the difference of the output as well; is that clear? So, now, whatever change is occurring between these two lines it will get eliminated because of the difference outputs with the difference inputs. So, in aggressor cell effects can be nullified equivalently by putting another parallel, another line for it; penalty is huge area you put it actually, but system people will tell you it is better to have larger area chip than not working chip.

So this is an issue which there we solve by different; this is a crosstalk issue, there are number of ways we try it and this also increases the power dissipation. So, for a low power this is one of the issue; how to reduce the power actually? So, there are issues which digital people are looking into and there also we will preferred difference outputs or difference inputs to in difference input. So, it is not really is a connected to diffamp word, but trying to show you that where these different schemes actually are useful; is that point clear? So, please take it these are the issues which are cross connected to digital.

So, as I said diffamp has advantage that it will do common mode rejections it possible and it will solve much of the biasing issue. In addition to that if it does something more, that is a bonus for me; if it does not do it at least gives gain of a commonly one single stage is fair enough, but if it does even better; which I think I will, then I have got much more value out of the same system. And that is why diffamps are most popular amplifiers, before we go to the small signal analysis; it intuitively one must think about the large signal behaviour. Large signal means only DC values are used there, AC's are small you can add to that if you wish, but basically we are looking for DC analysis.

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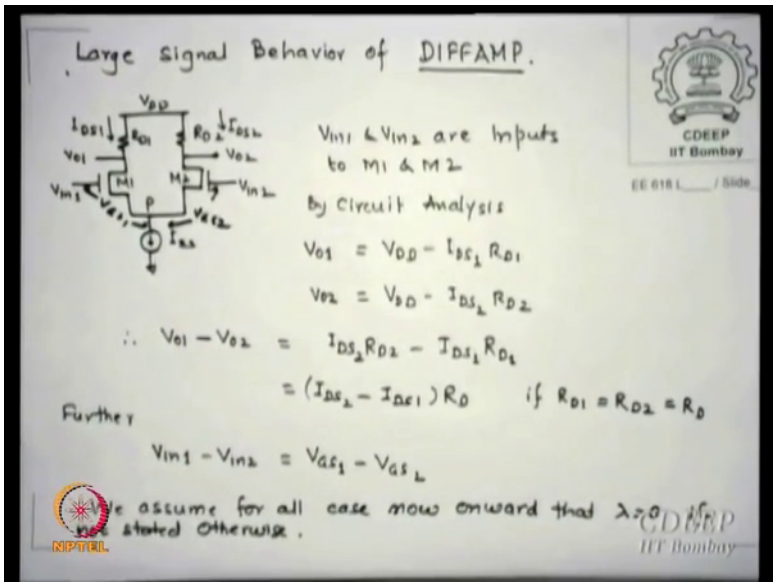

So let us say you have a differential amplifier with two transistor M 1 and M 2, which is biased by ISS, this word I change from I bias to ISS because this is what reserve is says. So, I thought at least if you go and read once at least you should not feel very thoroughly different. So, I first I wrote bias then I realized opened the book, what Taylor Current he says IS, so I changed to ISS; does not matter, you can use any now.

V M 1 and V M 2 are the inputs and the most important worry and most important point, which we want to discuss through this is this point P, which is common point for sources of both M 1 and M 2. Now figure it out this; if per say this voltage at P changes; VGS of this and VGS of this may not be same; is that correct? But does that really affects you? If it does not or does it change at all.

We like to see by this system whether the P point is stable that is why this large signal analysis. What is the VO 1 will be? VDD minus IDS 1 times; RD 1, VO 2 will be VDD minus drop across RD 2, I subtract VO 1 minus, this is difference output voltage; VO 1 minus VO 2 and if I subtract here, it is IDS 2 minus IDS 1; RD 1 or IDS 2 minus ID 1 into RD; assuming RD's are same. Further, if you look at the input side; this is VGS, so we say V in 1 minus V in 2; what is essentially the value V in 1 is equal to VGS plus drop across current source if any; is that correct? But that is common for both sides I do not take care other I say V in 1 minus V in 2 is subtraction of VGS 1 minus VGS 2.

For the simplicity, lambda is taken 0 for all analysis till stated otherwise; is that ok? Please remember lambda can be taken care; all that will happen is you know non-linear terms will start occurring in under routes and squares. And then analytical solutions will not be very easy to understand, we are not really designing on them; what we are using it to explain something. And since lambda is anyway 0.01 or 0.04 or 5 kind of things; it will not drastically change the physics anywhere; however, physically please do not leave lambda as 0, if you are calculating R 0 because otherwise that are 0 may becomes infinite and gains will infinite .

So, do not think that I am leaving lambda, but for explanation of voltages I do not believe it is very much important; is that ok? Is that expressions ok? We wrote V in 1 minus V in 2 as VGS 1 minus, VGS 2 and V O 1 minus V O two is IDS 2 minus IDS 1 times RD; if RD 1 equal to, RD 2 equal to RD; is that ok everyone?

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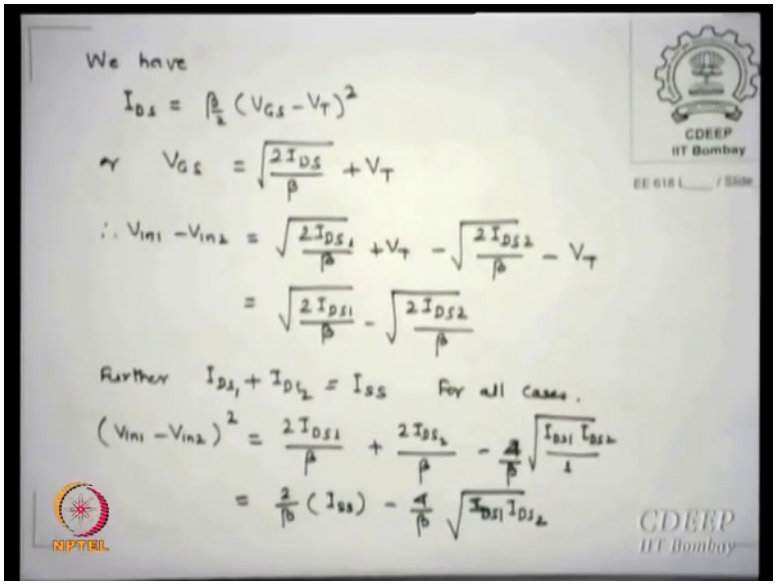


So, now we have; we write the drain current as beta by 2; VGS minus VT. So, we can also write VGS as under root of 2 IDS by beta, also we are used alpha equal to 1 in all this analysis. As I say unless stated otherwise use alpha 1; lambda 0, otherwise if given or even eta equal to 0 unless stated otherwise. So, VGS is for the large signal these do not matter; so, we do not add that much; small signal, I may add all those term because small signal, they will actually affect.

So, VGS is 2 IDS by beta plus VT; so, if I want to write V in 1 minus V in 2; then it is VGS; VT minus this which is essentially I write two terms for IDS V in 1 and V in 2; which is equal to 2 IDS; 1 beta minus 2 IDS, 2 over beta. Do you get the point? IDS 1 and IDS 2 appeared in output; so, I now replaced input also in terms of IDS 1 and IDS 2; is that point clear why I did this?

Now output was a function of IDS 1, IDS 2. So, I say input is also in a way explainable through IDS 1 and IDS 2. One important feature of diffamp is; which is very important if you write down till, you first write down only up to this and then I will come back and show figure and come back to this. Is that ok? This much you are written; above?

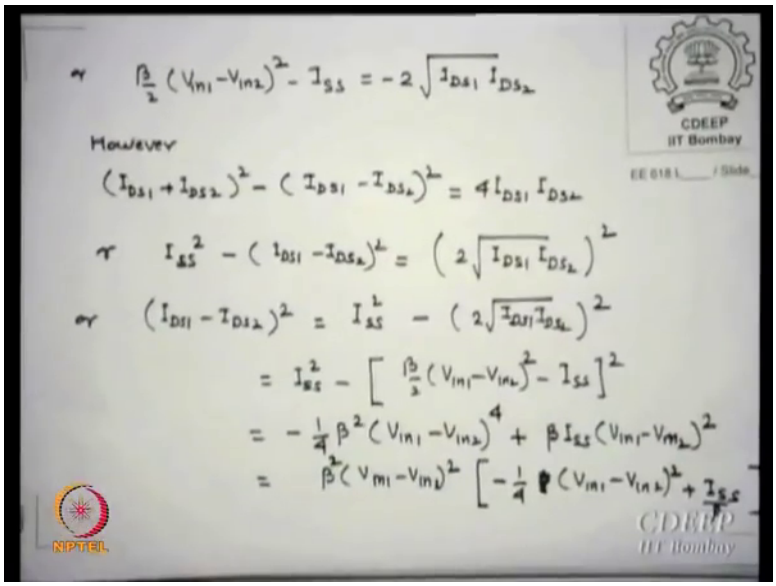
So, if we see the figure here the drain current of M 1 and drain current of M 2 can only sink through the current source. Which means whatever value of IDS 1 and IDS 2; the sum should be always equal to the ISS; so, this is the major feature of a diffamp. It may happen this may be larger, this may be smaller or this may be larger, this may be smaller or they may be equal; in any case the sum total will be always equal to ISS and that is the feature of a diffamp.

So, since for all cases IDS 1 equal to IDS 1 plus IDS; we now rewrite V in 1 minus V into square is square of this square of this minus two times this; multiply if you take it a 4 by beta; IDS 1, IDS 2, then we say IDS 1 plus IDS 2 is ISS. So, 2 by beta ISS minus 4 by beta under root of IDS 1; into IDS 2 [FL] mathematics [FL], but just I want to show at the end of the day what should be the limit of V in 1 minus V in 2; corresponding to which IDS 1, IDS 2 should be available to us.

Before I go ahead, maybe physically still I will tell you what I am trying to tell you. So, that this whole expression which I derive behaviour; is that ok you are written down these three lines? What I am trying to say you is the difference of these two currents; IDS 1 and IDS 2 is a function of difference in V in 1, V in 2, but if say V in 1 is equal to V in 2; then we believe that IDS 1, minus IDS 2 must be 0; they must be equal.

And if that occurs, we can say each current is half because IDS 1 must be equal to IDS 2 equal to ISS means? Each R must flow. So, if the inputs are same; we want to see or difference of input is 0; then the each on will get 50 percent of ISS; that is what we want to prove, which is anywhere visible from here, but mathematically maybe I will show you that it does come finally, after huge equation solving.

(Refer Slide Time: 41:42)



So, we say expressing that beta by 2; V 1 minus V 2 minus ISS is minus 2; IDS 1, IDS 2; under root of that; however, mathematically IDS 1 plus IDS 2 square; minus IDS 1 minus IDS 2 square they [FL] expand [FL].

4 IDS 1, IDS 2 [FL] minus [FL] so, [FL]. So, 4 IDS 1, IDS 2 is nothing but subtraction of these two, but what is this term? ISS square. So, we write ISS square minus IDS 1 minus IDS 2 square is 2 under root IDS 2 whole square. Therefore, this term IDS 1, IDS 2 square is ISS square minus 2 IDS square, but this term is how much? From here, beta by 2; V in 1 minus, V in 2 square minus ISS [FL] term [FL] I use this term in substituting here [FL] 2 IDS 1, IDS 2 [FL] beta minus V in 1 [FL] term [FL] expand [FL] that is what I was also thinking why I am doing this; I want to show that V in 1 minus V in 2; plus minus [FL].

So, up to what value of V in 1, minus V in 2 which currents both will flow or one of them will flow, from onwards where the other current will down. So, I say if IDS to start going down or IDS 1 start going down or IDS 1 becomes maximum; that figure I have to draw; is that ok? So, I want to plot IDS 2, IDS 1 against delta V in which can be plus or minus; why minus because if V in 1 is higher or lower than V in 2; it can be plus minus.

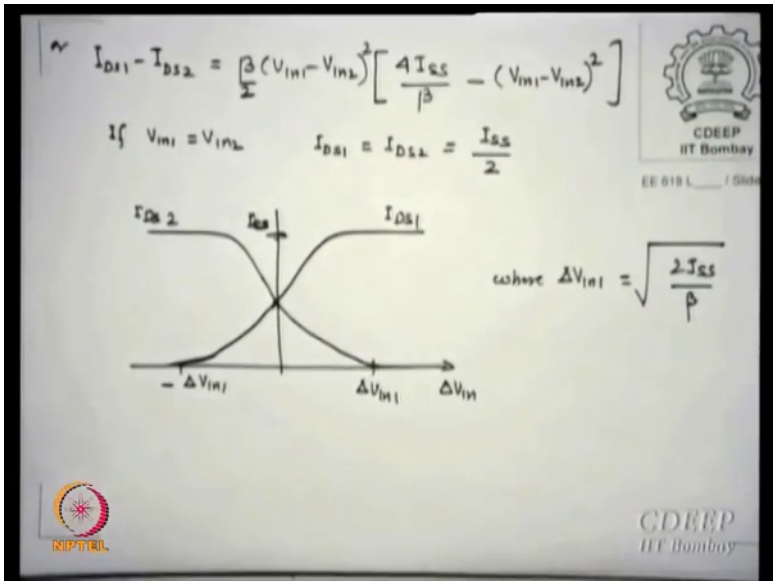
Physically I already said if V in 1 minus, you are written down this expression? You write down; I will come back to maths or physics again very trivial thing I am rewriting,

but I want to show mathematically derivable things, which you can otherwise also understand.

So, what I was saying you is this figure if you see again; basically what I am saying if VGS 1 is or V in 1 is much larger than V in 2; this will draw a larger current is that correct? Larger this current means smaller this current because ISS is fixed; so if this draws more current, the other will go down. If this is larger; that is delta V in is minus now; difference if this is larger, this will draw larger current, this will draw a smaller current.

After a while when this transistor does not have enough VT support, all the current will either flow here or flow here; is that correct? So, at certain value of delta V in, beyond that only one of the transistor will remain turn on and because of that all of ISS will flow through M 1 or M 2; is that clear to you? This is what physically visible.

(Refer Slide Time: 45:16)



So, after all that equation you can rewrite; this becomes IDS 1, IDS 2 is beta by 2; V in 1 minus V into square V 4 ISS by beta minus V in 1 minus V in 2 square. And V in 1 minus V in 2 is essentially delta V in; difference of the 2. So, if difference of the two V in 1 is equal to V in 2; IDS 1 minus IDS 2 is 0; first write the expression, which I said physically is visible now.

If V in 1 is equal to V in 2; that is delta V in is 0, IDS 1 is equal to IDS 2, but IDS 1 plus IDS 2 is ISS; each arm will take 50 percent of the ISS; so if both inputs are same then 50 percent current. In case this is larger delta V in is positive, this term will subtract from this and if you keep increasing plus delta V in; after a while, this term will start mathematically reducing and you can say or rather difference.

So, IDS 1 will almost become ISS this value is typically ISS; this was therefore, ISS by 2. So, as delta V in starts increasing, IDS 2 start falling and IDS 1 start increasing because that is the expression is asking me, as I increase bit beyond, the other (Refer Time: 47:02); it turns off and all of the current goes to IDS 1, by same logic if I do the opposite side symmetry being tails; IDS 2 will reach ISS and IDS 1 will become 0.

This fact that difference amplifier essentially allows current switching from one arm to the other, when the input changes beyond delta V in of this value will 2 ISS by beta, then we may say; it is either drawn current here or drawn current. So, as long as you remain between these ranges; you have some sort of IDS 1 and IDS 2 available; which is where difference should work; is that clear to you? So, what is the signal available to you to move out? Is only 2 delta V in; is that correct?

But the catch word there is; if you have an input V in, between two V in 1 minus V in 2. If I increase one by the same amount if I decrease the second then the change is double; is that point clear? If I say V in 1; plus delta V in; so the V in 2, minus delta V in, is that clear? So, the difference is now essentially to delta V in. So, you switch over from one to the other, is that point clear? That essentially the feature of a diffamp, is that point clear?

So, why I showed you all the math rather we did is to prove this point that device switches over from and in these two ranges, device is operating or as at both device are operating and therefore, certain amount of difference outputs can be obtained; is that clear? Now this interesting understanding is only to make point clear, it is not solution for anything, this is just to say what happens in diffamp.

So, this is called principle of diffamp operation; this only tells this that switchover occurs from one to the other. So, now we will like to prove later that if this V P point shifts or does it shift? If shift does it get troubles us and if it does not; why it does not shifts. If it does not shift; all this analysis will be valid because VGS, VGS I will see is same all the time.

This ISS bias it was two equal; both side will go only if VGS 1 is equal to VGS 2; is that clear? Now this fact S remaining same; will IDS 1 IDS 2 will also remain same, if not then I have to figure out because VGS changes IDS 1, IDS 2 will vary, but I feel I do not think IDS 1 vary because VO 1, VO 2 remain constant we observed . So, I want to say V P does not change; now to prove this point and to do a one method of analyzing in diffamp; why we are looking so much in diff amp?

Please remember differential amplifier is not independently used for all the application; most the time, it will be part of first input stage of op amp; that is the input stage of an op amp. So, we will see that that is the op amp part, so we will see output amplifiers separately.

Student: (Refer Time: 50:34).

We will see shifter, I already say it can be done.

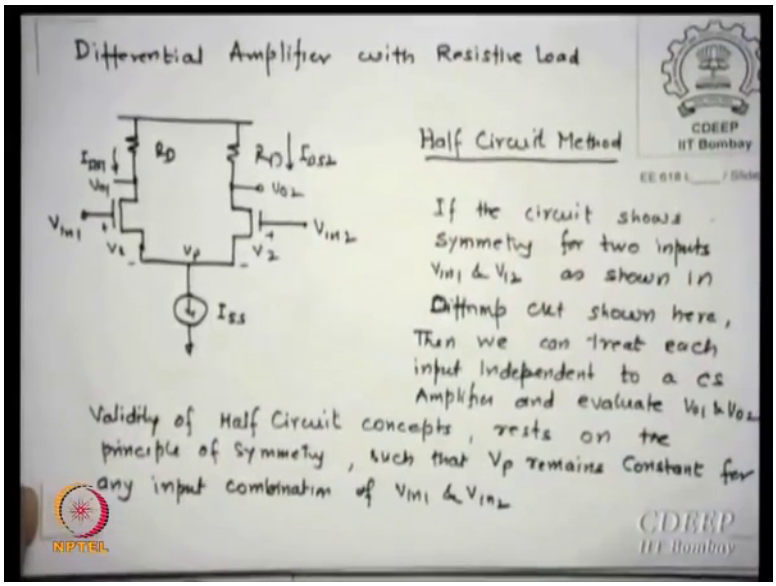
Student: (Refer Time: 50:37).

And if I see diffamp then I know now I can control my op amp characteristic because I know all three of them; that is the trick I am using; at the end of the day my interest is in designing a op amp. If I can design an open for a given spec, I have done almost 90 percent of analog efforts, 90 percent of analog systems will use at least op amp or valiant op amp. What is valiant? There are low noise op amps, low swing op amps, high swing op amps or oth; they are all basically.

Student: Pp (Refer Time: 51:12).

Op amps, so we will see that if I understand my diffamp well and the others two stages then I have controlled my op amp design and if I can do op amp for requirements like comparator it is also an op amp; switch capacitor filter also requires an op amp. So, name any analog system basic component is op amp; the biasing of diff amp is will take care which is useful for everywhere. So, we will also look into biasing circuits using constant current sources, constant current mirrors or constants reference voltages; how to do them, so these are some things which we are looking for.

(Refer Slide Time: 51:59)



There is a very interesting method which one can; one gives little interesting thought and therefore, this has been shown; it is called half circuit method. It essentially says that if your system is differential, what does the differential definition is? I repeat what is the differential definition I have? That if one input changes by plus value, the other input must go minus of that by same value; is that clear? That is called differential system, is that clear to you? V in plus delta V in; V in 2 minus delta V in; is that correct?

The swing has to be same plus and the other should correspondingly decrease. So, that V in 1 minus V in 2 should remain similar; now this fact is called differential circuit. So, if you have a differential circuit which is driven by a constant current source as shown here and it shows along this vertical line, symmetry on left and right Symmetry, the word is symmetry for the two inputs; then we can treat each arm independently.

And if you can treat this independently then it becomes single stage amplifier and then we can see the net effect together and figure out what is voltage here? What is voltage here? And then subtract and the ratio of VO 1 minus VO 2 by V 1 minus V 2; always can be found, so this is the technique which is called half.

So, what is the criteria I said? Each the system has to be differential, biased by common source, common current source or common bias technique; whichever you do and its symmetric for both inputs then the half circuit method is valid that correct is valid.

Student: (Refer Time: 54:07).

This is only names for left side is identical to right side as far as the circuit sheets; V in 2, RD 2 may be different, but on the right circuit is identical to say you may put values, but they are still symmetric. If I have mirror of this, this will come the same in that case; so it is symmetric to the source bias [FL] side case [FL] same [FL] so it is symmetric. Ideal symmetry will be when these are equal and these are also equal, but then that ISS bias 2; that we already checked is, but we like to see if even if they are not equal. As long as that any signal goes higher, the other must correspondingly reduced by same amount at the input done system will remain symmetric and we may say this is half circuit method is valid.

This is; of course we have a this is called half circuit lemma, which is given in a book maybe if time permitting will prove today. In that case, we say VP will remain constant for any input combinations; this remains constant and if this remains constant VGS always remains constant for both VGS 1; may be not be same as VGS 2, but VGS 1 and VGS 2; S is always same potential. If that occurs all our earlier theory is valid and therefore, we will prove this using this technique that VP is independent.

Please remember any input combination V in 1, V in 2 essentially still is differential in nature; change in V in 1 is opposite change in V in 2; that differentials part is most important in having half circuit technique valid, if it is not a differential system; this whole concept is not valid.

Student: Sir majority (Refer Time: 56:10).

Majority of differential systems will be always differential ok.

Student: (Refer Time: 56:16) differential what kind of (Refer Time: 56:20).

Student: [FL] (Refer Time: 56:22).

If; I can always go from single stage or single input stage to a different converters.

Student: (Refer Time: 56:29), but I am using a differential stage (Refer Time: 56:33).

If you see an op amp; the way it is done is one of the reference you create independent of that like you put something else and then outputs are picked up at the both ends.

Student: (Refer Time: 56:49) minimum (Refer Time: 56:50).

But that is essentially equivalent saying half here and half here minus; if I have, anyway that will come if total is something this, I can say half is a ascribe plus and minus half is ascribed here; which is difference is same that this is what automatic it will become difference.

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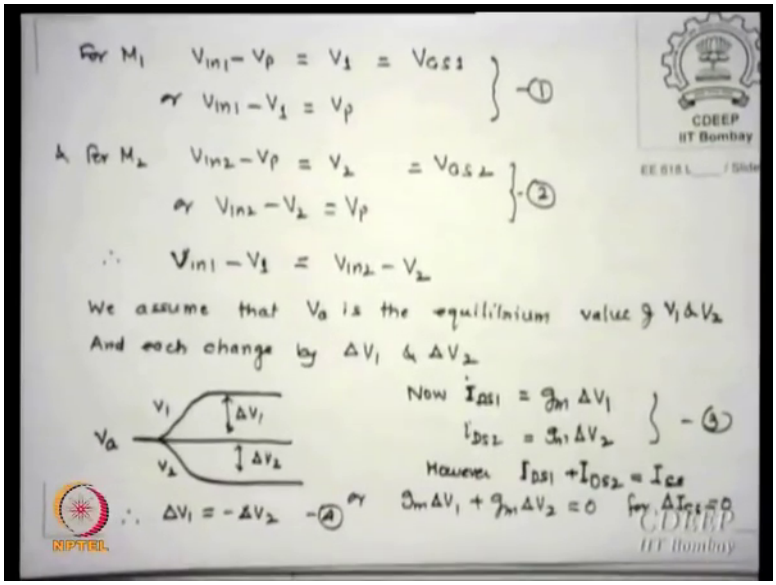

Few sheets and then we will stop maybe today; for M 1 please have your figure in front of you, I repeat this figure you should have it because you have on the sheet. So, you do not you look at that; V in 1 minus V P, let us say VGS is defined as VS; V 1 and V 2.

So, V in 1 minus VP is V 1, which is nothing but VGS 1 and therefore, V in 1 minus V in is V P; is that correct? VGS, this is VGS which is V 1, which is V in 1 minus V P, Is Raj clear? V in 1 minus V P is VGS for the transistor. So, I then I say; V in 1 minus V 1 is V P, for the second transistor by same argument I say V in 2 minus V 2 is V P. So, V since both are V P's, V in 1 minus V 1 is V in 2 minus V 2. Now let us assume that V A is the equilibrium value of V 1 and V 2; that differential were now coming and each change by delta V 1 and delta V 2; delta V 1 of this must be equal to minus delta V 2 down; is that clear? This is an average value.

So, if V 1 changes like this, V 2 must change in opposite sense by same value; opposite sign essentially saying delta V 1 must be equal to minus delta V. So, if I say small signal

analysis for this; delta means small signal, change is always equivalent of a small signal. So, IDS 1 is gm delta 1, IDS 2 is gm delta V 2; assuming M 1, M 2 are identical; however, the sum total of this current is always ISS or gm delta V 1, plus gm delta V 2 0 for delta ISS is 0; that is no change in the bias current.

So, these two current must sum to 0 which essentially trying to say that delta V 1 is equal to minus delta V 2; so if V A is the average one goes above, the other must go by same amount opposite directions from the average value. So, V in 1 plus delta V in; so V in 2 must go by V in 2 minus delta V that is essentially the feature of differential; that is what I said. So, any change in V 1 opposite change must come to V 2 by same amount; opposite in therefore, the signs is that ok? Trivials, but that is the concept.

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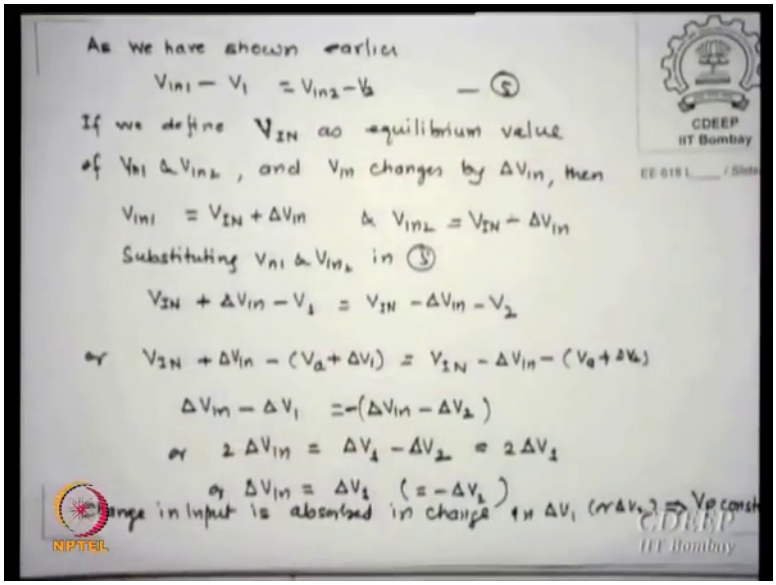

Since we already said that V in 1 minus V 1 is V in 2; minus V 2; we now define another term V in. Instead of V A for the other side, we say now V in is an equilibrium value of V in 1 and V in 2 and if V in changes by delta V in; then V in 1 is V in plus delta V in and V in two will be differential stage means; V in minus delta V in; substituting this here, V in plus delta V in minus V 1 is equal to V in minus delta V in minus V 2; collect the terms and you get 2 delta V in; V in 1 minus V in 2 is delta V 1 minus delta V 2, but we already said delta V 1 is minus delta V 2 or; so it is 2 delta V 1.

So, delta V in is delta V 1 or equal to minus delta V 2. So, change in input is essentially absorbed in delta V 1 or delta V 2. So, V P still remains constant, so any change is taken

care in the VGS value and not in the V P value; is that correct? Delta V 1 absorbs change in V in.

Student: (Refer Time: 61:31) right.

See average value of V in 1 is let us say something; so if V in increases beyond this or goes beyond that; below that. So, some value at the from where I am assuming like a DC level plus AC kind of thing. So, we say any change in V in from a given value; it always get absorbed in that V 1; V 2 values, delta V 1, delta V 2 and does not affect V P any time; is that correct?

Student: (Refer Time: 61:59).

Because we say it is a differential system, we already said any change; the first, earlier one we say change here is same as change here; that is the definition we gave for differential, any change here; opposite change must occur the other end. Which essentially telling by maths also that any change in the input is taken care by change in V 1 or V 2; signs taken care correctly and it does not therefore, any time changes V P value, is that correct?

And therefore, the half circuit concept which assumes V P is constant is valid; this is only to prove that my statement and I said V I am assuming V P constant; this is only a proof of saying that V P will always remain constant independent what you do. Based on this, once I now declared that diffamp; I can always assume that change V in 1 is compensate or opposite change will occur if V in 2; for a differential stage, in that case I will now solve a diffamp using two separate parts of the symmetry; one left, one right; solve independently outputs and subtract and figure it out, whether I get the actual diffamp values, which people diff amp say this is the value.

We will solve otherwise also a diffamp, other technique which is the most under technique, but this technique also is valid in diffamps. So, why did I show you all this? Because this gives you a concept of differential modes and that is why whole this lemma was proved; what is lemma? Lemma is not a theorem, so what is lemma?

Student: (Refer Time: 63:51).

Correct. So, it is the already I have used it to prove something, but I assumed it and proved it; that is what lemma decisions are. You assume it and say is correct or; obviously, you assumed it; so it will be correct. I start with an assumption which I say is correct; obviously, I already started and proved around everything on that thing; I came to same point yes you will, but that is what all lemmas and theorems prove, they start with something and at the end prove the same thing which they said, so QED. So, we will stop here.