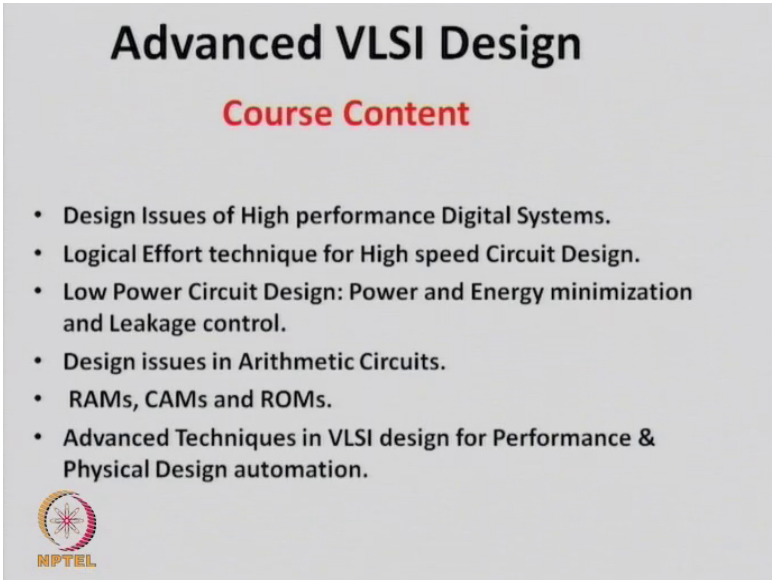
Advanced VLSI Design
Prof. A. N. Chandorkar
Department of Electrical Engineering
Indian Institute of Technology – Bombay

Lecture - 02
Historical Perspective and Future Trends in CMOS VLSI Circuit and System Design - Part II

We continue with what last time we said about the VLSI historical perspective and future trends in the CMOS circuits and system design, this is the part 2 of the same lecture which I gave last time, before I actually start the course let me tell you that what this goes is all about? And what is this course contain? And why we called it advanced? In our first course on VLSI design. We talked of basics of VLSI design including the circuit performance as well as Circuit Design based on which layouts can be created.

(Refer Slide Time: 01:02)

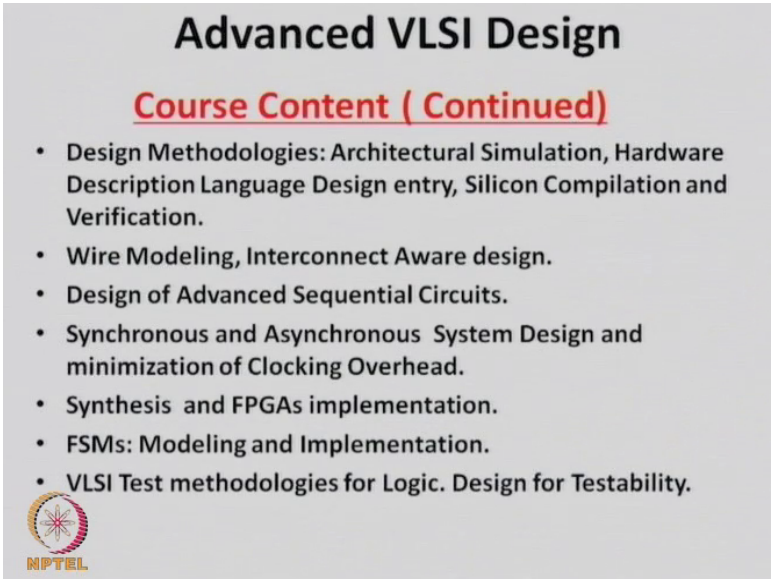


However, in this case we go little along the higher side and the performance side particularly we will look into design issues of high-performance digital systems we will look into how to design high speed circuit using logical efforts technique which was very popular or which has been made very popular by the effort of Sutherland, Sproull and Harris. Then we look into the present requirement of circuit design in VLSI.

Typically, we call low power circuit design and effort will be made by us to see power and energy minimization and in particular how to control leakage under sub modify nanometer circuits, design issues in Arithmetic will be another area of interest because I think the date of path is one of the major block which is used in almost all processing systems.We also look into some new RAMs and ROMs.

And also we talk about something on the Content Addressable Memory is called CAMs, then we will talk about advanced techniques in VLSI design for performance and physical design automation.

(Refer Slide Time: 02:03)



Continuing with the same strategy we will talk about Design Methodologies, Architectural simulation, Hardware description language how we actually put that design as an entry in the compilers and we will talk about Silicon compilation and also some part will spend on verification, what are the major worries right now in high performance circuit design? Is the delay caused because of the interconnects.

So this part we are looking into what we called Wire Modelling and Interconnect aware designs, then we will talk about the Advanced Sequential circuits design and particularly will spend time on Synchronous and Asynchronous system design and how to actually minimize the Clocking

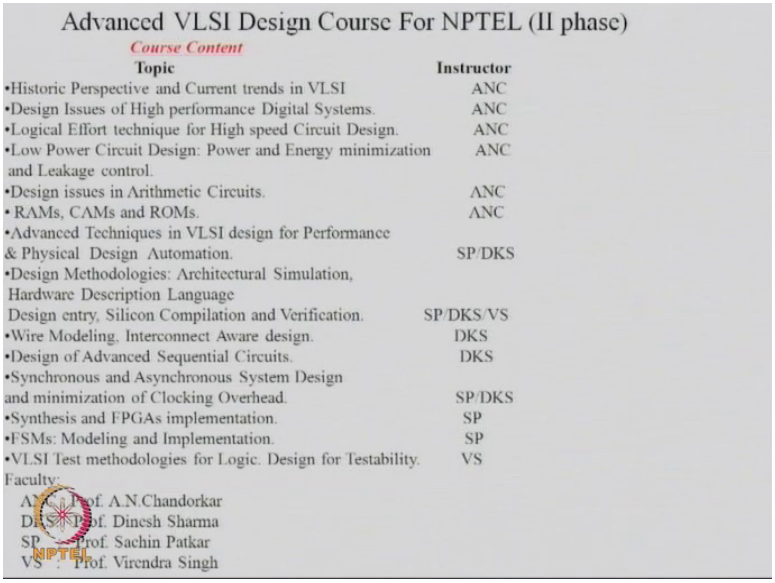
overhead. One of the major emphasis in this course will be how to synthesize the circuit and how do we implement that circuit or system on an FPGA block - FPGA boards.

So this area which is most common area for the most of the people who will probably use this course probably will spend more time on FPGA implementations of course depends on the speaker who will talk about, then we will also like to introduce to you most of the system in the world which you want actually put it on a chip are generally Finite State Machines and this area is very very important for all circuit designers and chip implementers.

So we will talk about how to implement FSM and how to model it and finally and if not the most important part in the whole game of VLSI is the testing of VLSI chip or VLSI logic and I think one of the major part of this course will be spent on VLSI test methodologies for logic and how do we design circuit or chip or testability. This area seems to be one area but I think we spent sufficient time to actually bring to you how these test methodologies are actually valuable.

And how new thing will come up in this area. this is typically a slide which I am you can see there is a pat up slide essentially it is the same topic which I wrote last two slides.

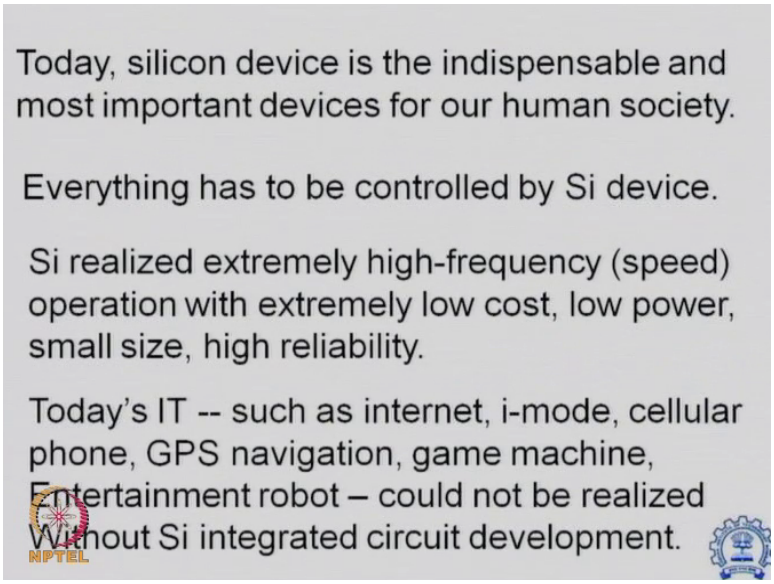
(Refer Slide Time: 04:09)



But who will be the instructors for this each area have been listed, for example first six areas will be covered by me I am A N Chandorkar as I said, then there will be areas covered by people like

prof. Dinesh Sharma, Prof. Sachin Patkar and Prof. Virendra Singh these are the three other faculty members who will actually contribute in this course, because of they are expertise in certain areas of research in which they are working so those area will be covered by them.

(Refer Slide Time: 04:40)



So coming back to what we were talking of historical perspective and trends, let me tell again that today the silicon device is indispensable and most important devices for our human society, if you see very carefully everything which we work or everything with which we work or use is now controlled by a silicon device particularly the silicon integrated circuit are simply called chip.

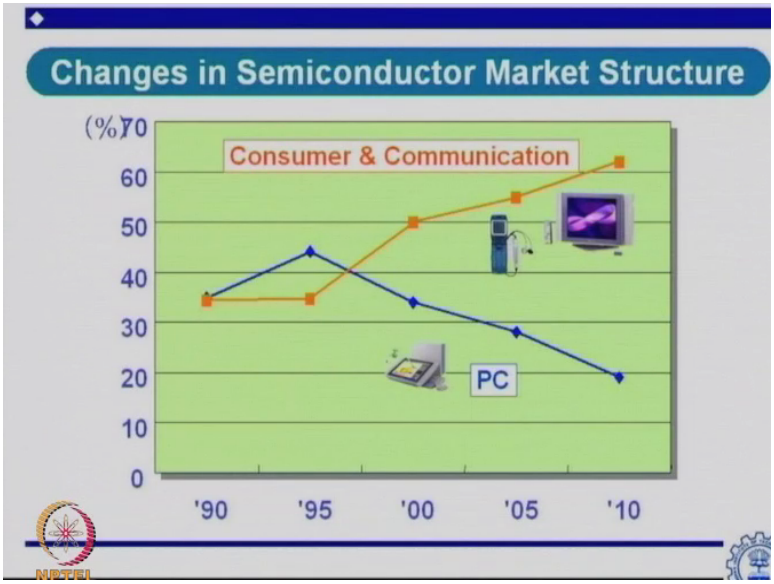
The silicon relies extremely high frequency operation with extremely low cost, very low power small size high reliability and because of this most of the electronics is actually revolving around silicon integrated circuits. If you see today's Information Technology area such as internet, i-modes, cellular phones, GPS Navigation, game machines, entertainment robots. You just think of them and you could not have realized them without silicon ICs valuable and that area.

And therefore the development of integrated circuit essentially revolves around now it is mostly and the consumer electronics and also some part into the defense areas, now what has happened over the years there are structural changes in electronics industry happened from say as we

started in 1960 let us say so by 1990 there are 2000 area we see there are lot of changes are occurred in electronic industry itself.

So I will give some example to show you how the electronics has modified itself in the new era.

(Refer Slide Time: 06:15)



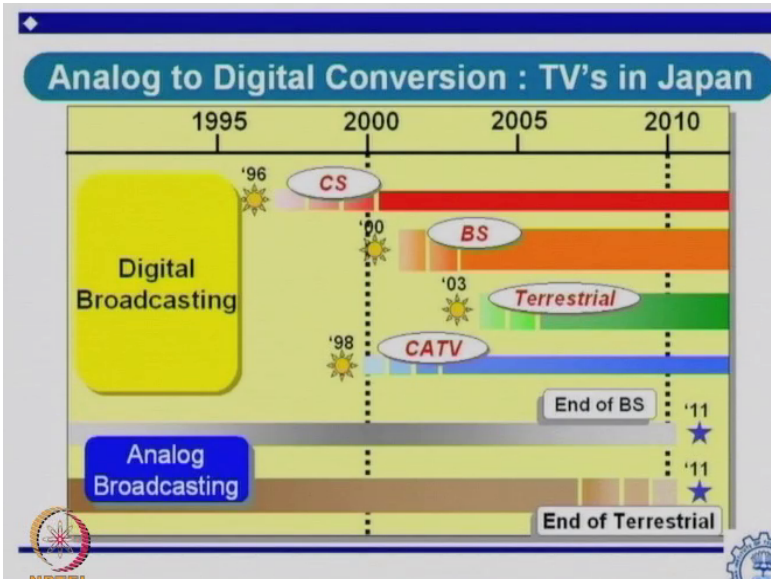
A very interesting slide shown here there are two components are showed one is PC the other is what we call as communication area and we see in early 90s the most of the effort was on PC development because consumer wanted more PCs to be available in the market and therefore up to 95 or so there are huge percentage of effort and money both was available in PC area.

However, by 2000 or 90 to 2000 onwards we can see now mobile phones, iPods, televisions all have they have become now very important part of the society most people cannot survive without the mobile these days many of them including in villages in India and therefore much of the effort in last 8 to 10 years have been now area of consumer and communication area rather than PC.

I do not mean to say that PC market is really very low or it will not continue, but compared to PC market now the consumer electronics market has actually taken over and because of this market structure the VLSI design area has to move on to those area where there is a lot of consumption

and therefore lot of money, one of the major thing happened over the years for example this is slide from Sony.

(Refer Slide Time: 07:34)

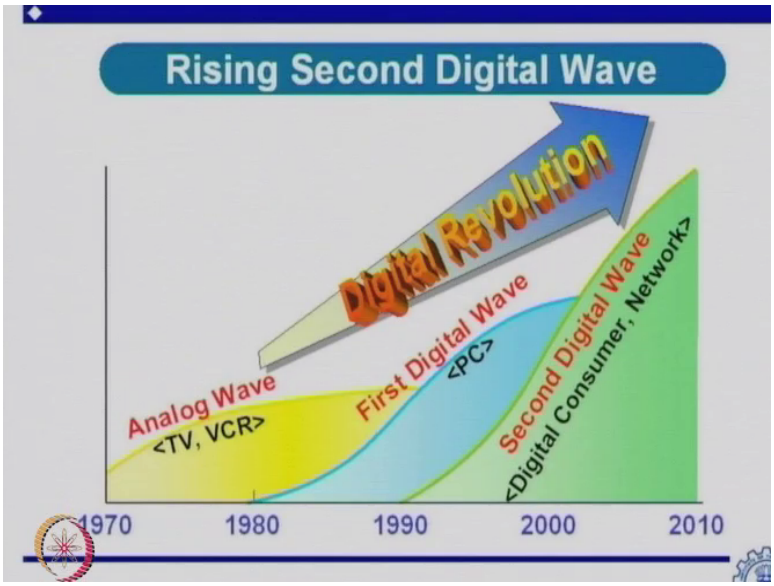


It says that initially the TV broadcast was analog broadcasting way back up to 2000 or 1995 or so and this analog broadcast continued from many years, but after say 2000 or 98 onwards one finds that the analog broadcasting shifted to digital broadcasting for variety of reason, one is the integrated circuit technology was more importantly developed for digital circuits rather than analog circuits.

And much of the advantage of digital is that you can compress data very much and because of that the actual transponders will smaller amount of circuit but can do much larger applications and with larger powers as well. Now you can see from here that since analog to digital conversion occurred much of the research now is more and digital then analog.

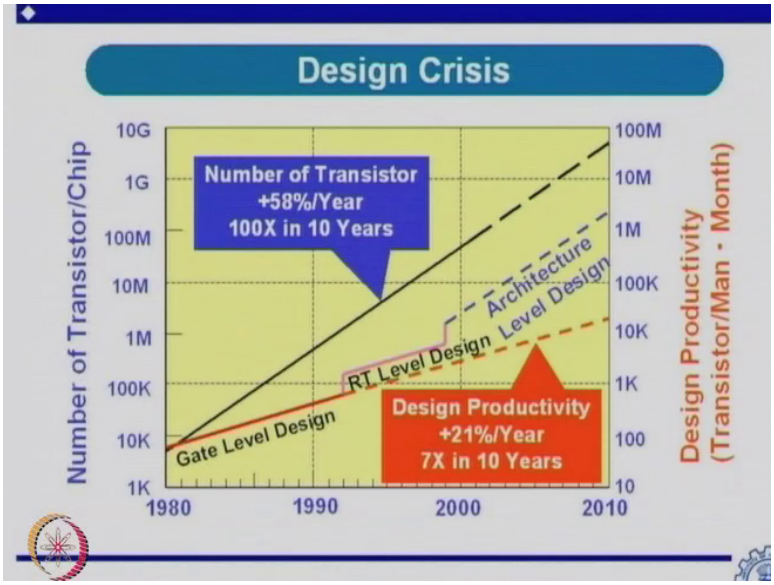
However, one must give rider here that since the nature is basically based on analog systems you do not talk in digital you always say something in analog continues in time therefore one area of a research will continue to happen in analog design which may be more important in the sense that is rather difficult to manage that however most of the silicon market will be actually revolving around digital.

(Refer Slide Time: 08:55)



So one just if I put it again in the same way the first wave one can say was the analog wave most of the VCRs or TVs in consumer market were analog based or analog electronics was used, the first digital wave was essentially based on digital PC market and now of course the second digital wave is essentially on the consumer and network market.

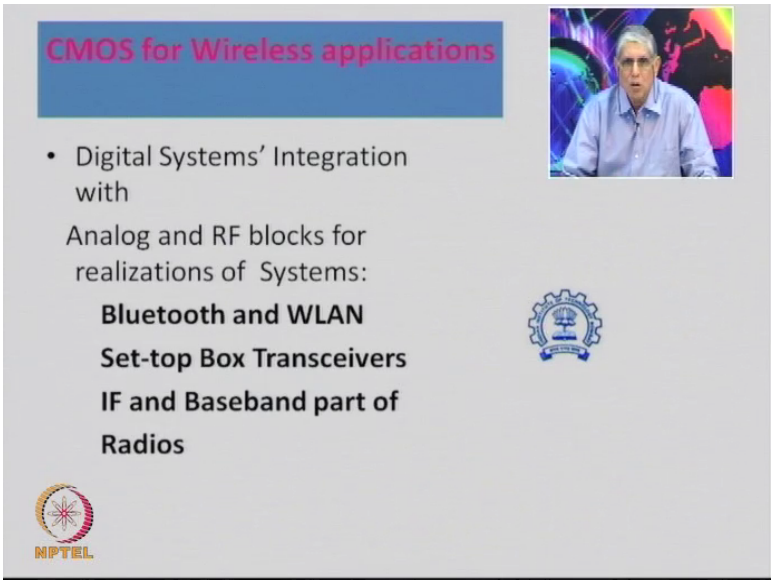
(Refer Slide Time: 09:21)



The problem right now of course the slide is slightly maybe two years older but it still wants to say the same we started with Gate level design early 90s then we went to RTL designs and now we are even talking about Architectural designs, so they are three areas in which we are progress towards the years. But one of the major worries as of now one people are saying that there are not sufficient engineers who actually can work on architectural level designs or RT level designs.

They of course, there are couple of old kind people like us who still believe that gate level design or transistor design is very relevant. And therefore we keep generating such designs in the form of what we called IPs and those intellectual property circuits can then be employ directly at the RT level or even in the architectural level, so the other areas they said apart from the consumer in this is the network area or wireless applications area.

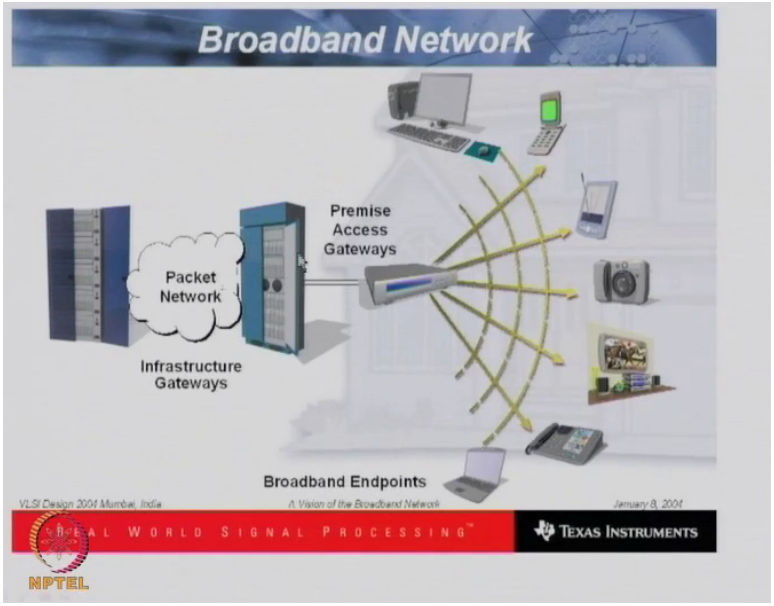
(Refer Slide Time: 10:22)



The digital systems integration is now compulsorily with Analog and RF blocks in realizing this wireless systems, for example there are popularly known systems call Bluetooth, WLAN and also at the homes we have Set-top box trans-receivers - transceivers then we have IF and Baseband part of radios, so all these require both analog RF and digital blocks together. So these are essentially more mixed signal designs which are becoming popular for wireless.

And an effort has to made by digital designers, so that they actually properly interface with both analog and RF systems, just give an idea what is network marketing? Is doing or broadcast on that area say broadband network shown to you here?

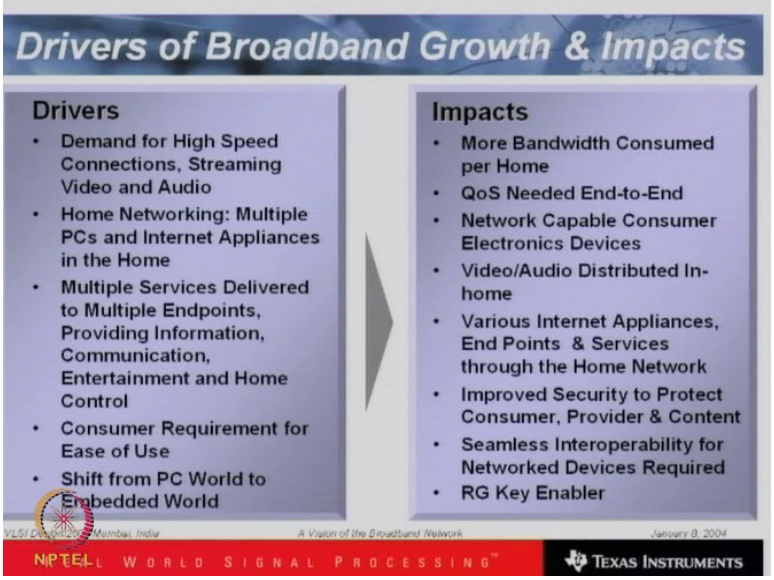
(Refer Slide Time: 11:10)



There is a on your left as I see there is the infrastructure gateways which passes packet network to this kind of storage and from there, there is a trans receiver through antennas they actually then passed to, access to gateways and gateways have connection with PCs, mobiles, iPads, camera, TVs name a printer's, laptops name everything.

So now you can see broadband can have internet connection, through internet can connect almost all kinds of equipment's sitting at one place and that is the area where much of the research and the chip area is done because for such applications the interface will be separate for each of them and one has to really work hard to get chip for all such areas. So what are the drivers of broadband growth and impacts?

(Refer Slide Time: 12:05)



So here is some table which I have you, why I am talking you all this is at the end of the day now as VLSI design engineers probably you will have to know much about the communication area because there is where your money is or there where there butter and bread is, so let us learn what exactly wireless people or broadband people are looking at and then start looking for designs which actually meets their specifications.

For example, in broad band area and told that demand for high speed connections streaming videos and audios probably you know it better streaming videos and audios is what all that you are constantly working at or listening at or seeing at and therefore that is the major demand people see and because of that lot of effort has been made to make such chips.

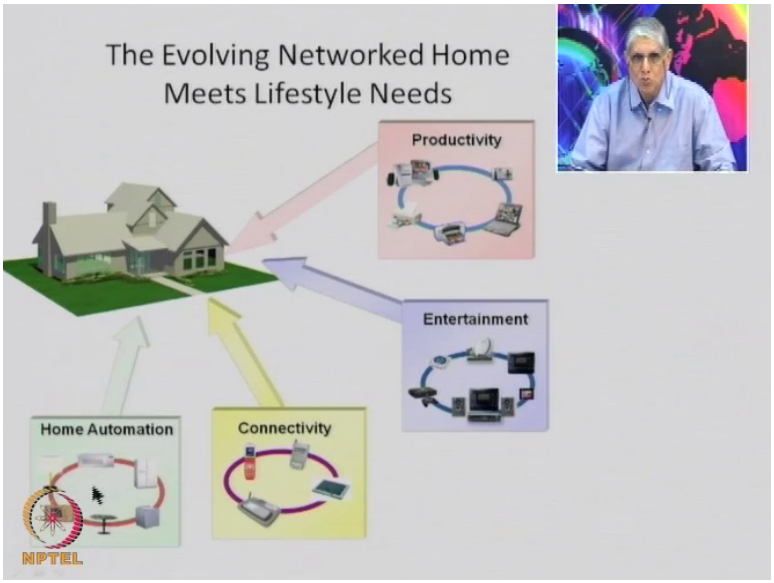
Then there is area like home networking which has multiple PCs and internet appliance at home and you want to connect to one of the internet connections or multiple internet connections are put together through a server router sorry, then there are multiple services to be delivered to multiple endpoints providing information, communication, entertainment and home control, consumer requirement for ease of use and shift from PC world to embedded world.

So what are the impacts? The impacts of these drivers or these requirements, one is expecting much more bandwidth consumed per home this is the impact one sees, then the quality of service needed to end-to-end now, then one also expect network capable consumer electronic devices,

video, audio distributed in homes, various internet appliances, endpoints and services through home network, improved security to protect consumer.

And provider and content, consumer provider and content and seamless inter-portability which is the major work right now going on for network devices required for RG key enablers. So here is some interesting slide evolving network home meets lifestyle presently you are sitting in a home.

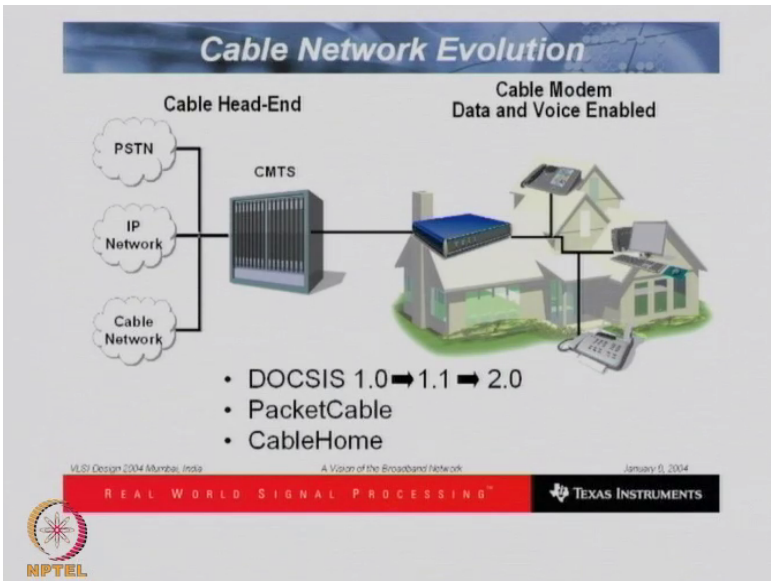
(Refer Slide Time: 14:08)



You need lot of Home Automation your equipment's washing machine to some kind of microwave ovens to heaters and all kinds they can be now directly controlled from which are these are homes, then you need connectivity to mobile and all such laptops and other this, you have entertainment parts sitting here and you have a protective parts like laptop, printer and everything this.

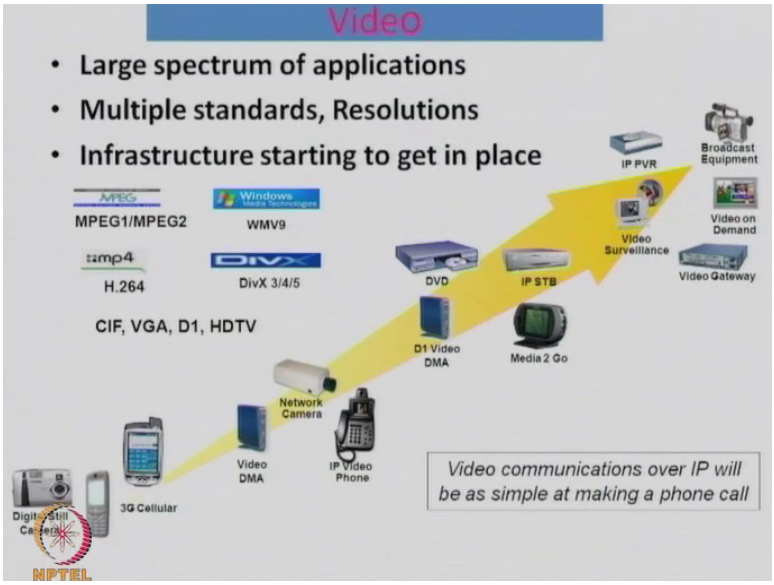
Now all these can be network to a home meets life this is how we are actually now working we are so many equipment at house at one needs to know connectivity instead of getting every now and then. The another evolution which has come over the years in wireless area is cable network and essential part of cable multipoint network is that it can done through a cable modem. One can actually connect the IP network or cable network PSTN directly to the home since cable is normally available in from the providers these days to home.

(Refer Slide Time: 15:16)



So you can have all kinds of standards can be met through three of these networks and directly to your house okay this is the and since it has a largest bandwidth one possible way instead of essential telephone lines or any other probably cable has the largest bandwidth and therefore one will like to continue to have at least Local area networks using cables.

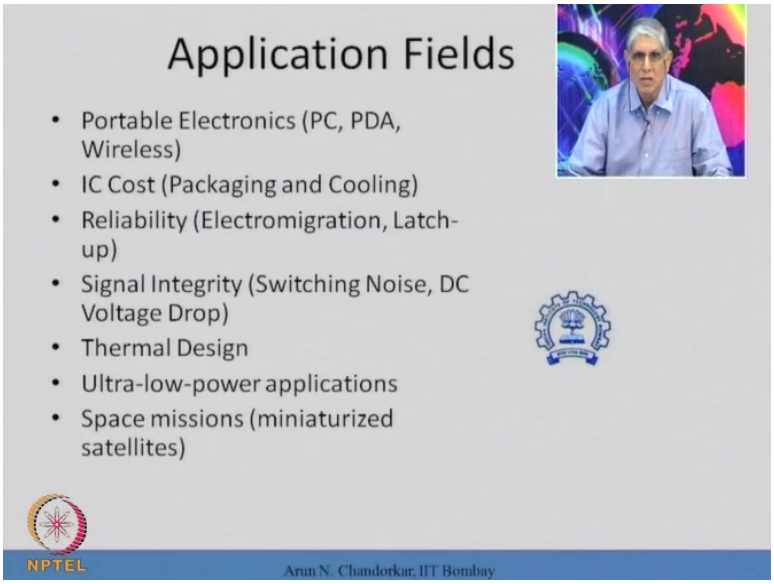
(Refer Slide Time: 15:33)



If you look at the video market right from digital cameras and CAMs, we have 3G cellular phones, we have video DMA, we have network camera, we have video DMA, we have DVDs, we have video surveillance and all kinds of large spectrum applications multiple standard resolutions infrastructure starting to get in the place, you need MPEG standard, JPEG standards and what not.

So in this application's there is a lot of scope for digital designers rather a VLSI designers to actually work for individual area and actually help this equipment's to be network as well as do their performance for better. So to summarize on that there are we call it application fields where VLSI will be required.

(Refer Slide Time: 16:25)



For example, in the area portable electronics like PC, PDA, wireless one of the important application based on application one has to worry about what is the cost of the chip? We are making, particularly we are more worried about packaging and cooling, please remember it is much easier much cheaper to make a chip but it is much costlier to package and keep it cooled. I think much of the research is now shifting and many industries on packaging and cooling area.

The other problems with application like PC, PDA, wireless or any other thing is an issue of reliability, particularly reliability due to in the chip itself due to electro migration and largest CMOS. The other areas of worry is of signal integrity we have too many interconnect lines moving on a chip this is something like a transmission line now working on those high frequencies of signal going which may give you lead to switching noise.

It may give voltage drops like power voltage droops or ground bounce noise, ground bouncers and that may actually change the signal from one line to other or may actually switch over. Now

these are the very relevant issue in 2010 and onwards and therefore much of the work and much of the chip design work is now going in the area of signal integrity, the other area of interest as I said is the chip as going to have large number of transistors typically millions of them hundreds of millions and we are going towards a billion now.

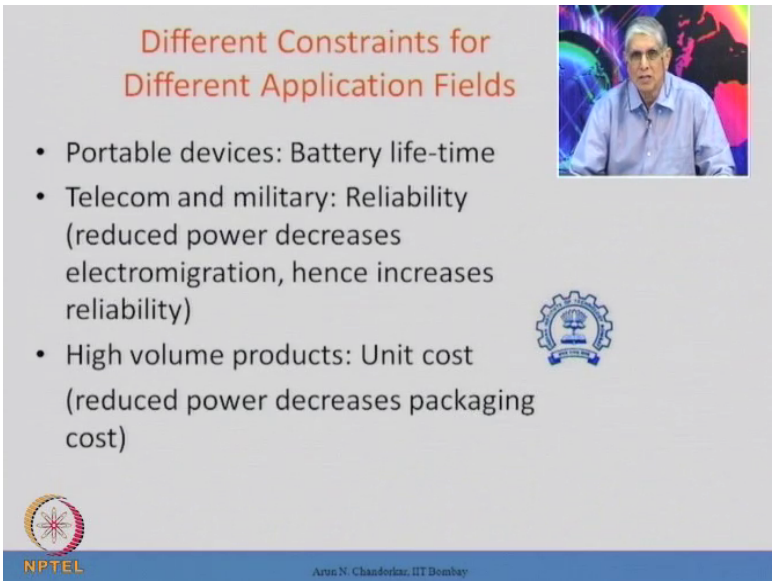
And therefore even if 50% of the transistors are on even if you are working on very low power design the kind of heating which chips are going to have is very excessive in particular power density is very very high and now much of the efforts needs and needs being done right now is to avoid or used to see how to remove this heat from the chip so that the chip continue to work. Please remember that around 175 degree centigrade all semiconductor junctions becomes no junctions.

And therefore the chip starts failing into their operations, so one has to keep worry about this thermal designs particularly the differential thermal design is very important because one spot there is may be large heating because of power dissipation the other maybe cooling. And therefore the gradients creation may have more problems than the heat at a spot itself and people are trying to see how to take heat out.

And the large area, large effort, right now they said is ultra-low power applications particularly all handheld systems like mobiles or PDAs or name one you will find you will not like to charge your battery often. And therefore we are really looking for chips which themselves consuming low power so that the battery last longer and you do not have to recharge every now and then. And particularly the last and the most important area field right now is space missions.

There you have much more problem. You have problem of power dissipation, you have problem of size, problem of weight and very high - high level of integrity of functions to be implemented and therefore space chips are very very difficult to design, however one need not worry because we know the techniques if someone wants to pay for it those chips also can be designed. Now there are I said, I already said some but I quickly repeat there are different constraints for different fields.

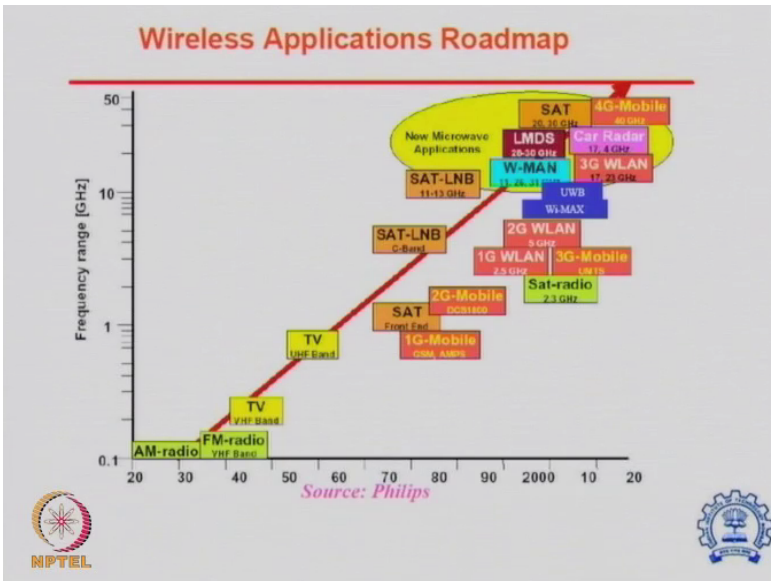
(Refer Slide Time: 19:55)



For example, portable devices essentially limited by battery life time, Telecom and military reliability decided rather worried about the reliability performance, high volume products of course always decided by unit cost and that is the constraint, because you make a chip and it is very, very costly how many buyers were buyed and then the cost of the product which you were going to have may not survive in the market.

so the particularly the off self-products like memories or something you must know why they are comparatively cheaper because they are we are trying to make them in millions so that the per unit cost is minimized and also of course they also require reduce power decreases packaging cost if you can reduce the power essentially one can also reduce the power packaging cost.

(Refer Slide Time: 20:47)

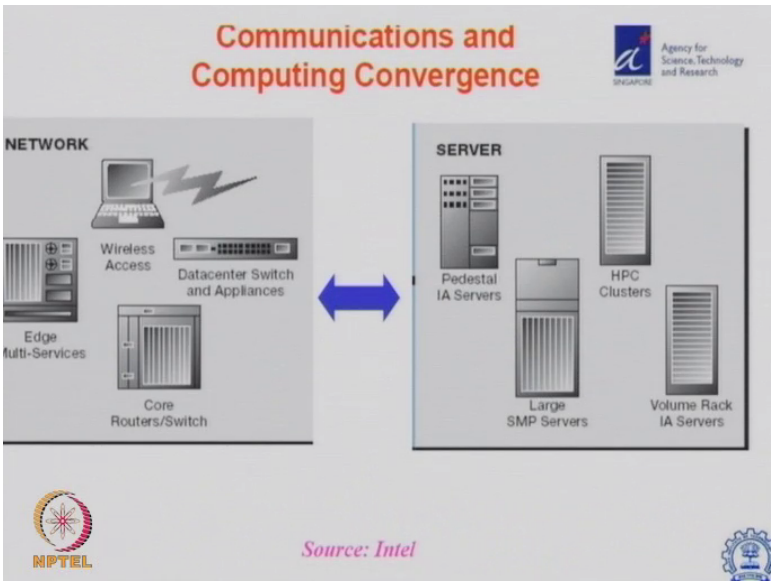


Here is the road map once again about the wireless applications roadmap, one can see over the years this is I have taken it from Philips, it shows the frequency range of operation over the years, we are started with FM radio, AM radio, FM radio, TV, VHS or recorders than TV with Ultra high band Ultra high frequency UHF instead of VHF. And continuing with this one can see now we are talking of LANs, we are talking of radars, we are talking of 3G, 4G mobile systems.

We are talking of other microwave applications, we are looking into I mean most of the circuits system which I written here are known to you and one can have look into these, these are the wireless systems which are coming in to market and day by day they are asking more and more applications and they are asking much more performance improvement in what we have so far able to give, so much of the result in VLSI is now dedicated towards communication and particular to the wireless.

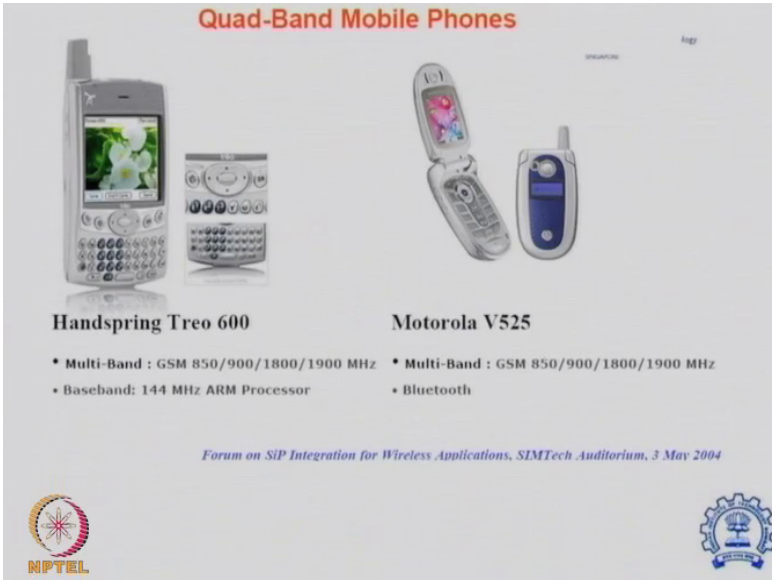
There is also as I said we always initially thought we are talking about computers in mostly chips were actually design mostly for logic which we went into PC market.

(Refer Slide Time: 22:07)



However, looking at the two figures here you know there are one is the network area, other is the server area and one has now a link between the two and there is a convergence going on between the communications and computing.

(Refer Slide Time: 22:21)



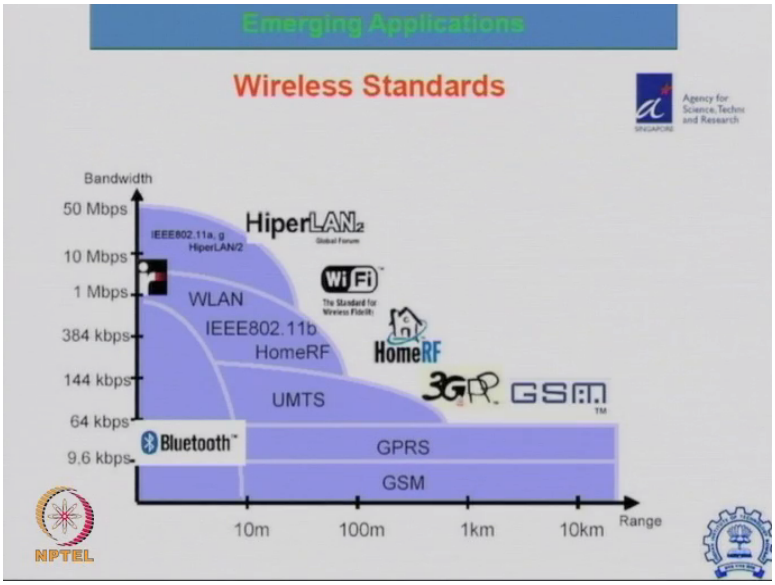
For example, another area which most of you are aware of is broadband mobile phones, you want to have all 4 bands 850, 900 and 1800 and 1900 covered in the single handset and because of that and they also has to work probably on the Bluetooth's. Generally, they use the ARM processor in most cases, wireless has become many times the standard has come from ARM processors and now to design around these systems and for all such required requirements.

It requires a lot of effort and lot of hardware to actually supports such kind of systems

(Refer Slide Time: 23:02)

The other area is the smartphone I do not have to say much about you know much about smartphone these days every now and then on the advertisement and any this you see continuously are talking of smartphone what it can do? Okay.

(Refer Slide Time: 23:14)

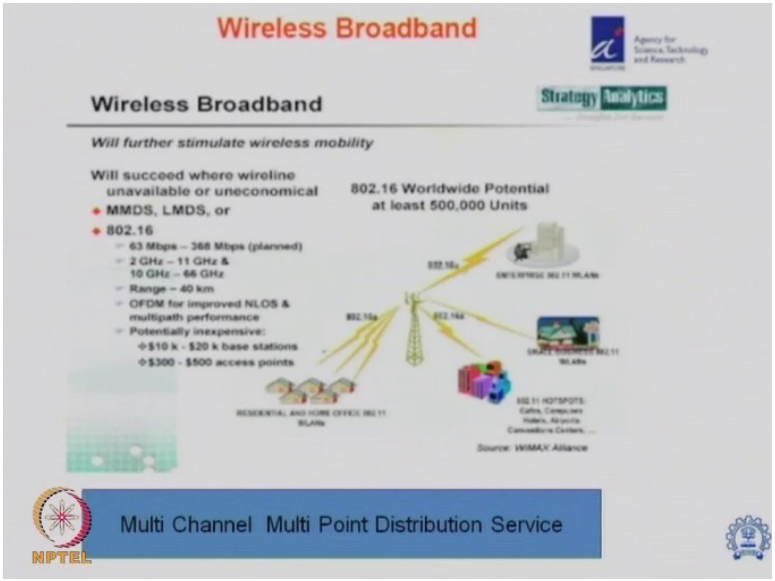


This is the same these are standards of wireless where we are trying to work, the problem with standards why I shown you this graph is the kind of bandwidth one is expecting and one is getting for example GSM requires say around so many KBPS say 60, 10 to 60 KBPS up to 10

kilometers range. So that range become most important in the case of GSM where other you have a WLAN.

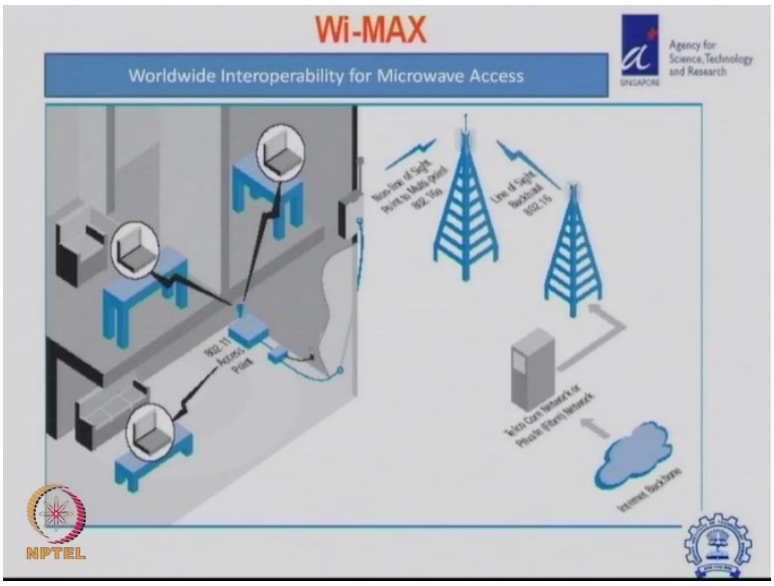
They have limited local area network or small low medium area networks their ranges are acquired smaller but they actually required 1 MBPS and above kind of bandwidths. So one of the work is how to improve the bandwidth and how to improve the range or the power and one probably knows from VLSI design basics that both frequency and power cannot be improved simultaneously but that is the area where one wants to work how to improve the bandwidth even with reduce power.

(Refer Slide Time: 24:23)



This is the wireless broadband please remember wireless is the multi-channel, multi-point distribution system which are now coming up they are the forerunners of VLSI designing communication, for example you know the new standards which are coming 802.11, 12, 13, A, B, C, D then there is 802.16 each has the different bandwidth, different ranges to act on, different applications to work on and for you have to work on every kind of area and design chips for them.

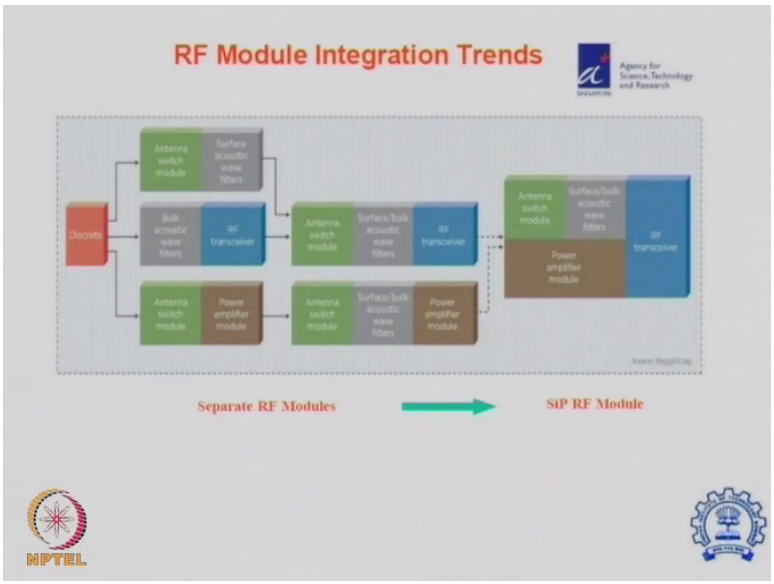
(Refer Slide Time: 24:50)



This is another interoperability microwave access worldwide which is Wi-MAX popularly known you are trying to connect your PCs through such kind of network, you want microwave access network and this is an area again where interconnection, interconnectivity is very important or inter-portability from one area to other is very important and the access is through microwave.

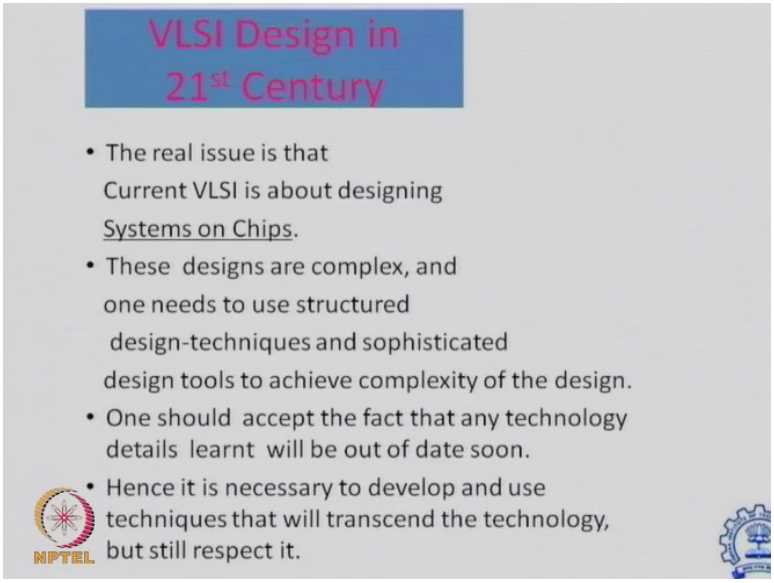
So now we are trying to see whether low frequency signals can be connected through or transmitted through very very high frequency signals to other areas and retransmitted back to your original frequency of basebands. The other area which is required in VLSI these days is RF modules which may be part of any wireless system.

(Refer Slide Time: 25:37)



If you see your left part, if there are more than say 9 or 10 parts on the RF module such 10 modules may be required to make a function and now you can there is a new technique of packaging has come what is called system inside a package? And if you do that we can see from here these all parts can be minimized into a smaller chip you can packaging one area and such a module will be much smaller in area as well as you do not need a breadboard or you do not need a board to put them on and associated problems of connectivity.

(Refer Slide Time: 26:21)



So what is VLSI design? In 21st century the real issue is the current VLSI's about designing system on chips, okay. Now these designs are extremely complex and one needs to use structured

design techniques and sophisticated design tools to achieve complexity of the design, one should accept the fact that any technology details which we learn over the years will be out of date soon.

To give an example in 1960s or 70s I was a student, I did not know anything about semiconductors in my under graduates but when I did my graduation Master's I did learn basics semiconductor theory, basic semiconductor diodes, basic semi and then we also learn something about integrated circuits in a smaller way a TTL circuit design was tried a way back in 70, but that was the great thing we were thinking we are ahead of time we used to think on those days.

However, the technology from TTL has shifted to mask as I have already shown you in my first lecture and we can see from there that the current technology trend because of the reduction feature sizes is going down very heavily from say 10 microns which we worked in 70's, then we worked on 5 microns in early 80, 81's and 3 microns in 85 and now we are working on 0.25 micron down as we may go to 7 nanometer technologies.

So if even if you master a design for any technology, the when the technology upgrades or rather improves because of whatever you say Moore's law then one has to redesign many circumstances, so effort is now being made because of the technology moves faster than what everyone thinks then one must learn to develop and use technique that will transcend technology.

But remember even if you are designing independent technology you will must know the technology well you must respect it because otherwise it is not possible to actually get the best performance in 1977 to 78 time the first VLSI design book appeared in the market and that was written by Conway Mead - Lynn Conway and Carver Mead, Carver Mead is a Professor at Caltech Professor emanators Professor of Computer Science, Electrical Engineering Electro Physics and what not.

He is one of the most respected person in VLSI area what meets just and that is what this last line is all about that if a computer scientist or computer engineer wants to design the chip he need not know much about technology and that is what he actually makes some kind of a rules which he

said or both of them said design rules, design rules were essentially technology constraint for a given technology.

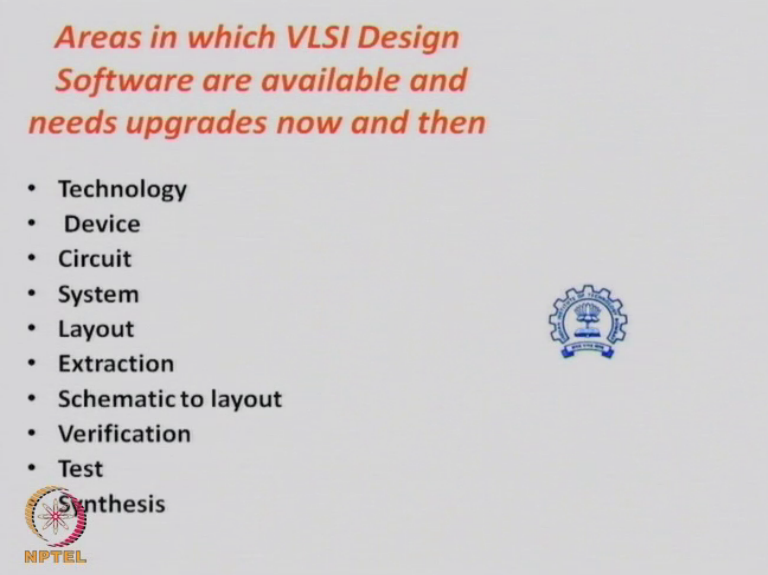
Because anyway finally when you go on silicon you have to print and you have to edge or deposit do something to make that process go there, now because the technology features very very technology based or difficult based and they have no litter spots as long as you actually follow the consent of technology in your designs the layouts you may then one possible. One of the major advantages that when those mask which are converted from your design or send to technology house.

Most likely, they will actually reproduced whatever designs you are asking however this word that you do not need technology any much now is valid maybe it was valid till today or maybe few years ago as of now when you are looking at 45 nanometer down process unfortunately the technology has not only improved many thing but also has induced many problems. Now these problems cannot be characterized in some kind of a design rule.

And they are very individualistic process technology based rules or technology constraints and therefore even a designer now has to understand the limits of technology in every case particular chip part of that may be a different rule, one has to now has to set with a strong technology person or also you need good modules to actually translate in to new tools. And therefore the physics people physics of or physics of technology physics people, technology people, device people, even optics people.

And also the VLSI designers both Computer scientist and Electrical engineers all should sit together and I essentially decide if a product has to made how will be they go about.

(Refer Slide Time: 31:12)



Now areas in which VLSI design software are now available and will need upgrades every now and then are the following one have software available in the area of technology, there are good technology tools available, the first technology process simulation tool came from Stanford over the years TCAD people have developed many new model based tools which can actually make technology go on the computer itself before actually realize in the lab.

So there are TCAD tools which also includes in the vocabulary of TCAD, there is also good device simulators are required or device designers are required which will pick up data from technology files and then actually design a device and then find its performance then we having made designs of your choice, we know the models of them.

One need to design a circuit, so you need those models to be put into like there are programs like Spectre or Spice, HSpice these are essentially circuit networks adware's and they can be used actually design a circuit and using a circuit you can design a multiple circuits and then bring them together to realize what we call systems and therefore you need to know having which blocks to put when the system performance can be attained.

So need a system simulator or system tools which will can see the performance, after making technology device, circuit simulation, system simulation or tools associated with them you can use for example famous such this comes from synopsis, cadence, mentor graphic all of them give

such CAD tools for every technology node. But finally at the end of the day since silicon your design has to translate on a silicon you need what we call the mask or an each on each mask.

You need the layout, so their layout simulation tools then after you laid out a circuit you want to know whether the circuit itself may work or may not, so you extract the circuit back from layout already drawn by you and you re-simulate both circuit level and check whether the specifications given for the system can be made by this layout which we already drawn. If it works fine otherwise, you will go turn around change do it again maybe device model sometimes.

Or change the device redo the circuit analysis circuit simulation, redo system simulation, redraw layouts, re-extract till the specifications what you started with actually meets, so you need extraction tools that is an effort to reduce the cost of design. So you every time you do not have to design a circuit specific tools and is this you can use this library of circuit systems and you can have their schematic available.

And then you can have a program which can directly converts your schematic to the layout for a given technology, so such tools are also available and we will need constant upgrade has a technology upgrades, as I said earlier also one of the major worry the VLSI design is the test. Because on a way for there may be thousands of chips may be more at times and in every chip there will be millions of transistors.

So there will be at least if you look at the small block level design test even then there maybe hundreds of them on a chip, now how do verify your performance can you go for every block checking or do you actually test every chip. Because if you test every chip and every block for its performance it takes excess your time that is called verification time is very high therefore manuals required are very high and therefore the money required is also high.

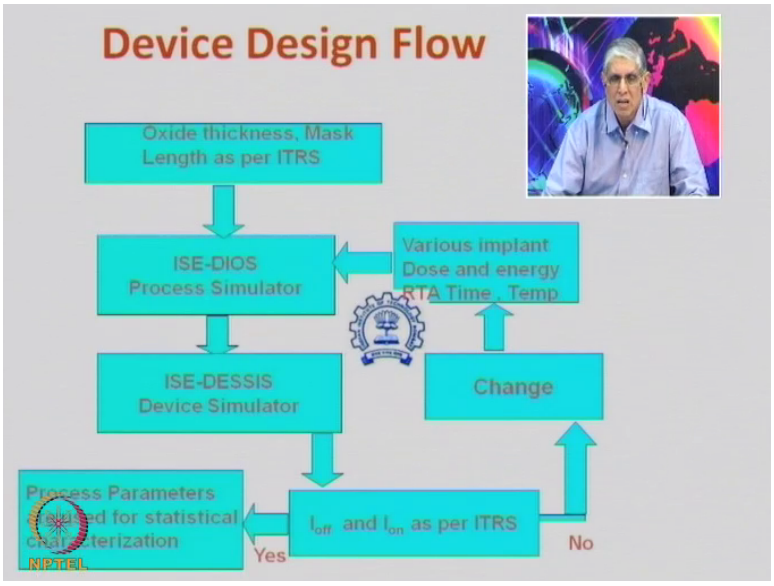
So one has to now generate some kind of tools which will as if say okay, if I take this much it almost gives you confidence levels of test 90% success, so to reduce your verification and testing time this verification test or not exactly same but they are may be together. And one has to really

find the process in which both can be used to actually minimize the effort before actually chips are made.

Then, there is a last area particularly for when you want to see whether circuit can be directly put on silicon or even at on FPGA kind of boards or many other standard cell based designs. So you have to synthesize you need lot of synthesis tools which will actually be able to then decide whether your performance due to interconnects and putting all blocks together will actually work. A typical what IIT Bombay we have a device design flow just to tell you what kind of TCAD tools we use.

For example, if I want to design a MOSFET, I have, I had to first say what is for a given technology node from the ITRS, I know what is the oxide thickness? And what are the features sizes as per the technology node I am working at.

(Refer Slide Time: 36:25)



Then I use a process simulator which is DIOS which is ISE-DIOS and it requires some inputs like it needs to know all kinds of implant dose and energy, it requires RTA that is Rapid Thermal Annealing times and temperatures these are the for individual process in the process simulator for oxidation, diffusion, implants other are at least I must tell you there are at least 450 process test through which we go through when we make a chip.

So far each of them you have to provide the exact data which the process will use and based on that process simulator will tell what is the performance of this device will be? So having made a process properly required then you actually use device which is made out of this process maybe a MOSFET, may be a transistor other than MOSFET, may be HEMT's or maybe diodes may be capacitors any device which you made out of this simulator has to be done tested for device performance.

And we say there is a program which is called device simulator this is and using this we know what are the device parameters? For example, MOSFET you get off current on current you monitor them what is you get it and you must see that whether these are as per the process you are started with which is as per the ITRS, ITRS stand for International Technology Roadmap Services.

And this is a body of engineers all across the world from industry academy which decide what next that is today's ITRS will tell you something about 2012 road map, next year they will say what about happened in 2013 based on their previous experience so ITRS is a very interesting body which is essentially managed by Semiconductor Industry Association and they actually predict what will be the next and how will you go about and they are which will be our standards.

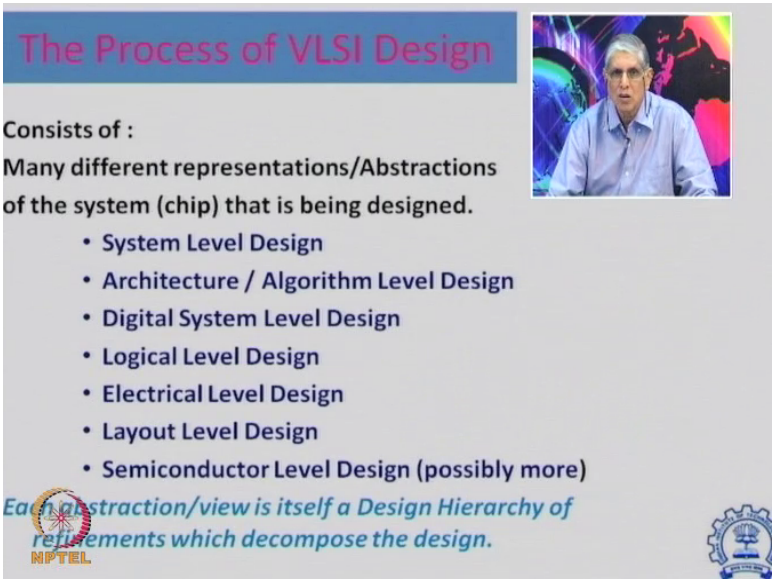
So if your process you started with for an ITRS process step 0.13 or 90 nanometer or 45 for those devices ITRS already prescribed off current and on current maximum in and if after your simulation device designed you find those are not met you actually change once again your process parameters you go back to your DIOS we change process parameters you redesign the device and get device simulators and check for off and on current, any other specks can also be tested.

But these are the major iron essentially which is majorly look for the I dsat, so once we get those specks which we start which we are looking for then we have a process parameters are used for statistical characterization because they are variation in process parameters so one has to another

realization whether they are process parameters of statistical in nature otherwise you may have to do redo again your DIOS and this is once again.

So this is how devices design so one can see if you do not have a simulator you cannot keep tweaking so many parameters like for example in the case of implant energy dose and many steps, there will be at least thousands of combinations you will have to try and manually it is just not possible to do any such simulations, so what is essentially in nutshell we say this process of VLSI design is.

(Refer Slide Time: 39:58)



While it consists of many different representation and abstractions of the system that is being designed, for example there are many levels of abstraction and representations for a given design on a chip or system which you have to actually look into their individual hierarchy level design the highest of them hierarchy level system level design, so one start with design what system you want to actually require, what are the specifications? And how will you design that system?

The next level in hierarchy is architecture and here where we do most algorithm based designs and having decided an architecture for your individual blocks which you can algorithmically test and design, then you look for the how do we implement those algorithms architecture using digital systems.

So you come back and then start looking for digital system level design which can then use to create systems or blocks which can then go to architecture and which finally such architecture with different blocks can be create a system, but each digital system we know is essentially consist of logic, so we have to come down again in hierarchy and we say okay we will look into logical level designs for each block of system which you want and at that time you will only simulate the logical performance of the block.

For example, if you have a NAND gate or a NOR gate or a higher level arithmetic unit or multipliers, so you actually test the performance based on the logical level design, however logical levels for a given technology will be decided by what technology rules you have for example you are working on certain technology node.

So what is the kind of speeds you are looking for, what is the kind of power dissipation you are looking for, what is the size of transistors you are looking for, these essentially will decide the performance of your logic gate, therefore the next level of hierarchy is the electrical level design and this is the most important design for an engineer of my kind who basically believes that the electrical designs are the ones which finally decides the performance of a system.

However, I do not want to reemphasize again that only electrical level design is important, if people have already designed many of the electrical level design blocks they can be reused in logical we can have more logical redesigned blocks, you can use in larger digital system and many such systems can be created in to systems, so it is not my point to say that only has to work on electrical level designs.

But if you are a computer scientist or computer engineer probably you may prefer to work on first three hierarchy levels where system basically things are available and you are trying to reaching them in to a given performance, where are the if you are more of an electrical person or who thinks more about electrical performance as the only thing for him then he should more work on logical level electrical level kind of.

If you are a process level man or something at the end of the day you need must be created out of your design, so someone has to make layouts for each of the mask you are designing for the electrical performance essentially transistor sizing, transistor connections through interconnects at each level of mask you have to design, so you need layout level design is very important because many times the failure of the chip occurs at the bad layout done by you, okay.

because there are parasitics associated which many times you are not able to extract and if you do not do that well then you are circuit does not work, therefore this level design is very very crucial these days particularly in the case when you are doing analog RF and digital on ship as a layout essentially decides the success of your system, having done layout designs the final and the most important part is the semiconductor level design which is essentially talking about the process.

There are many other levels possibly one can go down more specific on the process side but this course since its more on the VLSI design side I will restrict myself to only this level, now most important thing out of all this what I said that each abstraction or a view is itself a design hierarchy of refinements which decomposed the designs, so essentially many times I person like me will say you actually design from the top so it is called top down design.

But when you implement you always do bottom up implementation, first you will have to look into the device process available based on which what layout you can create, then the layouts are created to make the electrical performances extract back, so what we say top down design and bottom-up implementation is the best hierarchical design one can try in most of the VLSI system - VLSI system designs.

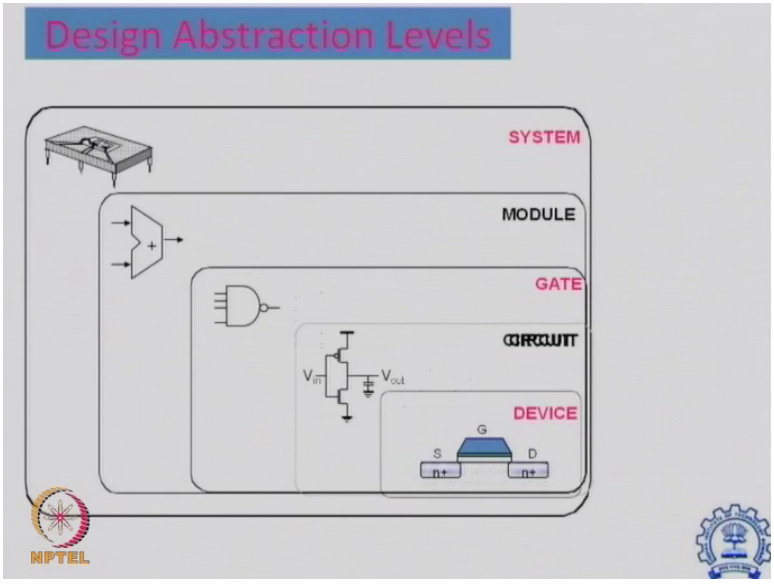
So basic idea is to decompose the system into blocks of algorithms architectural blocks, each such block and be converted into digital blocks, each digital block can go into different logical blocks, each logical block should contain the electrical transition level blocks and like for example a NAND gate consists of 4 transistors, so electrically you have only two n channel to p channel transistors in static CMOS, where are logical levels you have one single gate, okay.

So hierarchically you are actually decomposing from the top side towards the bottom side and you actually designed from the lower side so that you achieve the top side which the specks you are starting with, this is a typical process of VLSI design. There are other direct methods one interesting feature of this hierarchical design is you are allowed to enter at any hierarchical level.

For example, if things are available up to this take that thing logical blocks available and start designing digital architecture system of implementing them however there are you are limited by how many blocks you have available but if you have large number of blocks which can among from which you can make requisite digital system and therefore based on a given architecture can create a systems so well and so good.

Because it will save you a lot of effort, money, time in the last three four parts and therefore it will save lot of economic it makes economic sense to go on the higher level, however not every time it is true or not every time it is so easy.

(Refer Slide Time: 46:48)



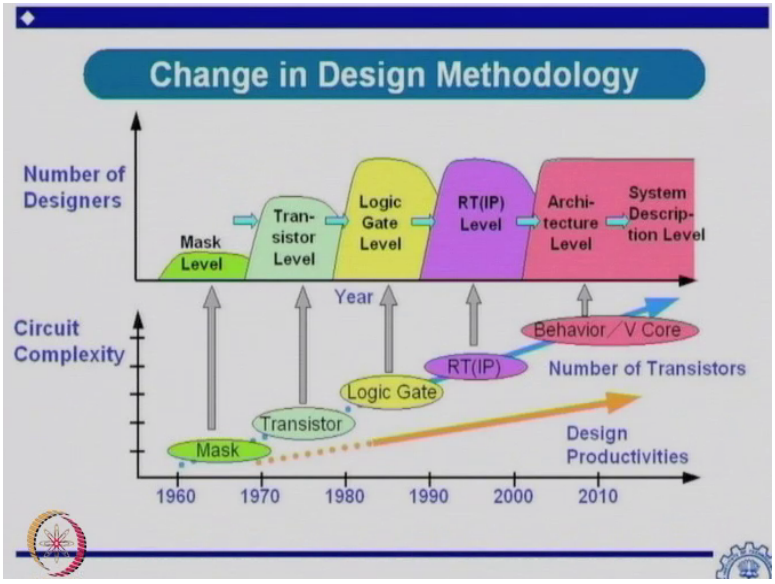
So to give the same thing what I said so far I may give you a figure the first hierarchy down - the lowest level of hierarchy is device, the next level is the circuit you can see a inverter CMOS inverter had been shown using one n channel device this is a one transistor, so I have one n channel, one p channel to create a circuit, then next level using these inverters and separate connections for different transistors, I can create a gate.

For example, if I put two p channel and two n channel devices in series, two p channel in parallel and two n channel in series for two inputs it becomes a NAND gate, so I can create using four transistors NAND or NOR gate, so you say the next hierarchy is the gate using gate number of gates you can create a module.

For example, a simple module shown is a masks 2 to 1 masks or we have 4 to 1 or whatever masks you have or decoders and encoders or even higher levels multipliers even adders they can become modules and based on these modules you can do interconnection and then you can make a system which can be package.

So this is typical hierarchy in Which VLSI design is work and as I keep saying you have the possibility of entering at any level if the lower level data is available to you. Now this is just to show you what people like us in 70's we were trying to design circuits, integrated circuits and what at your level now you are looking for.

(Refer Slide Time: 48:23)



There are two circuit shown to you - two graphs shown to you the lower one shows circuit complexity process versus years and one can see from here we started with mask, then we went for transistor, logic gate as this you know we were trying to improve the productivity that is

number of transistors per chip and this is what we did for many years on the circuit complexity side.

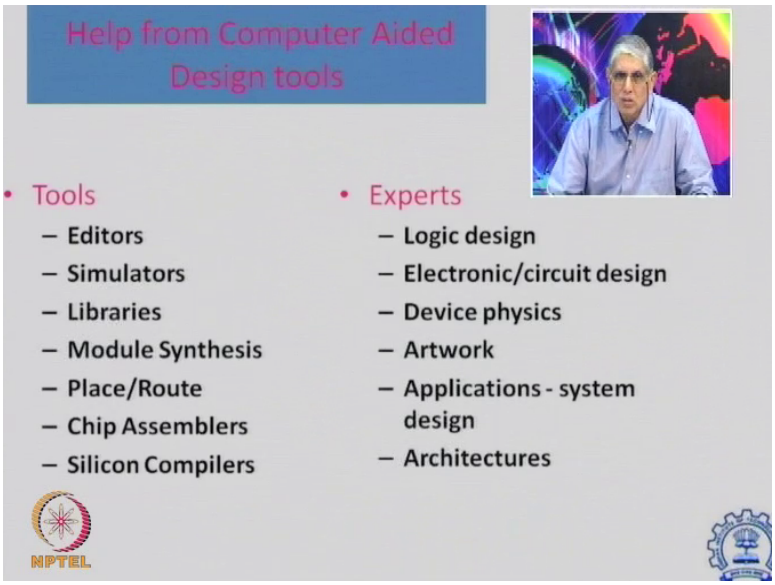
Then when you see now ahead we say now number of designers required at the mask level or some numbers, you need much higher number at transistor level, you need much higher now at logical level and presently probably once you know behaviour of the core itself you need many more engineers at RT level are creating using IP's then architecture level and system description level.

So the attitude of VLSI designers are now moved from basic transistor design which electrical people always believe as the best possible design, now is what is available from your library of functions and then you can do RTL's or architecture level or system design descriptions and can design a chip much more efficiently and much more cheaper way.

At times it may not be able to if you are not able to meet specification exactly you do turn around take another level of gates and redo all this but you certainly do not have to every time go to a transistor level design because this kind of blocks are already made available to you by something called library functions.

So the idea behind all these designs which I said is essentially cannot be done manually and since it cannot be done manually you will have to use computers and the tools which help you are called CAD tools, CAD design tools or CAD tools, so for example you have a tools available now in editors, these are called editors.

(Refer Slide Time: 50:27)



There are tools which like simulators, there are tools like libraries were the functions are stored, then you have tools like module synthesis tools, then you have place and route kind of tools in which you have a different blocks standard cell blocks, you can place them automatically and also reconnect them number of ways to get the best performance, so place and route algorithms are available and tools are available.

Then there are chip assemblers, number of such chips can be together put to make a larger system and finally there attempt to make all of it together in one area which is like a computer compiler one can do a silicon compilation automatically designer chip giving a performance, so you give a behavioral description and probably it will give you the final silicon requirements on that.

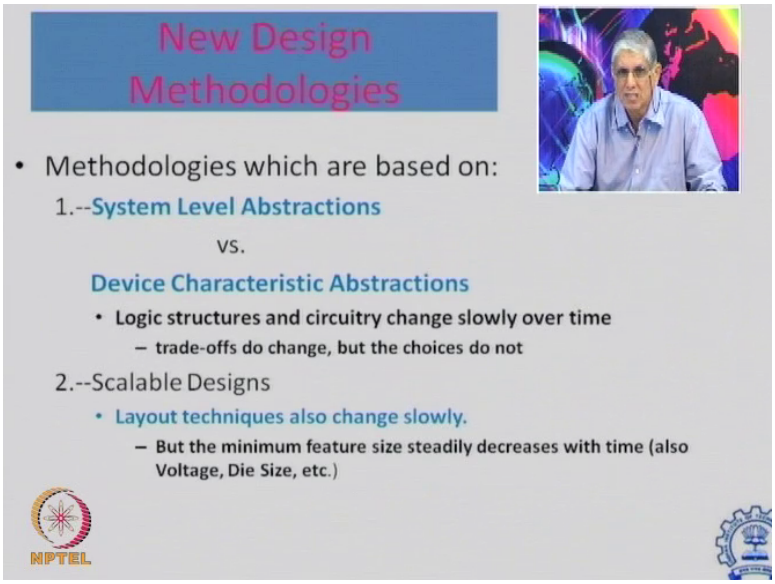
However, you need to do all this kind of tools you actually need experts on logical design, you need exports on circuit and electronic circuit design, you also need lot many physics people now after we are going down in technological nodes to 65, 45 nanometers 32, 28 because lot of device properties are changing as you scale down.

And because of that the ill effects of scaling probably have to taken care and this device physics people are the only ones probably who can suggest modifications or how to handle that, then

there is you need for layouts for example you need a good art work people, you also need people in application system design people and you need people in the architectures.

So if you are in any of these areas I think VLSI designers look for you it is not that only circuit designers are most important or logic designers or layout designers or device everyone has to contribute to a success of a larger VLSI system.

(Refer Slide Time: 52:50)

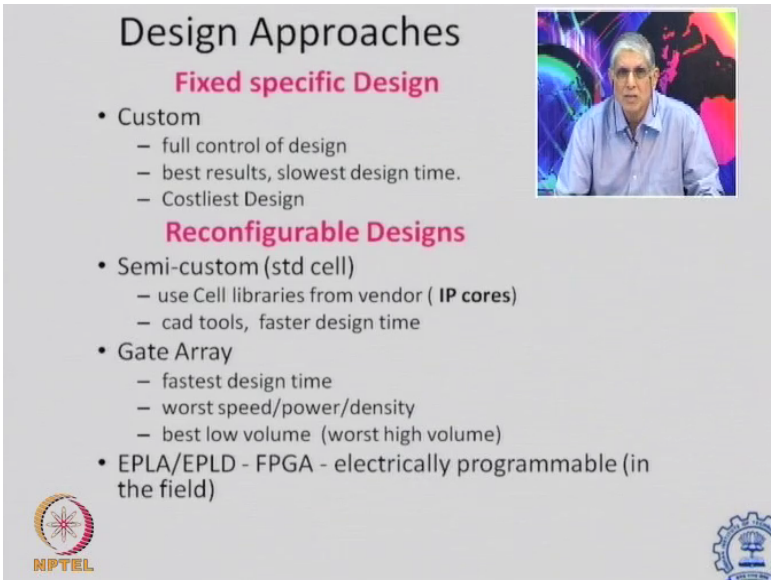


So what are the new design methodologies, the new methodologies now based on system level abstractions versus device characteristic abstractions, logic structures and circuitry change slowly over time you know they change over the time, so you need to do trade-off due to this change but choices do not, the unfortunate that you may have to change trade-off will change but the choices are very limited and therefore it is become very difficult whether you should do system level abstractions or you should do device level abstractions.

Then you should also now look for designs which are technology independent essentially what we say scalable designs require design a chip for 65 nanometer by 0.7 if I make 45 nanometer so might design should automatically go to 45 nanometer, so unfortunately the layout techniques also do not change as fast as the scaling, but the minimum features size is steadily decreasing with time.

And also because of that for technology nodes the voltage going down, die size is increasing since these are the bad points which are happening but we need layouts are not really working as improving as fast the scalability is an issue which one has to take into new designs. So there are number of way the design can be approached and there are two ways of doing most popular being the second part but let us start with the first one.

(Refer Slide Time: 53:56)



The first design procedure or method is fixed specific design which is essentially is called custom design, a customer gives the specification he gives the money that this is the money I have, these are the number of chips I want and they must perform to this specification this is called customer requirement, for example a video game chip, a video games for kids may require some kind of video kind of processors which can we need not be very very fast in all areas.

But at least the video should be good enough because I cannot do more better than certain seconds to milliseconds to retain the figure, so you can use those kinds of things in many such applications, so one has to see that a user or a customer decides this is what I want, for example a space scientist or a space engineer in ISRO or a NASA he may say I want a processor which is 128 bit processor,

And should work at 8 gigahertz which should have a system speed and it should not consume so much power, so such specks will be very odd specks but he come out with it, but he may say

okay, I do not mind the size the chip, because then probably something can be met and therefore this essentially is called full control of a design occurs in custom you can get the best result.

Because you are optimizing every time it actually is slowest designed time as element they are takes long time to designs the word slightly is misleading essentially what I meant was they are very slowest, slowing designs because you have to keep optimizing and it takes large amount of time before you get a correct one and therefore nutshell it is the costliest design available, but if someone is paying money for why not, okay.

For example, some of the official products like say microprocessor or memories chips they are sold in millions, so at that time probably a custom design is most obvious because that can make your advertisements show okay my I particular memory has access time of so much but has larger density of so much which is better than available memory in the market, so you probably will like to improve the specification to stand in the market for official product.

And therefore they need full custom design, the advantage of learning custom design is obvious because even if you are doing what we call the second area of reconfigurable, one has to use the same techniques of custom design to create what we called semi-custom blocks and therefore as a VLSI design course people I always insist on teaching custom design to most of the students, because once you learn how to design a block or a chip or a part of the chip.

Then you can reuse in any number of times in a modified form or otherwise but you should know how to get those blocks unless of course you are working in an industry which are all such blocks are reassigned to you which not many industries are every time can provide. the second area of design approach is reconfigurable which is the most popular essentially because of economics, it has very popular areas known to you this one is called semi-custom based on standard cells.

The basic idea in standard cell library is or now what we call IP cores which is essentially generated by the manufacturer okay or called vendors, these vendors will provide you the schematics and the performance of every block they have designed, fabricated and tested, for

example he may give even a simple NAND gates three layouts it may give a three driving capabilities one million, two millions, ten millions.

So each will be one IP core with different layouts strategies, different capacitance available, so each in such cell which is predesigned, prefab, pretested for its performance is guaranteed by standard cell people and that is why it is called standard cell and once you have such a library of such standard cells in the schematic form the best idea is to use those blocks call it a masks, call it decoder or call it arithmetic unit or whatever blocks you have you can just connected by placement in route techniques which can be automated.

And then you can get a system auto fed as fast as what you are looking for and you can then test it for its performance, since you are using already designed blocks a number of ways only you and doing almost automated placement route systems of the creating a system this will be very fast in design time and because of that the amount of money relatively used for designing of a system will be very small compare to the custom design.

The other technique which is slightly get which is not so very popular now possibly because of the other systems have become equally cheap is the Gate array, gate array is essentially number of layouts, number of transistors put in a standard layout forms and all that you need is to create a mask, a metal mask to give interconnection to create any different system, they are of course the faster in any design time you can create the chip in hours' time.

However they have the bad part because the standard (()) (59:26) size transistor put in a fixed layouts they will have not necessarily the best of speed may be sometime the worst of speed, worst of power and worst of density as well, because they are limited by everything because you have predesigned the best ideas that you are already prefabricated all these transistors everything on a layout on a particular structure only thing you left for a people for design is to put the metal interconnect mask for a given system performance.

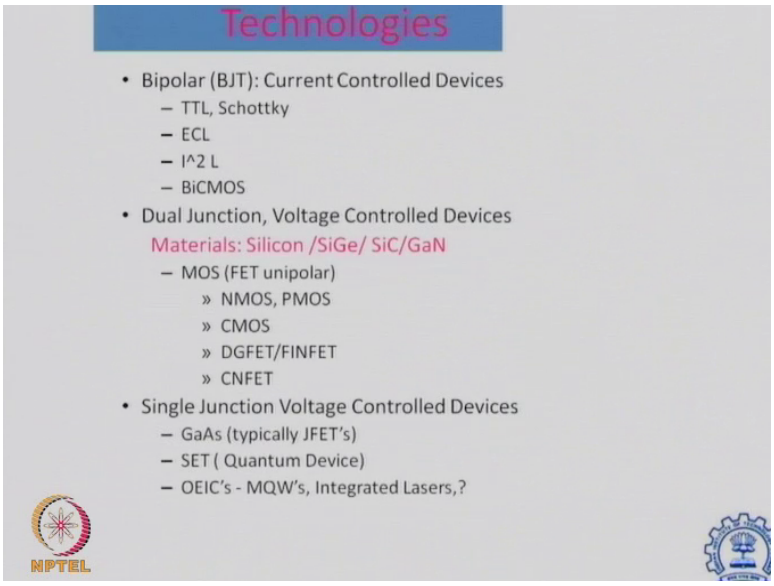
And since the wafers are ready all the time in numbers, 100 numbers, 10 numbers or 200 numbers, even small numbers can be used and then you can actually put your design in a very

short time, since it gives you very fast design it but and also can give very low volumes it is very popular with small electronic product people because it gets the output of a chip in a smaller time and smaller money however they are not the best in their performances.

The other possibilities is to use electrical programmable logic array, electrically logic devices and the most popular among these based on these are FPGA's which are electric programmable in the field that means at the user end you can actually connect them, so basically nothing is really fabricated as of now chips are anyway fabricated and you can electrically program them to create a system.

So these are popular design approaches to put a system on a chip and that is what people are actually looking in a design course. If you look at the available choices for designing a VLSI, so the first and foremost technology we started the all integrated circuit progress was bipolar.

(Refer Slide Time: 01:01:22)



They are essentially current control devices the kinds of technologies available from them were TTL, Schottky TTL then Emitter Coupled Logic ECL, I square L and finally BiCMOS, however decently heterostructures have comeback and using this heterostructures you may have a dual junction, voltage controlled devices even in bipolar area and they may have probably start computing in some sense beyond more area of silicon technology.

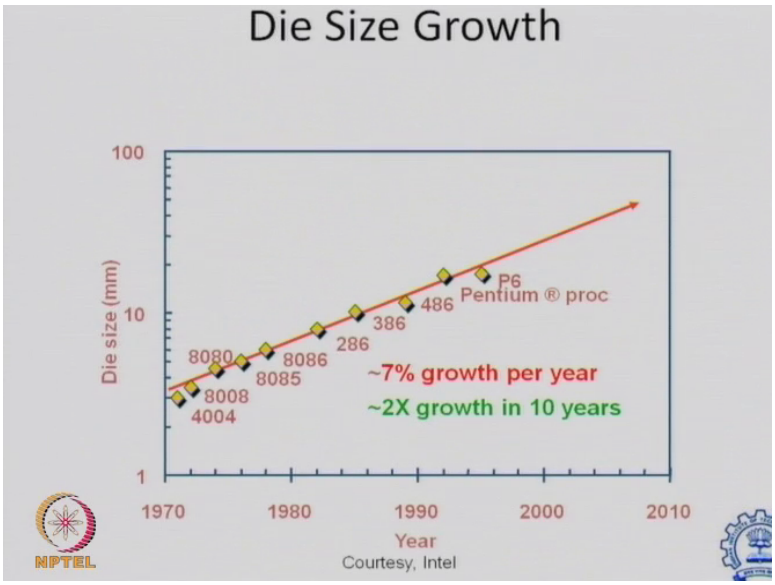
The other technology areas which is more important for us is for example MOSFET's are essentially from the dual junctions side and they are mostly voltage control devices, the materials which probably we have been working all through last 40 years silicon project will remain silicon for many more years irrespective whatever people say.

The other alternatives tried and being tried at least partially on with silicon technologies silicon germanium, silicon carbide and very off late people are also looking into gallium nitride, the devices used essentially are MOSFET's typically of those kinds are NMOS, PMOS or Complementary MOS we have modified these transistors now from simple MOSFET to what we called double gate MOSFET or FIN kind of surround gates FINFET's number of FIN's of gates.

And people are also looking into similar device in which the channel is connected by carbon nanotube and therefore they are called CNFET's - CNFET these are dual junction devices, however there is an attempt now going on to go beyond more as I said and we are looking for single junction voltage controlled devices similar like JFET's okay, the other devices JFET's are normally tried with 3, 5 compounds.

We are also looking for single electron transistor which is a quantum device and another effort going on this area is Optoelectronic IC's or Quantum lasers based Integrated lasers or quantum world devices and these are the essential part in technologies which probably make then integrated in to an chip and may we create even different times of combination of functions like you can have an optical block along with silicon - along with electrical block together working for an optoelectronic product.

(Refer Slide Time: 01:04:00)

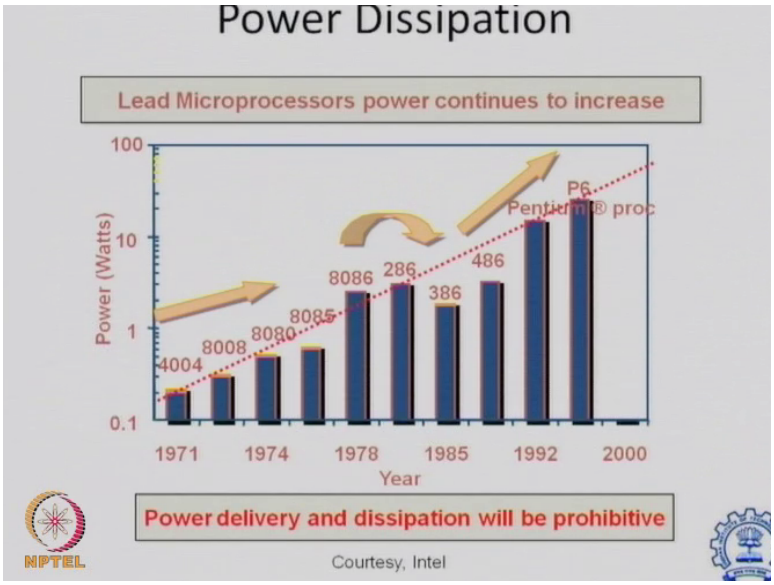


One of the major worries over the years is the Die size growth, for example in 70's we have around 4 mm square area when we started but in 2010 we are talking about 2.5 centimeter by 25 centimeter, so it is almost double its growing twice every 10 years or one can say it is 7% growth per year, since the question is always ask that the like say Pentium Proc Pentium's P5 P6 there are millions of transistors.

So what made people not to have a larger die size in 70 itself and could have put larger number of transistors, the reason why one has to worry about the area then was the silicon technology or silicon material technology was not very good, we could not do produce is this wafer which is defect fully for a larger areas and since it was impossible to create single crystal silicon large area wafers with uniform properties one has to restrict to at least get some finitely a smaller chip area of the order of 2 mm by 2 mm.

So that at least out of a wafer of 2 inch he may get at least 20 or 200 or 300 good chips and may be 600 not working good chips, however as a technology of silicon growth is improving over the years we can go now larger area chip and therefore over the years the areas of die started increasing and I say we have right now working on two and a half centimeter by two and a half centimeter and I am not sure at the end you may have actually even 4 mm – 4 centimeter by 4 centimeter chip later, you can see die size growth 20% to satisfied Moore's law, okay.

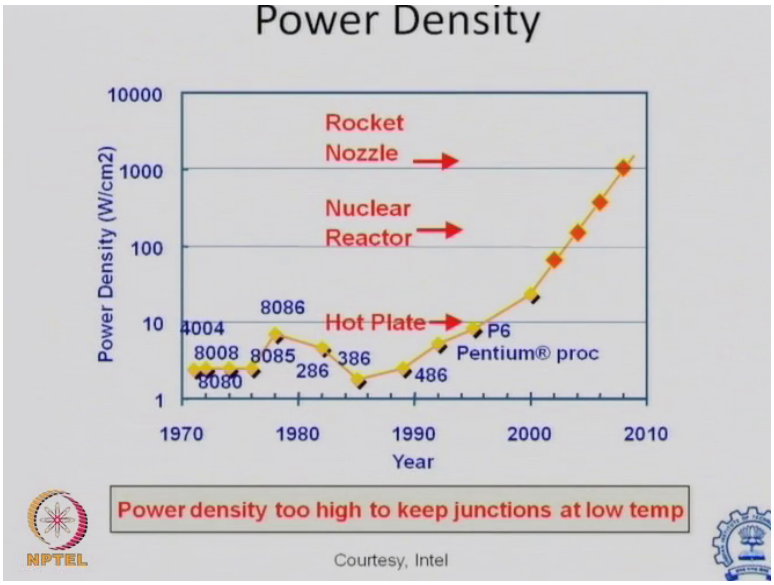
(Refer Slide Time: 01:06:03)



If you see a power dissipation over the year which is another constraint of VLSI design is the power against the years I have plot it which is also an Intel slide, we can see initially from 4004 we have a few microwatts of power milliwatts of power consumed to a Pentium 386 is relatively low power, we change the architecture to some extent from 286 to 386 and when it went to Pentium onwards again power dissipation increases normally.

And you can see from here the power dissipation is increasing over this and the consequence can be seen from here this is one slope, this is another slope and this is the third slope and I say what it is trying to do for us now this is an next slide of my, if you continue to work on this the power delivery and dissipation will be extremely prohibitive and one does not know how things can be managed.

(Refer Slide Time: 01:07:02)

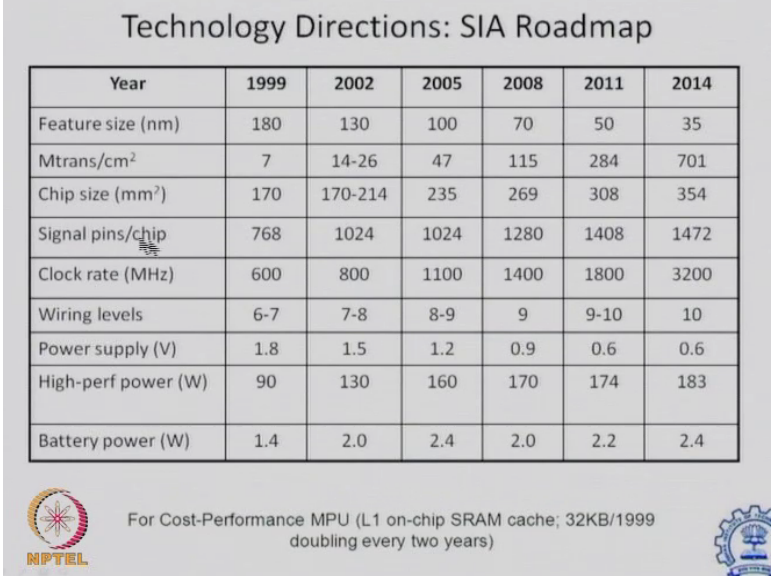


here is the figure here is the graph which actually says what I just now just said in the words, I have a power density watt per centimeter square against years, the P6 which came around 98 kind of time or 90's to 98 it has a power density of typically of the order of tens of watt per centimeter square which is like a Hot plate.

In 2006 or 7 we have now chips which are available which has the temperature such that the power density is around 200 watts to 300 watts per centimeter square which is the kind of power density in a Nuclear reactor and if you continue to improve the chips whatever number of transistors to put higher and higher the problem will be that the power density will rise to 1000 watts per centimeter square.

And of course this red marks therefore I has only put red because they are trying to improve on that but if you continue on this what we started in 2004 we can see the temperature may rise as much as to Rocket nozzle and at those temperatures take from me the silicon will actually evaporate, so power density is too high to keep junctions at low temperature is the major worry and therefore any designer must take care that the heat removal is the major important design issue which should take care in your designs.

(Refer Slide Time: 01:08:37)



This is called a road map coming from ITRS from semiconductor industry associations over the years from 1999 to 2014 release of course an old slide from them, some numbers have been modified later beyond 2008 but it is fine we expected 180 nanometer we started 180 nanometer 0.18 micron in 99 and we believe that we would go to 35 nanometer by 2014 but you have a measurement we are already working in 2012 on 28 nanometer process.

And by 2014 probably will work on 16 nanometer or even 11 nanometer process - features sizes. The million transistors we were looking for 7, so many transistors per centimeter 79 and we are already crossed 700 million transistors we already have a billion transistors circuit now, of course this is per centimeter square so I do not know exactly if I divide probably we are yet to reach this number.

The chip size we restarted with 170 mm square okay which is around 2 mm, 1.1 mm by 1.3mm kind of structure and we are now looking for area which is of the order of as I say 2 centimeter by 2 centimeter or above, okay. Number of pins we could then put 768 pen chip and now we are looking for 3200 pins, so you can think what kind of level of complexity road map is asking for.

The clock rate was 600 megahertz earlier and we are looking for of course this is slightly odd because we already crossed 3.2 gigahertz, we already reached 4.8 gigahertz clock rates. wiring

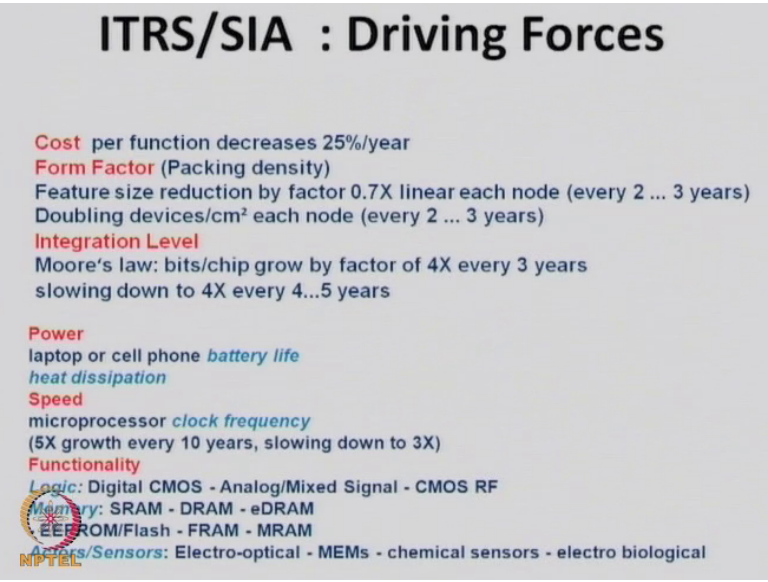
levels the interconnect levels on a chip were 6 to 7 earlier and we have already crossed 10 number, we already on now 12 to 14 interconnect levels are available.

Power supply, so one can see from here what we predicted in 2000 something we already crossed the performance what we thought done and what is now available, if you see power supply 1.8 volts we already reached 0.6 volts in many chips, however not all microprocessor chips but some chips we are made of 0.6 volts supply.

And the higher performance power has reached 180 watts here we are trying to reduce it but I think that is one major worries one of the thing while we are not going for very high performance circuit is because of this voltage, once this thermal problem is solved one will be able to reach both the frequency and power and requirements.

And the battery which supplies we are trying to put better batteries which can deliver larger voltages on a smaller area, particularly we are looking a microprocessor unit at least there is few L1 cache on SRAM 32KB now every double year this cache is (()) (01:11:29), in 2012 there is already megabits of SRAM processor or cache available on the chip itself.

(Refer Slide Time: 01:11:39)



So what are the driving forces as far as the International Technology Roadmap people which is essentially because of Semiconductor Industry Association driven, so these are driving forces for

example we see the cost per function must decrease 25% every year, it decreases in fact. The packing density or what we call form factor the feature size is reducing by you stand by 0.7X every node, now of course earlier it was every 2 now every years 3 years, okay.

And therefore the devices are getting double per centimeter square at every node though node may actually come in now not every year but every 2 years or every 3 years. Integration level if you see by Moore's law bits per chip grow by factor of 4X every 3 years and we may now slowdown that instead of 4X it may become 4.5 something in 4 to 5 years instead of 3 years that maybe become 4 years or 5 years it may slowing down now.

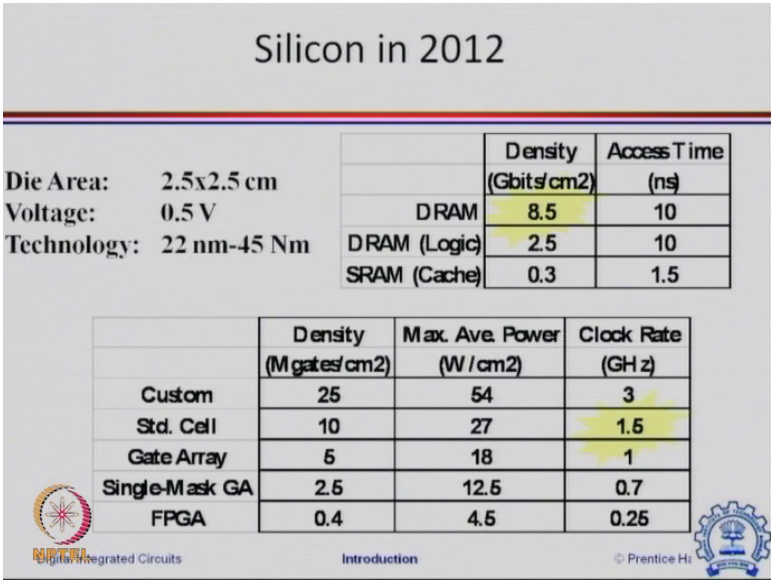
The reason as I say is the heat is the major worry and if you can solve the thermal problems I think much of those can be even better electrical performance is guaranteed, if you look at the other side which is the power side particularly for laptop or cell phone or any handle system the battery life and the heat dissipation are the crux which is worrying us most. If you look at the speed microprocessor clock frequency, we have a 5X growth every 10 years.

However, it is slowing down in last few years so it is now only 3 years growth every 10 years. if you look at the functionality the logic, if you see Digital CMOS, Analogue mixed signal and CMOS RF all three areas are now covered by Digital CMOS, logic is available for all three of them, if you look at the memory SRAM, DRAM and Embedded DRAM's are coming in to it, added with E square PROM Flash and Ferroelectric RAM's and Magnetic RAM's are also possibilities of memories.

And there are Actuators and Sensors are another area of interest where Electro-optical MEM's are being tried chemical sensors, electro biological sensors and actuators are being tried using semiconductor technology to a great extent. So one can see when I am working on improved things I am working for cost, I am working for form factor, I am working for integration level, other driving force are speed, power, functionality and what I can do.

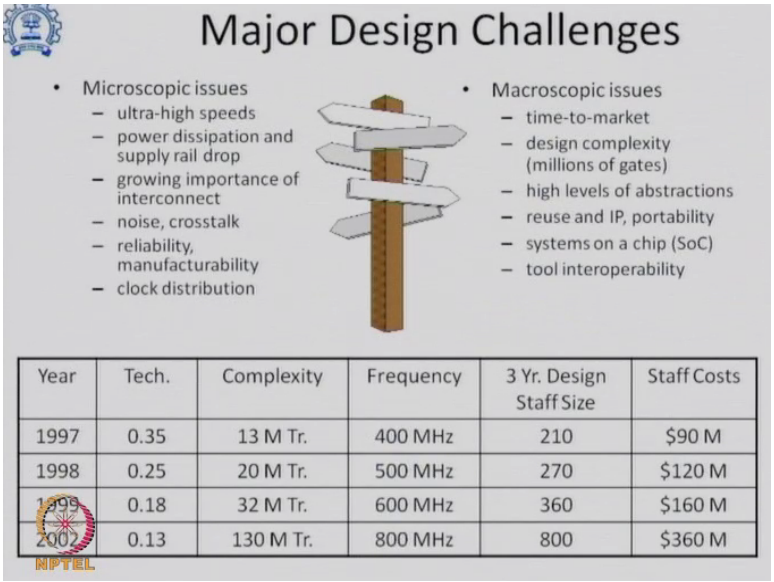
And therefore the SIA or ITRS every year describes what next and I think people are actually go seriously to follow what ITRS or SIA wants.

(Refer Slide Time: 01:14:35)



This is an old slide we are actually improving technology from 45 nanometer, 25 nanometer and voltages may go to 0.5, we may look for 8.5 gigabits per centimeter and DRAM's and access time of 10 nanoseconds or lower later, for a custom, standard cell, gate array, single mask GA, FPGA these are the clock rates we are looking for, we may look for FPGA's with one gigahertz sooner or later, so that you do not have to go every time for fill silicon solutions, these are the important milestones.

(Refer Slide Time: 01:15:13)



So what are the challenges we are facing, the microscopic issues, ultra-high speed, power dissipation, supply rail drop, growing importance of interconnect, noise and crosstalk, reliability

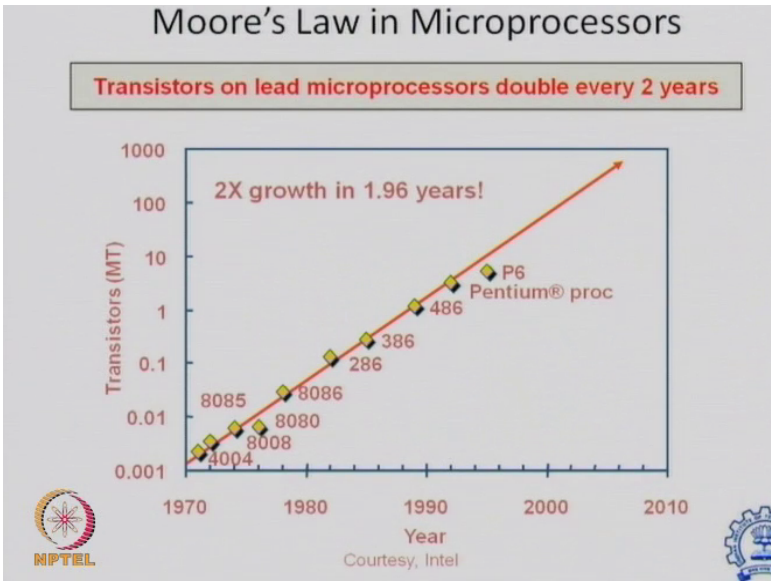
and manufacturing and clock distribution these are the microscopic issues. And if you look at the macroscopic issues, there are major issues in design is when to market your chip, time to market is very crucial for any success of design.

How much is number of gates you are going to use or what we called design complexity, what is the level of abstraction you can start design which is very important to the save time as well as money, how much reuse and IP and portability is possible and whether one can use system on a chip approach to improve the design to get the design faster and as good as possible on single chip and whether the tools used for all of them is inter portable for technology or any level of hierarchy.

So typical one of the major worry which we are seeing right now, this is an old slide I still wanted to show you because I do not have recent data, in 97 we were working on let us say 0.35-micron technology and staff cost the frequency was at complexity of 1.3 million transistors, staff cost was 90 million dollars, by 2002 we were working on 0.13 microns process, 130 million transistors ten at least hundred times we improved.

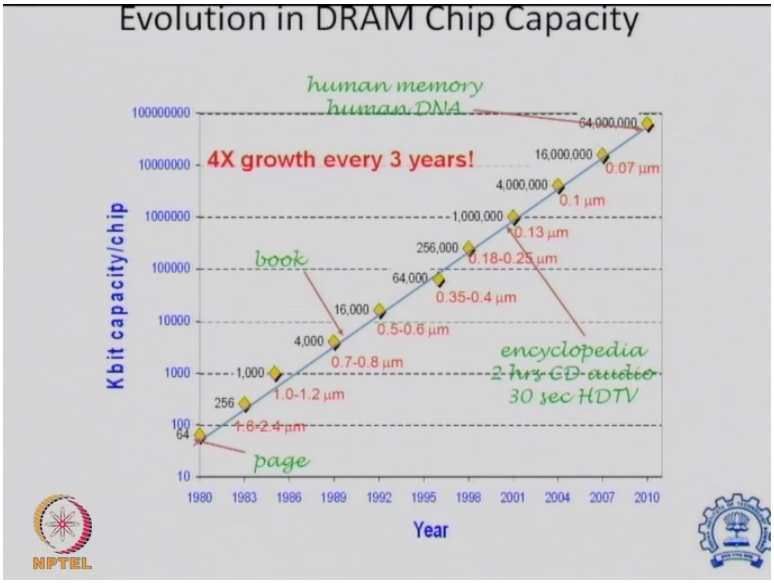
Frequency went from 400 megahertz to almost around a gigahertz, let us say 3 year design staff size is around you require now from 200 people to 800 people and because of that the amount of money you will spend is 360 million dollars, so essentially the cost of making chip itself is also increasing because of the staff cost you are increasing, so when I say that you do inter portability or system on design or reuse of IP essentially we want to reduce the staff cost because the design time then can be minimized.

(Refer Slide Time: 01:17:27)



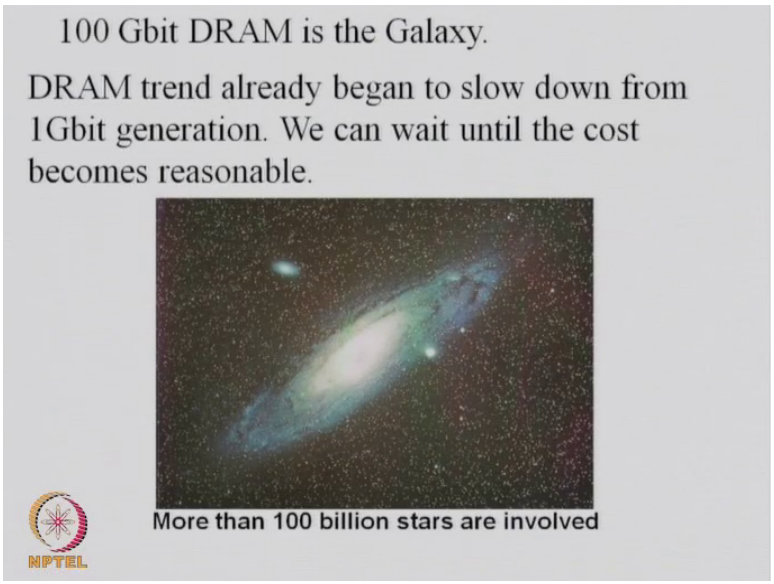
This is standard Moore's law which I already said, transistor on lead microprocessors double every 2 years.

(Refer Slide Time: 01:17:32)



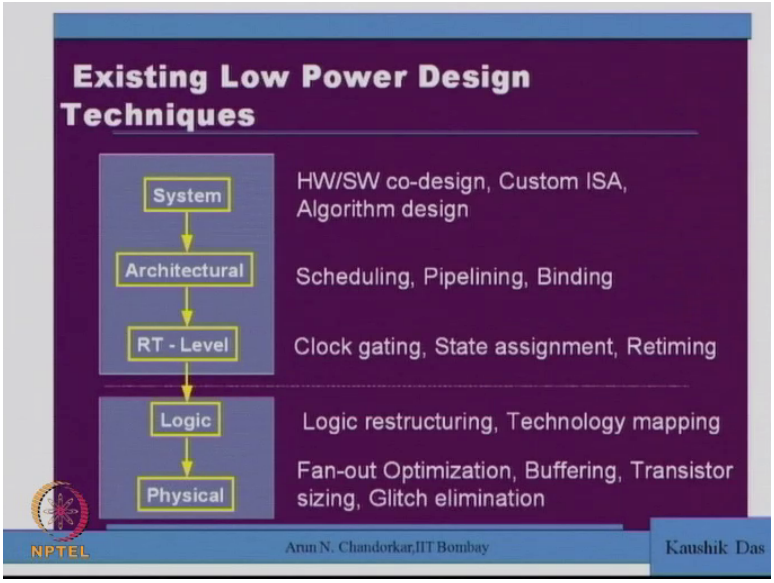
This is DRAM chip, we already 64 gigabits of DRAM possible in 2010 though it is not really marketed by 45 nanometer, but it is growing every 3 years 4 times every 3 years, this is equivalent of a page something written on a single page of a book, this is something for equivalent of a book which is around 4000 kind of bits, then this is 1 million or something is encyclopedia and ultimately we are looking for memory is equivalent of a human DNA, this is what actually driving us.

(Refer Slide Time: 01:18:14)



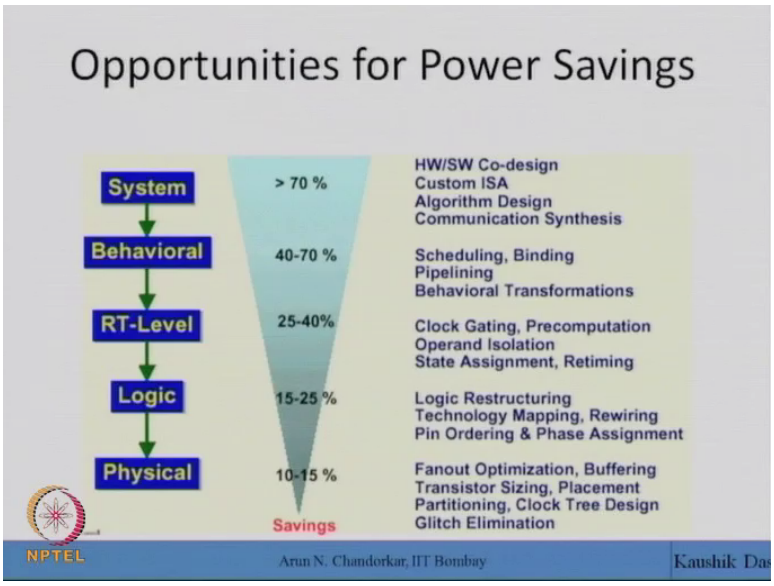
A typical 100 gigabit DRAM in a galaxy DRAM trend already began to slow down from 1 gigabit generation. we can wait until the cost becomes reasonable, you can see this is a galaxy which has hundred billion stars are involved and which is equivalent to saying a DRAM is right now is actually looking for 100 gigabits which is like a galaxy of memory.

(Refer Slide Time: 01:18:49)



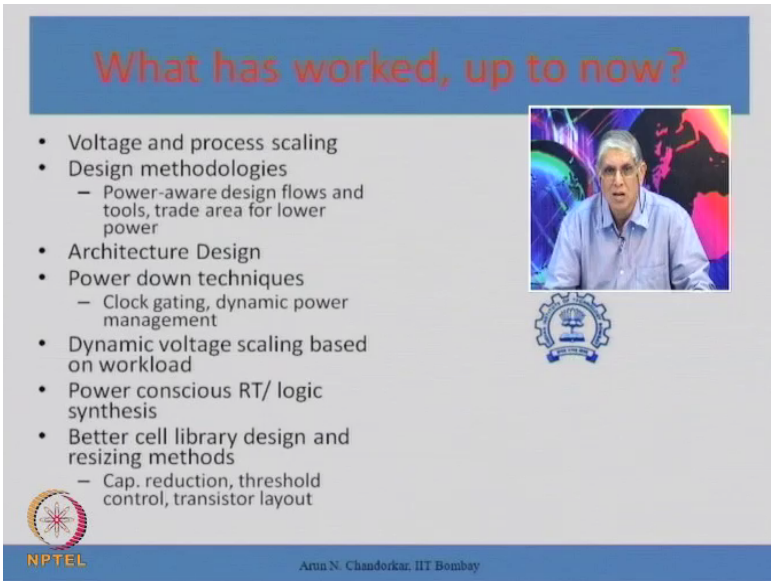
There are another effort because of the thermal issues and power issues we are looking for low power designs this is the hierarchy of design, I will discuss this more in detail when I am discuss low power design later, but essentially the level at which power can be minimized is at System level, Architecture level, RT level, Logical level and Physical level more details will come later.

(Refer Slide Time: 01:19:03)



And this is where the opportunities of power saving, the highest power saving probably can occur at the behavioral and system level and not so much at the physical level where 99% of effort is really going on the physical and logical levels.

(Refer Slide Time: 01:19:18)



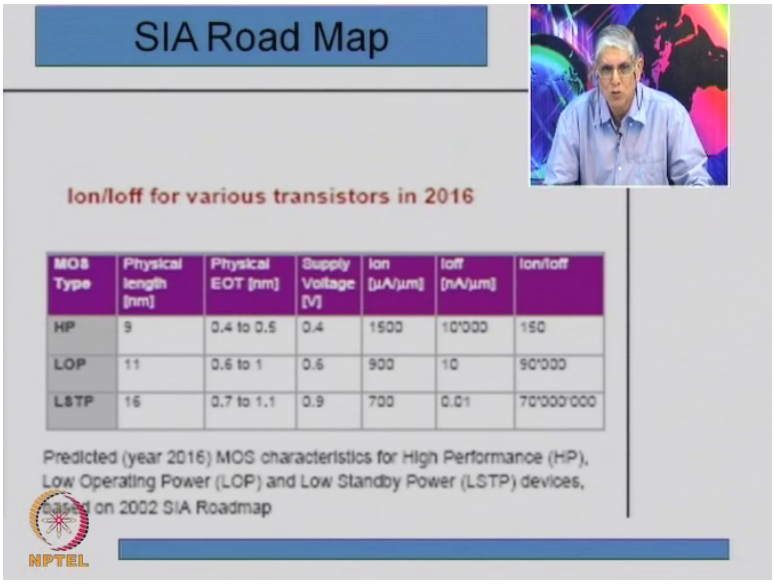
So what has worked, up till now we have been able to scale process that is feature size, we also are able to scale down voltages not to the Moore's law but at least we are scaling down, we started with 3.3 volts, 5 volts, 3.3 volt, 2.1 volt, 1.5 volt, 1.2 volt, 1.1 volt, 0.8 volt, 0.6 volt, 0.5 volt, so we are going scaling down voltages definitely.

Features we are definitely going in features size and there is no denying on that, we already reached 28 nanometer, 22 nanometers, 16, 11, 7 are on the way, the methodologies we are now looking into power aware design instead of just good design, we are also seeing that the speeds are attained, but at the same time power is minimized, there are trade areas for low power and newer tools are required.

Then we are also looking into we are able to manage many of the architectural designs and we need lot of effort to improve architectures now, we are also looking to reduce power by what we called power down techniques getting the clock gating, dynamic power managements, we are also looking for dynamic voltage scaling based on workload that is when to switch on or switch off outputs.

Then we are looking for power conscious RTL synthesis and we are also looking for better cell library design and resizing methods to reduce capacitances, threshold control and transistor layouts, something we have already worked on something needs improvement.

(Refer Slide Time: 01:20:50)



This is the kind of three kinds of circuits which as I suggest one must work on, the first one we called is High Performance circuit which are essentially performances speed, so high speed circuits require so much on current and so much off current ratio, typically 1500 microns per

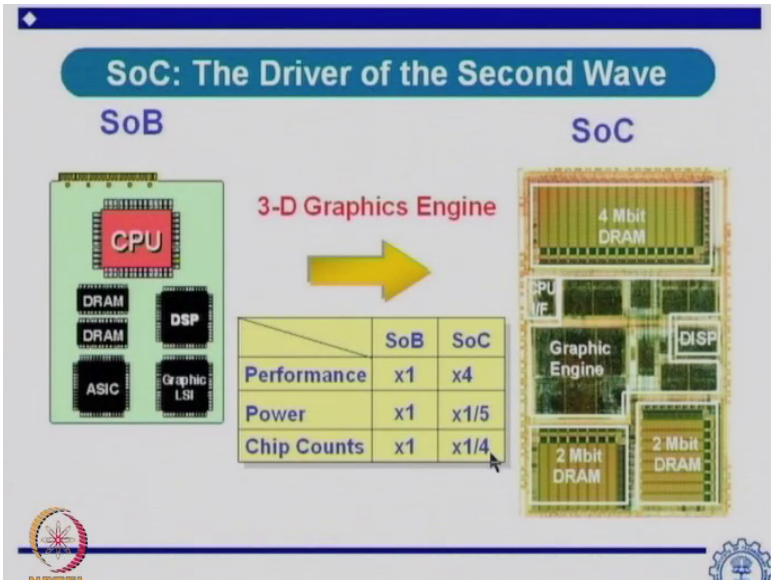
micron is the on current expectations okay, voltages will be as low as 0.4 volt, okay and the gate thickness will be equal and oxide thickness will be around 0.4 nanometers.

We are then the low power circuits which has a which may have a gate length of around 11 nanometers and however we are looking for ratio of 90 in that on current maybe slightly lower 10 compared to such a line number earlier 1500 to 900, then we are looking for Low Standby Power circuit like a mobile when you are switching you do not you keep the mobile fully off it is on, but not really working so it is called standby power.

And major effort for these handheld system is on LSTP circuits and there also we are looking for low power off current and on current like for 700 microampere is current 0.01 is the off current, so you are reducing the off current from 10 microampere microns to 0.01 microampere micron as we go from high performance to low standby circuits, so this is what we are to achieve by 2016 these numbers are not for today but possibly can be attained over the time.

The second wave which is now coming is what we called System on Chip and this is something we want to improve the design improve the rather fast on around the chip design, so we went from what we called System on Board.

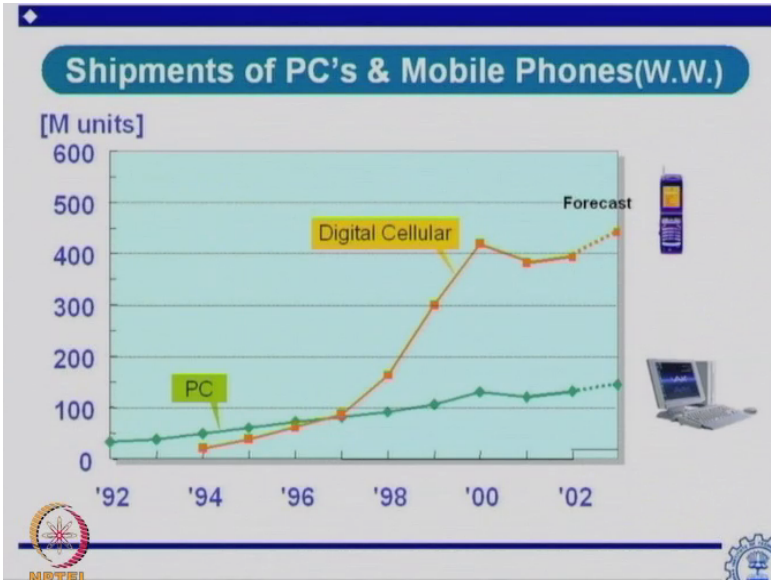
(Refer Slide Time: 01:22:47)



For example, on the your left you can see on a board you have a CPU, you have a DRAM, you have a DSP processor, Graphic processor, you may have some ASIC which is doing particular functions, so you can see performance wise SoB let us say initial level of 1X power performance chip and if I use this 3D graphic engine which is shown here on an System on Chip which is on a single chip putting all those blocks the way I shown.

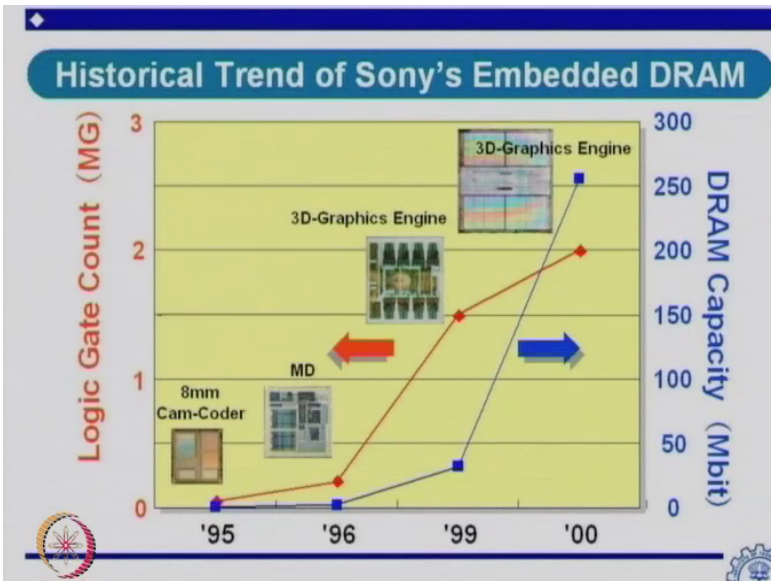
Then one can say I can improve the performance 4 times by speed essentially I mean I can reduce the power one fifth and I can reduce the chip count from says so many one to one forth, so one can easily guess from here that the new approach for design will be now based on SoC design, because SoC is somehow is someway reducing the power, improving the performance and also reducing the number of chips per centimeter square.

(Refer Slide Time: 01:23:50)



We can see over the years the Digital market over PC market has improved enormously and forecast is it will go to 500 million units sooner.

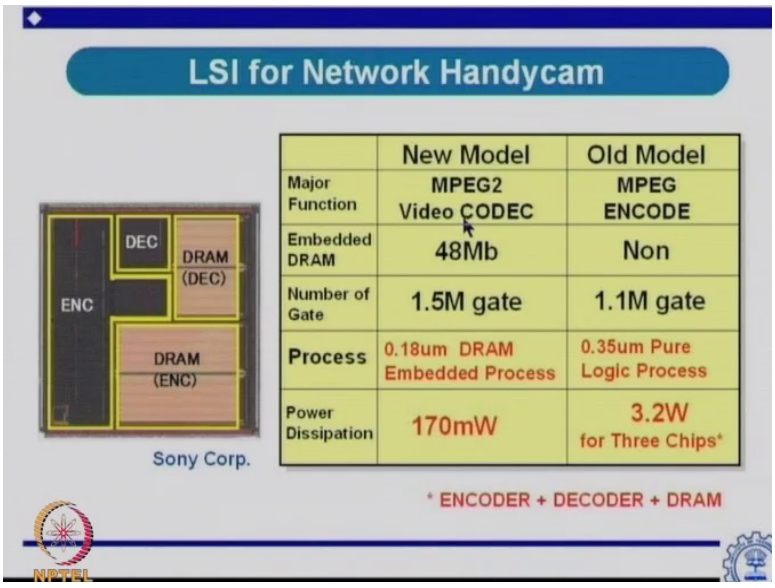
(Refer Slide Time: 01:23:57)



So Sony was the first make an Embedded DRAM way back in 90's and one can see it is improvement the left side is logic gate count, the other side is DRAM capacity and one can see from here somewhere around 2000 or 90 around 2000 the logic level count - logical level count is set 2 million gates but by then we already created 250 megabits of DRAM.

So we are already now we can see the DRAM technology, Embedded DRAM technology has cross the logic gate technology much more in a speed or better way and therefore future circuits probably will have to now take care that you have an Embedded DRAM which you can very interestingly used in your data flow and therefore can improve both speed and reduce powers.

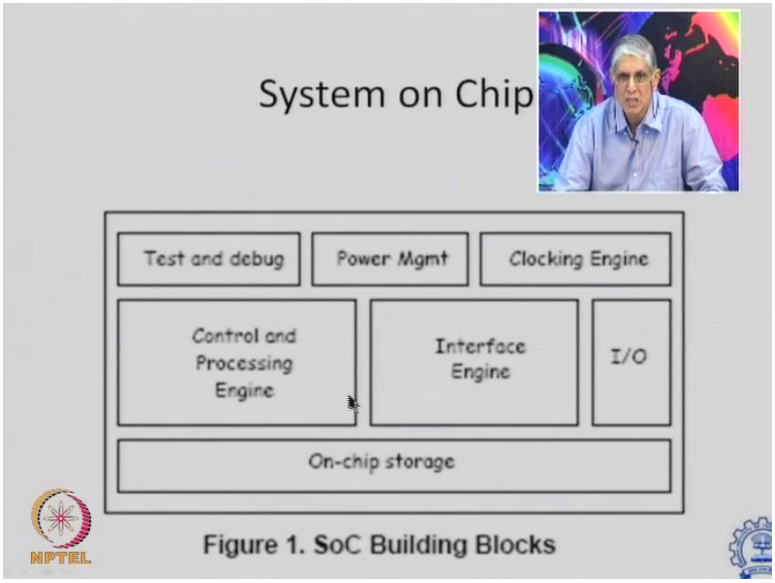
(Refer Slide Time: 01:24:51)



This is typically an Handycam of Sony, these are the blocks of Sony early handycam, and there old model has following things it was working on it consume 3.2 watts, it has am MPEG ENCODE, it has no Embedded DRAM, it has around 1.1 million gate, when they change over to Embedded system this using Embedded memories you have now video CODEC, you have 48 Mb Embedded DRAM, you have 1.5 million gates.

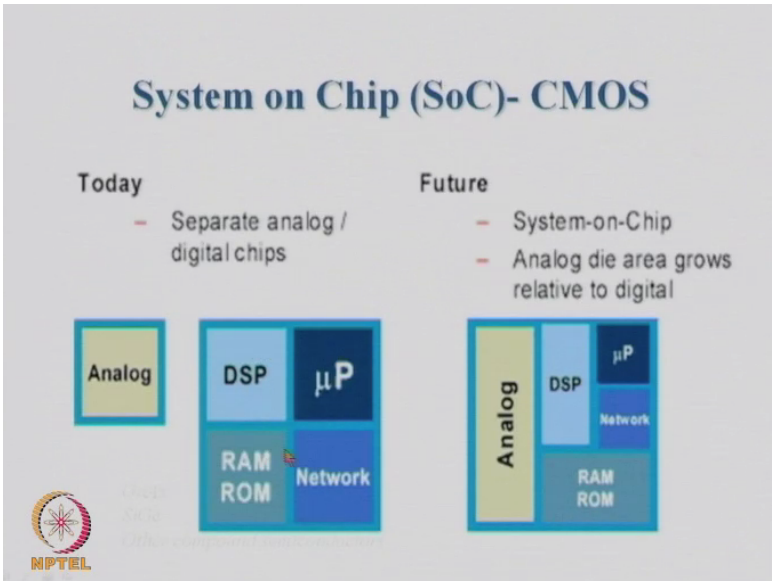
It is now we are working on that this is the old slide of the Sony because they do not give you newer slides, so it is a 0.18 micron DRAM embedded process and the power dissipation has reduced from 3 chips 3.2 single ship 170 milliwatts, so SoC is one of the panacea for better performance of the VLSI systems.

(Refer Slide Time: 01:25:43)



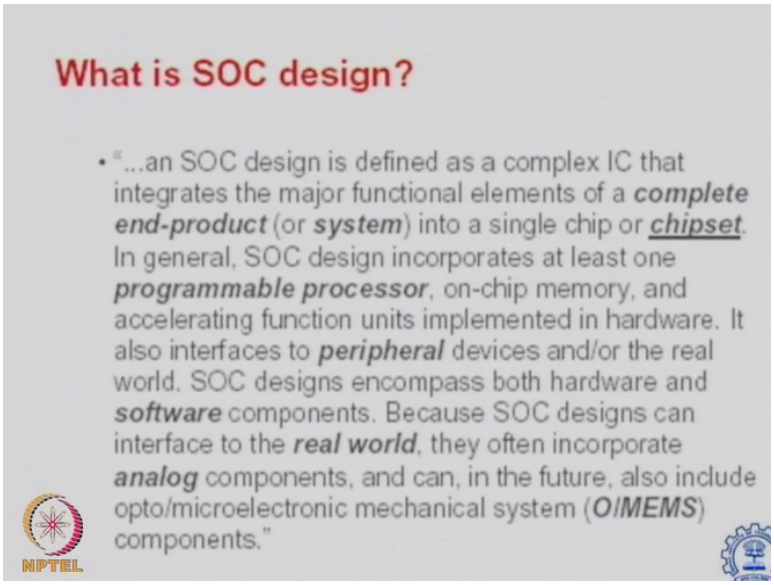
Typically, System on Chips have following blocks, you have a some kind of control unit, processing engine, there is a power management unit, there is a clocking engine, this is your interface and this is IO on chips storage memory and then you have test and debug on chip, so these are typical blocks in an SoC.

(Refer Slide Time: 01:26:03)



Here is some example again taken from Sony, this is an analog block which is separate, because analog circuits cannot be in those days put on the same digital technologies so you have a analog chip separated from digital chip which has DSP, Microprocessor, RAM, ROM and a Network and if you put it on the system on a chip analog in the same area, so essentially analog area has grown compared to digital but overall area is smaller than the earlier one.

(Refer Slide Time: 01:26:36)

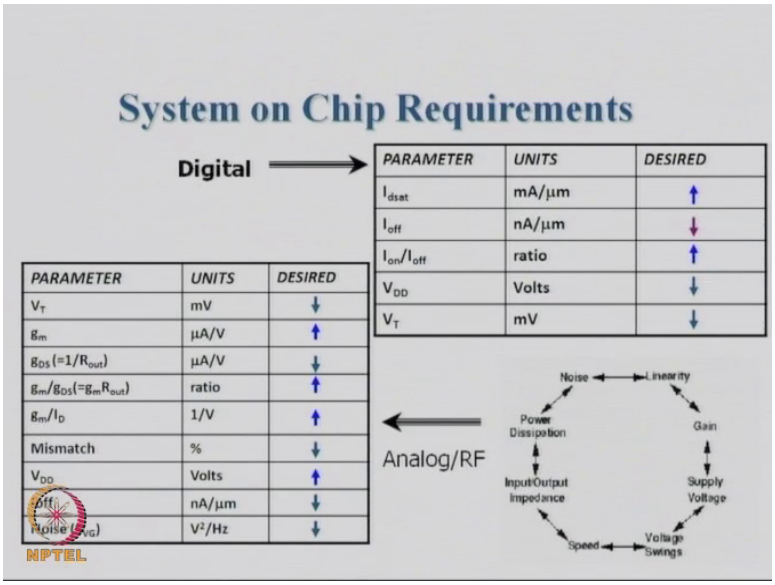


So what is an SOC design essentially, so let us read out and tell you what exactly I thought of it, an SOC design is defined as a complex IC that integrates the major functional elements of a complete end-product or a system into a single chip or then I call it chipset. In general, an SOC

design incorporates at least one programmable processor, on chip memory, accelerating function units which is implemented on a hardware.

It also interfaces to peripherals and or any other real-world device and it encompasses both hardware and software components together. Because SOC designs can interface to the real world, they often incorporate analog components and can in future also include any opto -microelectronic systems, micro electro mechanical systems on chip together.

(Refer Slide Time: 01:27:38)

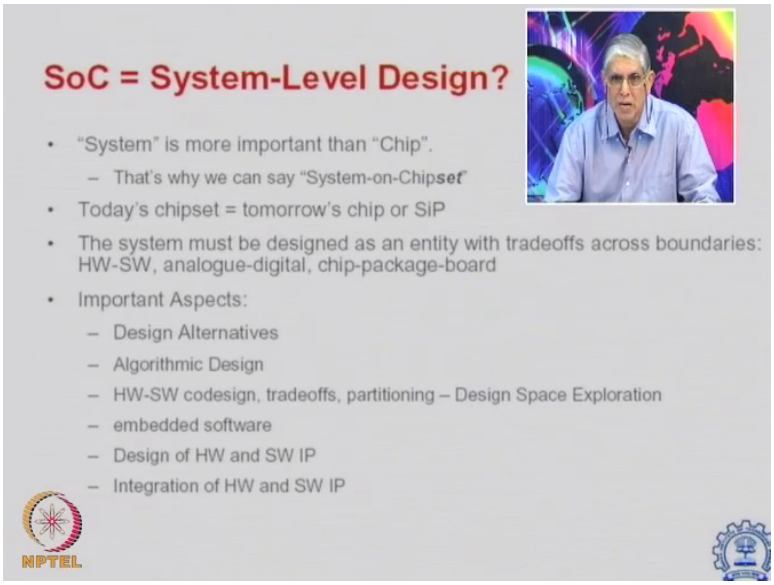


Typically, if you see a SoC requirement from the transistor point of view this is analog requirement, this is digital requirement and one can see basically in the case of digital we are looking for I dsat current that is on current, we want lower off current, higher on off to ratio, lower V DD and lower V T's or if you look at analog blocks you need low V T which is good anyway.

Then you need because you need larger g m, you need lower g o2 or larger R o, you want a ratio of g m to g o2 be very high for the gain, you want g m by I d ratio which should be very high and mismatch be less than very small percentage, you want higher voltage to operate because g m will be higher because the I dsat will be higher, okay and you want very small off current which is same as digital and you want practically no noise in the circuits.

You can say there are there is an hexagon for your management of this, in the case of digital you only look for power, speed and area, here there are more than 8 parameters you have to optimize but when you optimize better performance of analog or RF many of them are not same as required for digital and therefore there is a conflict and therefore something kind of a tradeoff between good performance of analog and good performance on digital has to be met, so that system on chip both can be implemented together.

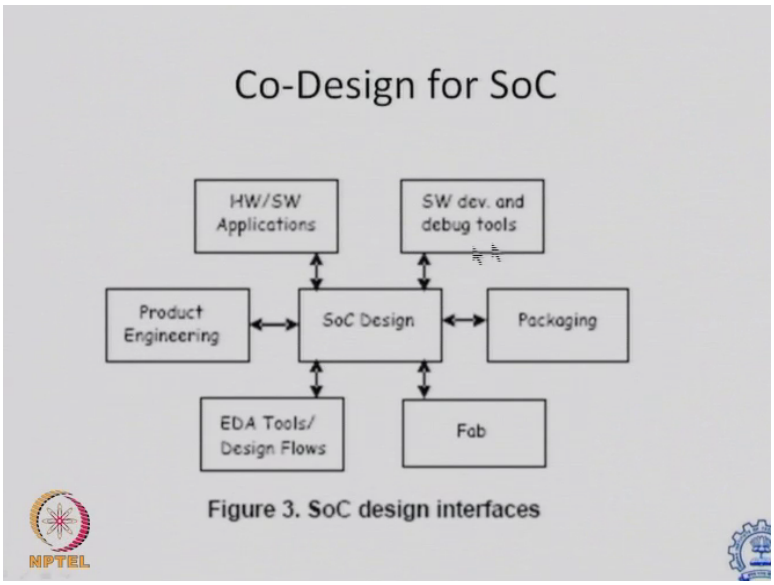
(Refer Slide Time: 01:29:11)



Please remember that System on Chip why so important is system is more important than a chip, that is why we can say system on chipset, today's chipset will be tomorrow's chip and more than such chips can become newer chips a newer chipset. The system must be designed as an entity with trade-offs across boundaries, and the important aspects therefore for a such hardware-software, analog-digital, chip-package everything has to be taken care in a system design.

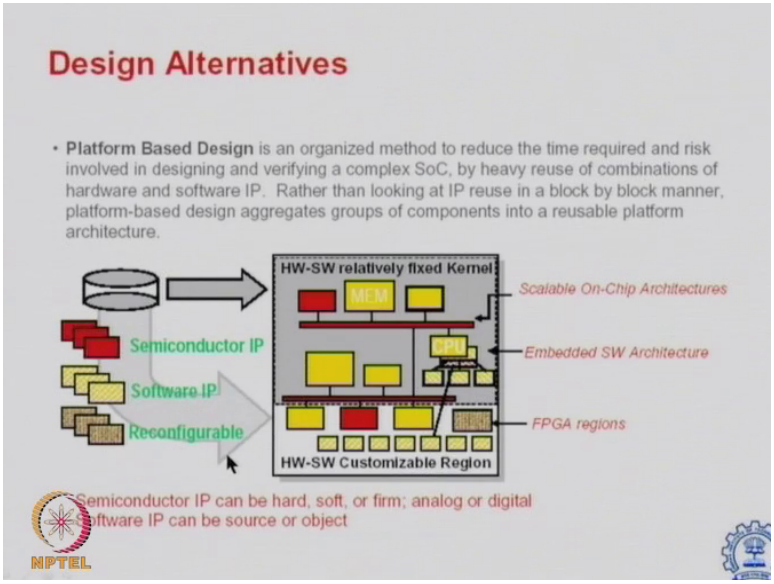
So you need to have aspects of design alternatives, you share good algorithm design procedures available, both hardware software co-design, trade-offs, partitioning, design space exploration has to be available to you good embedded software's must be available to you, design of hardware and software IP's must be known to you and integration of hardware and software IP's is also very important.

(Refer Slide Time: 01:30:03)



So when you do a co-design you have SoC design in the center, this is hardware software co-applications, this is tools available, product engineering, EDA tools, Fab, packaging this is how you interface.

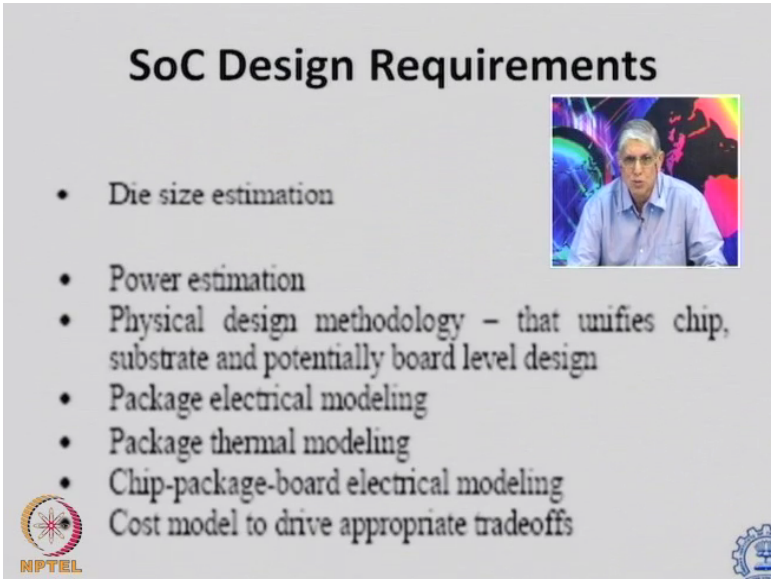
(Refer Slide Time: 01:30:16)



A typical in nutshell this slide gives you everything together what is scalable architectures, what is the hard copy, which is the software IP's, which are reconfigurable IP's, if you do all such things on a single chip single platform that will be an idealized ideal system and one can think of it now that semiconductor IP can be hard, soft or a firm, it can be analog or digital or RF software IP can be source or an object code.

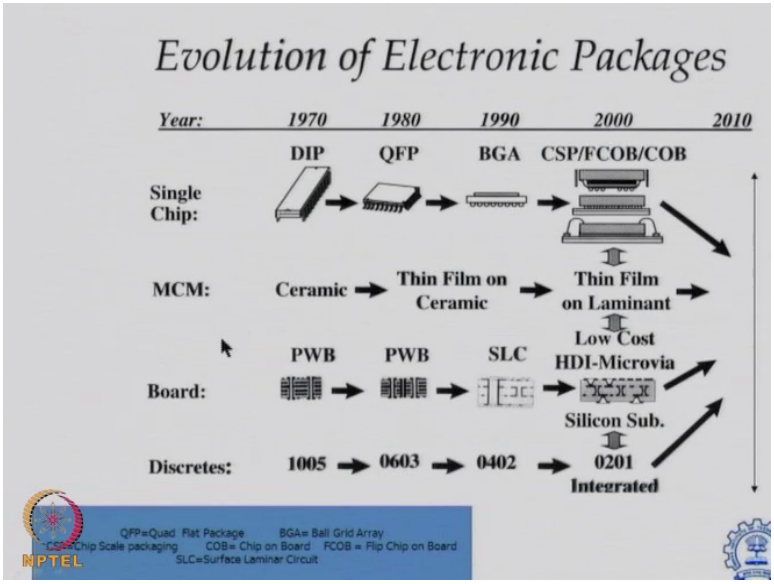
And if all of them is variable creating a system on chip will be much easier compared to any other way and therefore can make a complex SoC circuit or systems.

(Refer Slide Time: 01:30:57)



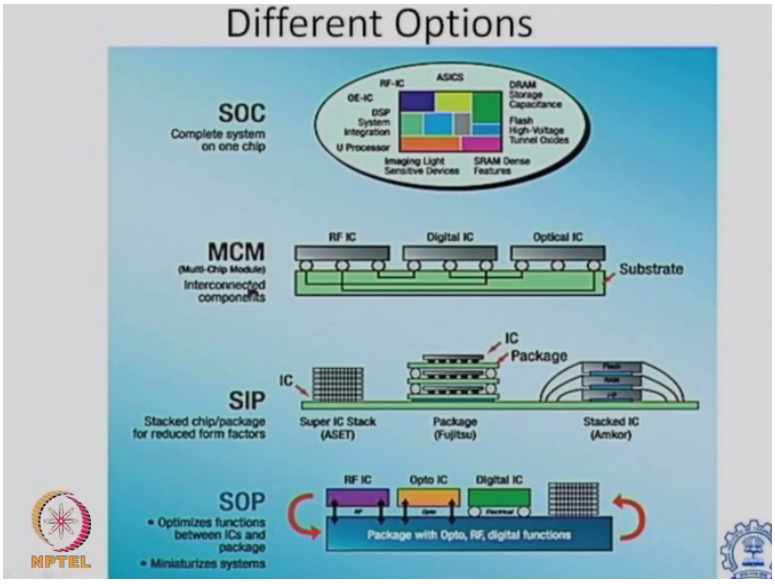
The design requirements are die size estimation, power estimation, physical design methodologies to be used, what substrate you are going to use, finally which board level design you are going to use, package electrical modelling, package thermal modelling, chip-package board electrical modelling, cost modelling all these are issues in SoC's. So one possible last option I may quickly run through is called design automation design option from packaging.

(Refer Slide Time: 01:31:34)



So for example we started with Quad packages of plastics, Dual in package, Quad in package and Ball Grid Array's kind of the thing as we started improving technology for a Single chip, we have Multi-chip modules, then we have Boards and we have now Discretes available.

(Refer Slide Time: 01:31:45)



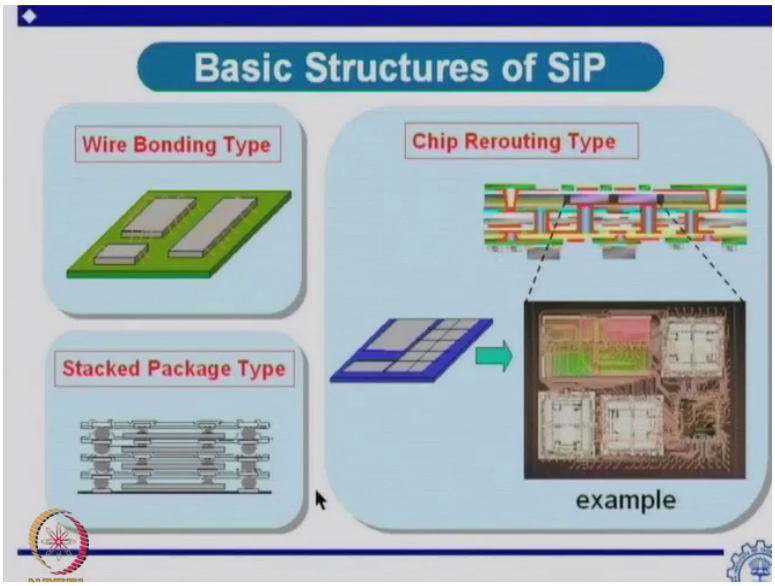
So now I can show you in this a typical SoC has all those blocks shown here, this is a complete system on a chip, one can have a different chip but you can have in a package you can have different modules bonded together are called multi-chips modules inside a package on a single substrate and these are ball grid array as we say, this is ball bonding and not wire bonding so to prove the resistance, small resistance and lower inductance.

Then there is another possibilities what we called System in Package, now this is stack what's you can have a number of such stacks number of chips available on single vertical package mounted one over the other and once you do this kind of this system inside a package you have now the total area of this package will be smaller, however the heat transfer, electrical connections everything will not very easy in this chip.

But it is being one of the major interest area of current do that you can make a good system inside a package by actually vertical stacking them and there is finally this System on Package is another area in which you can have number of chips and of different SoC's together can be mounted on a single package once again and therefore can create a very large system inside a

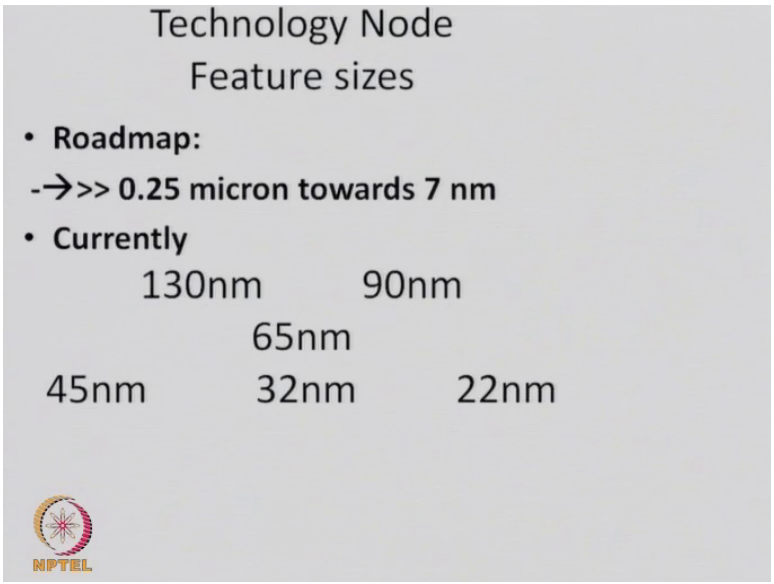
packages as in system on package, so this what essentially options we have in the packaging area which we have to succinctly used to improve a larger system VLSI design, okay.

(Refer Slide Time: 01:33:20)



I will skip this, this is typically what I said if this is your stacking, this is your wire bonding type, and you can see this is an example of a single chip and you can bond number of such layers 4 layers, 5 layers on top of each and you can make a system inside a package.

(Refer Slide Time: 01:33:46)

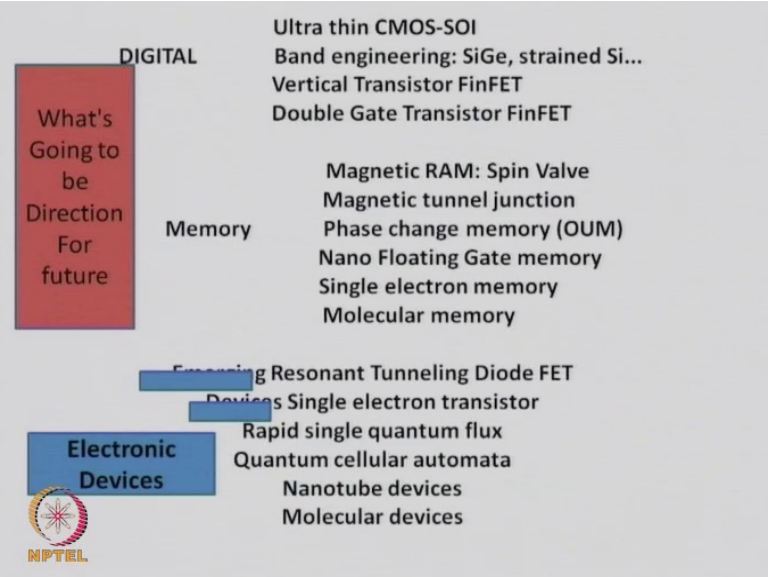


So at the end of the today's talk I may say you what is future for VLSI design the first thing is as per SIA road map says we are started earlier with 0.25 micron process in 99, 90's and by now we are expecting to reach towards 7 nanometer technology nodes which was a oxide thickness of the

order of 0.1 nanometer EOT, currently we have mostly working on 130 nanometers some chips, 90 nanometer some chips, 65 is still in the work hours.

Now recently last three four years 45 nanometer chips are major chips available in the market 45, the Intel processors now will be coming an 28 nanometer process which is essentially 32 nanometer node and there are also made other companies also made some chips you think 22 nanometers and as I say our ultimate aim is to reach 7 nanometers go on forward it should not become 0 nanometers.

(Refer Slide Time: 01:34:40)



So what's going to be discrete directions for future for the digital side one can see, you will have a different technology Ultra-thin, CMOS, Silicon insulator, Newer wafers, newer process of making chips will be found or rather available, but has to be improve much more, we will have to work on other materials of silicon related like strained silicon, silicon germanium we can do something on Band gap engineering.

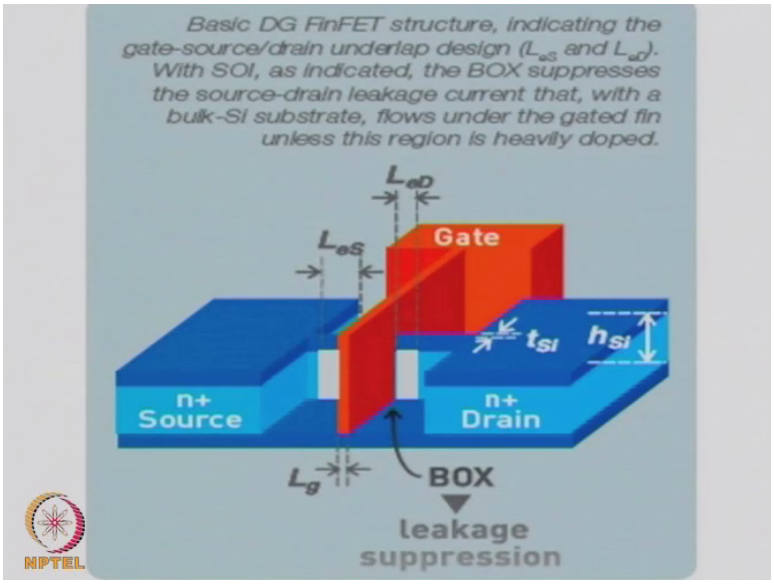
We also have to work with more with the FinFET's, vertical device, vertical transistor FinFET's, we can also work with double gate instead of simple mask transistor which we have been using so often, the basic transistor structure will have to change to FinFET's or any of the above using different technology.

The memories may become sooner or later Spin based Magnetic RAM's will have to be worked on Magnetic tunnel junction memories have to be worked on, Phase change memories these are non-silicon memories one has to work on, Nano floating gate memory are being worked on, the Single electron memory is being worked on and Molecular memory, so these are the areas in which research will continue on memory side.

And the devices side we may have an even more different devices to use Resonant tunneling diode, Single electron transistor, Rapid single quantum flux, Quantum cellular automata, Nanotube devices and Molecular devices, so these are the areas where VLSI design has to concentrate.

And therefore change the concept of design itself start looking into a newer models for newer devices, newer circuit simulations how to create better architectures and which digital technology to use and which memories can be used which have a different kinds of memories which consumes lower power faster access.

(Refer Slide Time: 01:36:35)

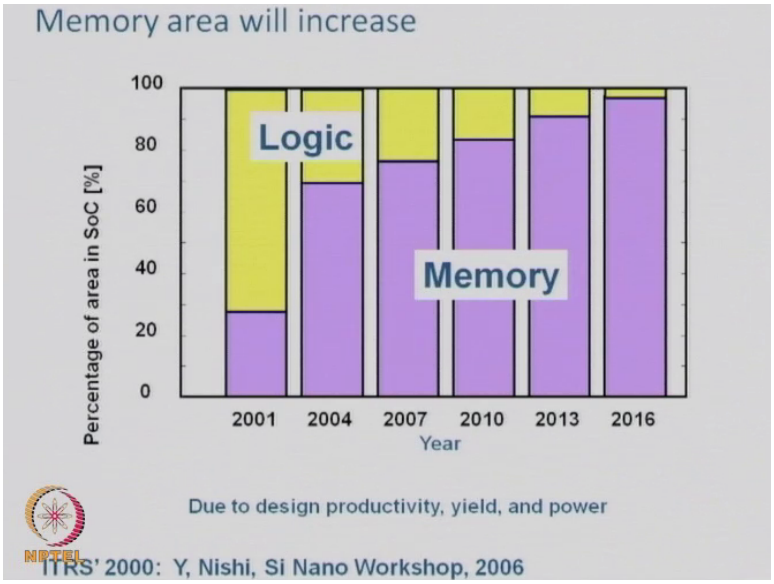


This is a typical photograph of a digital basic double gate FinFET structure which appeared in 2000 which is based on in a SOI technology and the advantage of this FinFET is that it improves a performance of MOSFET drastically and avoids many of the short channel effects which

normal MOSFEF faces when you scale down the device from say 10-micron channel length to 10 nanometer or to 1 nanometer or 0.1 nanometer kind of device lengths you are looking.

So the problems because of scaling which are appearing are called short channel effects they can be elevated partly by using double gate or multiple gate structure called FinFET's.

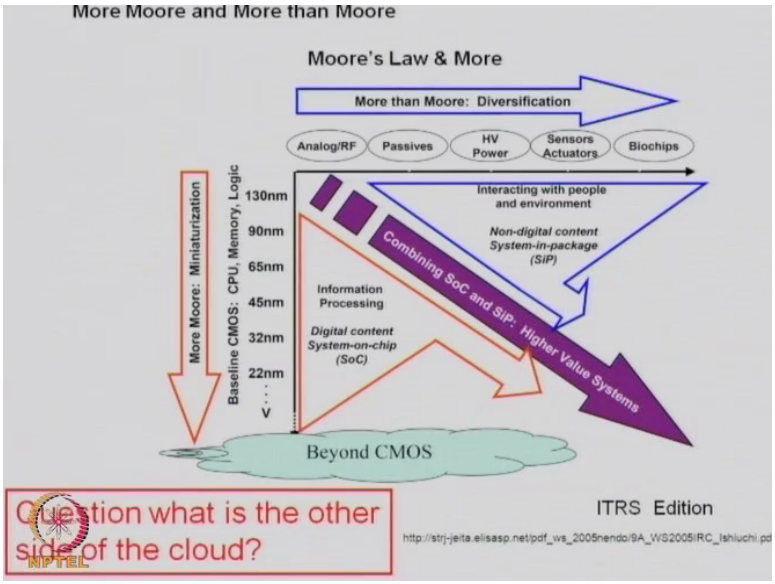
(Refer Slide Time: 01:37:20)



What will happen on the system side? is because we are improving embedded memory designs, we are improving memory technology as well, we more and more effort will be actually on improvement in memories and actually the logic part in the SoC will be comparatively reducing over the years. Because it will then we are looking really a three parameters now design productivity, yield and low power.

And these are the three parameters based on these one can see more and more logic more and more memory based designs will appear compared to the logic based designs.

(Refer Slide Time: 01:38:01)



At the end what is the wave Moore will look, if you see this horizontal line More than Moore diversification and this is More Moore miniaturization, you have the circuits of the kind analog RF, passive components, HV high voltage devices, then you have Actuators and then you have Biochips. Then on this side you have technology going from 130 nanometers down to 7 nanometers, lot of information processing in this triangle this area digital content system on chip on this side you have interaction with people and environment.

Because you are looking for biosensors, high voltage devices and mostly it is non-digital content of SiP which is on this side as you move. And this you have to combine SoC and SiP for higher value system and below this 22 nanometer cloud which we said beyond Moore we do not know what is the other side of the cloud and because of that what will happen on this side is also not very well known.

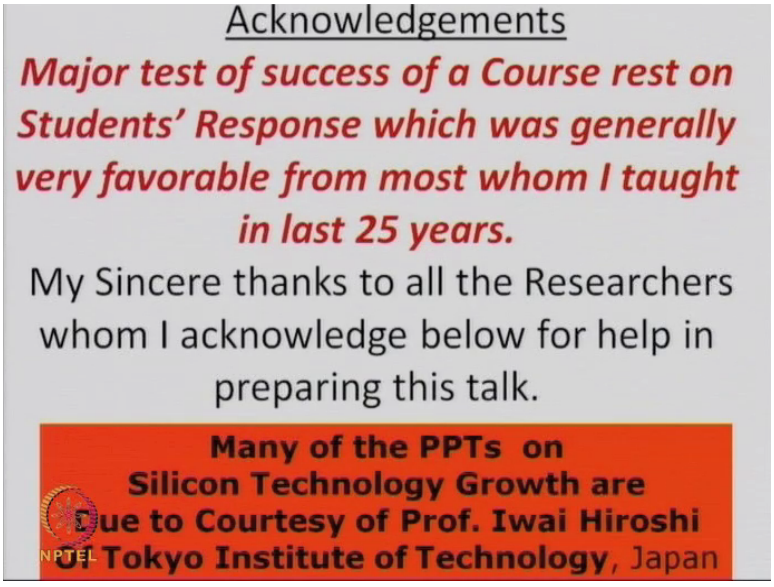
We hope that the research in VLSI will continue and I assure all VLSI design engineers who are taking this course and try to become engineers later in VLSI area. Till 2060 may be or at least 60 I would say at least 50 years then you will be productively employed in the VLSI area come what me I cannot predict much more than that neither I am competent and maybe I will not even see that day.

Because you cannot come to me than to say sir you said something and it has not happened. So 2060 is what I keep saying you are safe keep working on VLSI you will be not only paid well, but you will also get satisfaction of actually making things which are interesting and also useful. At the end of the course, at the end of this lecture I will like to thank many of my people who help me in this, forming this course, teaching this course.

One can always say from the student's side that if I teach a course which this VLSI design I taught in IIT Bombay for 15 to 18 years now, maybe earlier even 5 more 25 years I have been connected VLSI design courses and VLSI technology courses, so any course I teach whether it is good or bad you can always know what is student's response in the class, in the exams and afterwards.

And I trust that my students have if not extreme favorable to my teaching and my method of teaching and my content of teaching mostly they were favorable and based on this, this course have been actually designed and given.

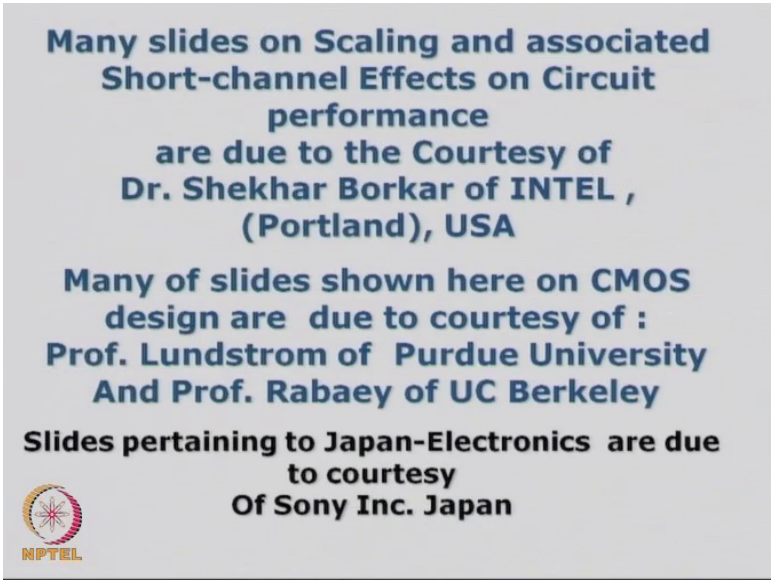
(Refer Slide Time: 01:41:01)



My sincere thanks to all researches whom I acknowledge below for the help of preparing this talk, I must tell you many of the PPT's which many of them I have removed, some of them I kept in this because say huge lectures I have conceded for the course, mostly Silicon Technology

course what will happen in future kind of things, these are courtesy due to one of my good friend Prof. Iwai Hiroshi, who is most distinguished faculty at Tokyo Institute of Technology in Japan.

(Refer Slide Time: 01:41:34)



Many slides on Scaling and short-channel Effects on Circuit performance are due to courtesy of director of Intel at Portland Dr. Shekhar Borkar is one of the outstanding Intel fellow who made the Architecture of Microprocessor and improvements in that which makes Intel number one microprocessor industry in the world and Shekhar Borkar has a large share in progress of Intel, he being from Mumbai, he being friend of us for last 20 years or 25 years.

We have some connection with this gentleman and he keeps feeding us some interesting data happening if not of (()) (01:42:05) this at least 5 years ahead of what they did it. many of the slides shown here on the CMOS design are also courtesy due to one of the faculty from Purdue University Professor Lundstrom and also from the book and the site therefore Professor Rabaey's book on Digital Integrated Circuit.

Professor Rabaey teaches at UC Berkeley of Digital Integrated Circuit so many of the slides have been taken from his site. And slides pertaining to Japan-Electronics are due to courtesy of the Vice President of Sony Incorporate, Japan. Thank you very much all of you for this.