

**Solar Photovoltaics:
Fundamental Technology and Applications
Prof. Soumitra Satapathi
Department of Physics
Indian Institute of Technology-Roorkee**

**Lecture-13
Crystalline Silicon Fabrication Methods**

Welcome everyone once again to our course solar photovoltaics, today we will learn about how to make a single crystal silicon from metallurgical grade silicon and how to assemble them to fabricate a silicon solar cell. Now if you remember in the last class we have learnt about starting from the sand how to process metallurgical grade silicon and we have mention that metallurgical grade silicon has a purity of 98%, this is good for steel and aluminum industry.

But if you wanted to go for electronics industry we need to further purify it, today we will learn about starting from metallurgical grade silicon how we can make a semiconductor grade silicon.

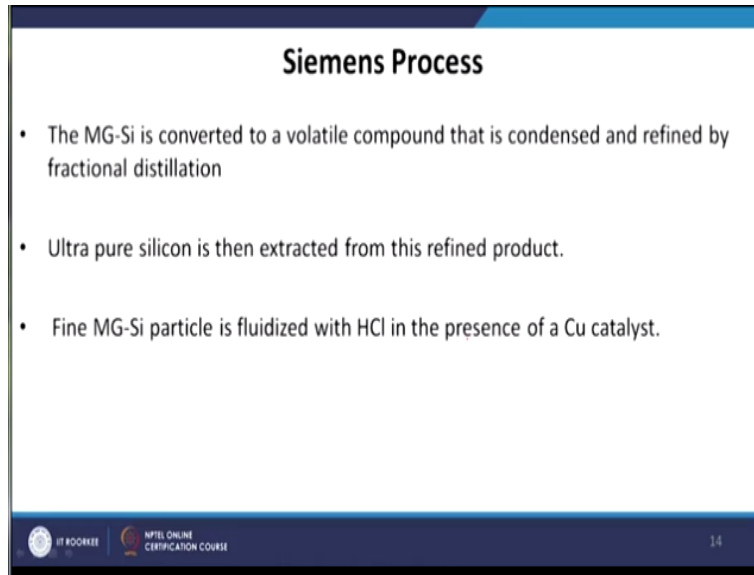
(Refer Slide Time: 01:07)

The slide is titled "Metallurgical grade Silicon to Semiconductor Grade Silicon". It contains two bullet points. The first bullet point states: "For use in solar cells as well as other semiconductor devices, silicon must be much purer than Metallurgical Grade -Si." Next to this point, the handwritten text "99.999999%" is written in red. The second bullet point states: "The standard process to purifying it is known as Siemens process", where "Siemens process" is circled in red. At the bottom of the slide, there are logos for IIT Roorkee and NPTEL Online Certification Course, and the number 13.

For use in solar cell as well as in other semiconductor devices silicon must be very pure in comparison to metallurgical grade silicon, what we mean by the very pure is a purity of silicon which is 99.999999%. So there are six 9 after the decimal point, this standard process is purifying is known as the Siemens method or Siemens process. Siemens process is usually

adopted in the industry to make a polycrystalline silicon starting from the metallurgical grade silicon, what is a Siemens process.

(Refer Slide Time: 01:44)



The slide is titled "Siemens Process" and contains three bullet points. The first point states that metallurgical grade silicon (MG-Si) is converted to a volatile compound, which is then condensed and refined through fractional distillation. The second point notes that ultra-pure silicon is extracted from this refined product. The third point describes the fluidization of fine MG-Si particles with HCl in the presence of a copper catalyst. The slide footer includes the IIT Roorkee logo and the text "NPTEL ONLINE CERTIFICATION COURSE" along with the slide number "14".

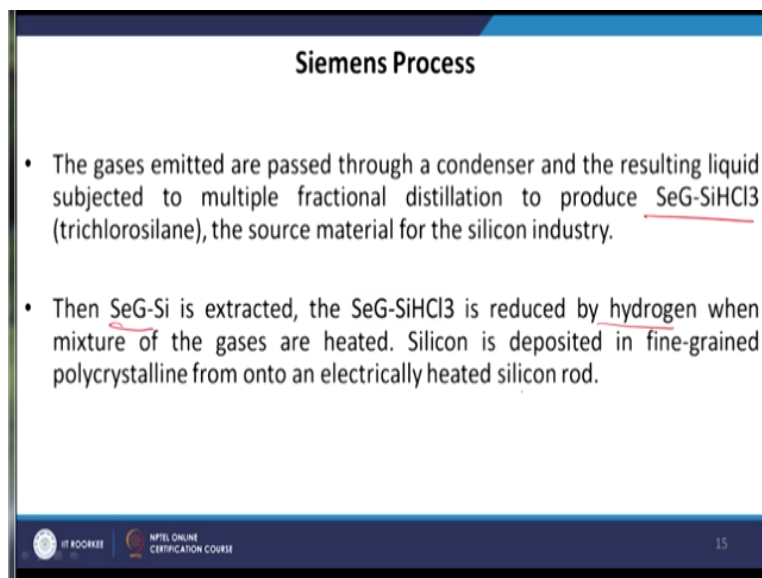
Siemens Process

- The MG-Si is converted to a volatile compound that is condensed and refined by fractional distillation
- Ultra pure silicon is then extracted from this refined product.
- Fine MG-Si particle is fluidized with HCl in the presence of a Cu catalyst.

IIT ROORKEE NPTEL ONLINE CERTIFICATION COURSE 14

The metallurgical grade silicon is converted to a volatile compound that is condensed and refined by fractional distillations, what is the fractional distillations that we learn. Ultra pure silicon is then extracted from this refined product and fine metallurgical grade silicon particle is fluidized with HCl or hydrochloric acid in the presence of the copper catalysis.

(Refer Slide Time: 02:05)



The slide is titled "Siemens Process" and contains two bullet points. The first point explains that gases emitted are passed through a condenser, and the resulting liquid is subjected to multiple fractional distillations to produce SeG-SiHCl_3 (trichlorosilane), which is the source material for the silicon industry. The second point states that SeG-Si is extracted, and SeG-SiHCl_3 is reduced by hydrogen when a mixture of the gases is heated. Silicon is then deposited as fine-grained polycrystalline material onto an electrically heated silicon rod. The slide footer includes the IIT Roorkee logo and the text "NPTEL ONLINE CERTIFICATION COURSE" along with the slide number "15".

Siemens Process

- The gases emitted are passed through a condenser and the resulting liquid subjected to multiple fractional distillation to produce SeG-SiHCl_3 (trichlorosilane), the source material for the silicon industry.
- Then SeG-Si is extracted, the SeG-SiHCl_3 is reduced by hydrogen when mixture of the gases are heated. Silicon is deposited in fine-grained polycrystalline form onto an electrically heated silicon rod.

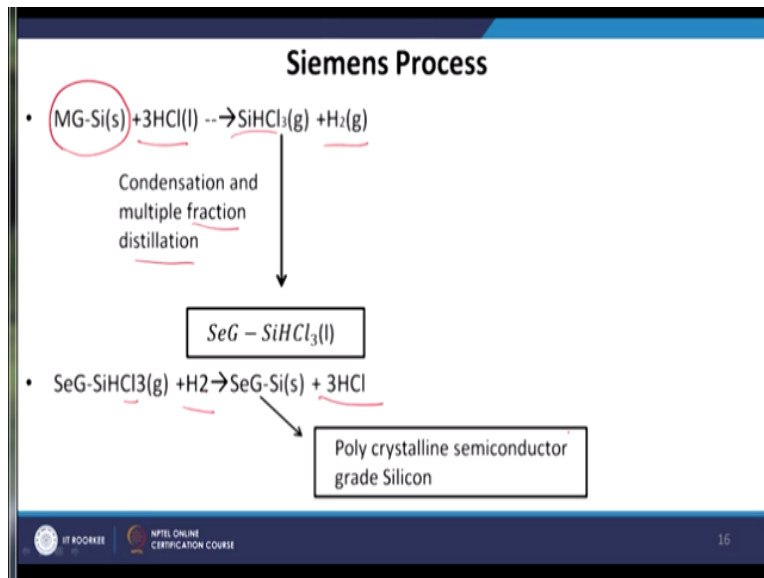
IIT ROORKEE NPTEL ONLINE CERTIFICATION COURSE 15

The gases emitted are passed through a condenser and the resulting liquid subjected to multiple fractional distillations. So in fractional distillations we vary the pressure and we get it the

required chemical or required materials out of a combinations of the material. Now we use fractional distillations in Siemens method to produce this trichlorosilane or SeG-SiHCl₃ and the source material for the silicon industry.

This trichlorosilane is further use to extract the SeG-Si or the SeG-Si is extracted the SeG-SiHCl₃ is reduced by hydrogen when the mixture of the gas and heated. Silicon is deposited in a fine grain polycrystalline from onto an electrically heated silicon rod.

(Refer Slide Time: 02:52)

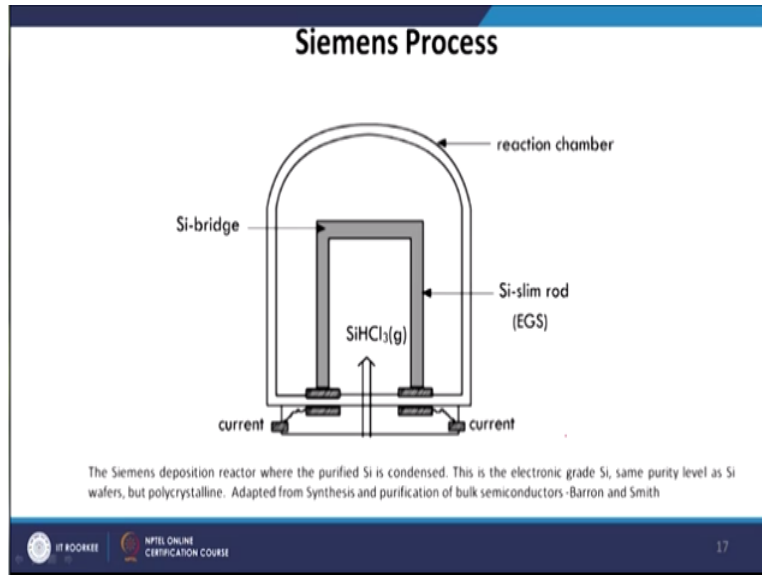


So the reaction process can be summarized by the following method, so we start with a metallurgical grade silicon which is MG-Si we react with a 3HCl hydrochloric acid. So what will happen we will make chlorosilane SiHCl₃ which is a gas + hydrogen, silicon will react with this HCl to make SiHCl₃ and hydrogen. Now this SiHCl₃ this is been condensed and it went through further multiple fractional distillations.

So fractional distillations has been done of this chlorosilane what we get from there, we get SeG-SiHCl₃ and from there SeG-SiHCl₃ which is a gaseous form we react that with a hydrogen to get the hydrogen will react with this chlorine to make the 3HCl again and it will release the SeG-Si from this chlorosilane compound. So we get the polycrystalline silicon and also get the hydrochloric acid back.

This hydrochloric acid can further use to reduce the metallurgical grade silicon to make the chlorosilane, so this process then repeats and we get polycrystalline semiconductor grade silicon.

(Refer Slide Time: 04:05)



In this furnace here what we do here you see that this furnace has a reaction chamber and there is a silicon bridge and this side there is a silicon slim rod is there. Now with the chlorosilane which is coming from here as a gaseous form is condensed and then it going through the further fractional distillations. The current source is hereby given by the 2 electrodes, the Siemens deposition reactors where the purified silicon is condensed, the purified silicon will be condensed here.

This is the electronic grade silicon same purity level as silicon vapors but these are polycrystalline adopted from the synthesis and purification of the bulk semiconductor the book Barron and Smith.

(Refer Slide Time: 04:43)

Siemens Process

- Requirement a lot of energy
- Low yield ~37%
- The high cost of this stage
- Reach to purity 99.9999%

IT ROOKIE NPTEL ONLINE CERTIFICATION COURSE 18

Now Siemens process has some disadvantage, one big disadvantage is that it requires a lot of energy and actually this is the main the single crystal silicon solar cell is so costly. And the yield is also low like 37%, so in industry people like the yield should be very high and the cost of production should be low. The high cost of this stage but the advantage is that we can reach a purity of 99.9999 even you can add 2 more 9 for an industry grade silicon this much purity percentage.

So there are some disadvantage and some advantage related to the Siemens method. But the Siemens method produce a polycrystalline silicon. We need to get a single crystal silicon starting from a poly crystal silicon, how we can get that.

(Refer Slide Time: 05:31)

Semiconductor – grade poly crystalline to single-crystal wafers

- Two types of processes are well known for the crystal pulling or ingots pulling for mono crystalline Si which is circular in shape. These are Czochralski process and float zone process.
- **Czochralski technique (CZ)** - this is the dominant technique for manufacturing single crystals. It is especially suited for the large wafers that are currently used in IC fabrication.
- **Float zone technique** - this is mainly used for small sized wafers. The float zone technique is used for producing specialty wafers that have low oxygen impurity concentration.



There are 2 different methods for that for getting a crystal pulling or inverse pulling for the mono crystalline silicon which is circular in shape. There are 2 methods that one is called Czochralski technique and another is called the float zone technique. We will learn about this techniques today in Czochralski technique this is the dominant technique for manufacturing single crystal, it is especially suited for the large wafers that are currently used in IC fabrication.

And in float zone technique this is used for the small size vapors, the float technique is use for producing specifically wafers that have low oxygen impurity concentrations.

(Refer Slide Time: 06:07)

Czochralski technique (CZ)

- A schematic of this growth process is shown in figure. The various components of the process are
 1. Furnace
 2. Crystal pulling mechanism
 3. Ambient control - atmosphere
 4. Control system
- The starting material for the CZ process is electronic grade silicon, which is melted in the furnace. To minimize contamination, the crucible is made of SiO_2 or SiN_x . The furnace is heated above 1500 C , since Si melting point is 1412 C . A small seed crystal, with the desired orientation of the final wafer, is dipped in the molten Si and slowly withdrawn by the crystal pulling mechanism.

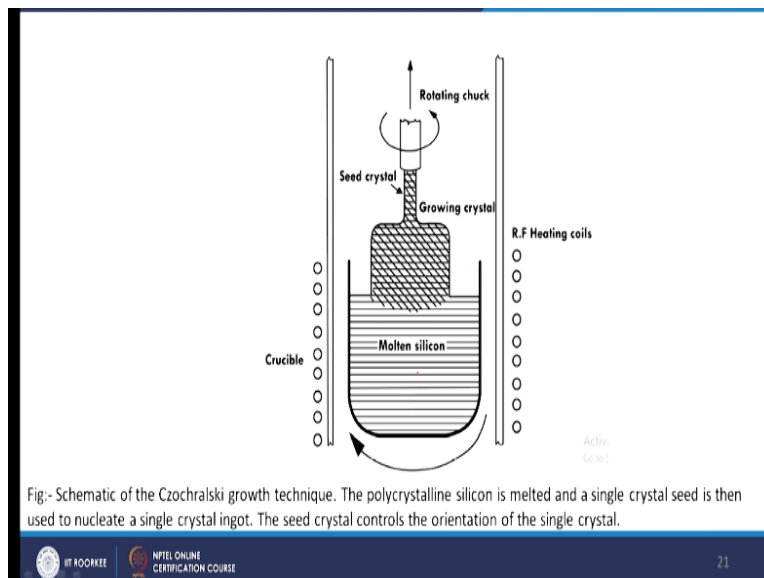


Now in **in in** Czochralski technique a schematic of this growth process is shown in the next figure. Here there are different components are there one component is furnace then there are crystal pulling mechanism there are ambient control atmosphere and there are control system. The starting method for the CZ process is electronic grade silicon, so this silicon or electronic grade silicon but they are poly crystalline which is melted in the furnace.

To minimize contamination the crucible is made of Silicon dioxide or SiN_x . So that the silicon is kept in an environment of silicon only, the furnace is heated above 1500 degree Celsius since silicon melting point is 1412 degree Celsius. So silicon melting point is 1412 degree Celsius, so if we have to melt silicon then we need to heat it beyond this temperature. And CZ method the poly crystalline silicon is heated at 1500 degree Celsius.

A small seed crystal with the desired orientation of the final wafer is dipped in the molten silicon and slowly withdrawn by the crystal pulling mechanisms. So to grow the single crystal we need to have a seed, so first a small seed of the fine wafer is dipped inside the molten silicon and slowly withdrawn by the crystal pulling methods. So the liquid silicon will grown on this seed and we will get a single crystal silicon.

(Refer Slide Time: 07:33)



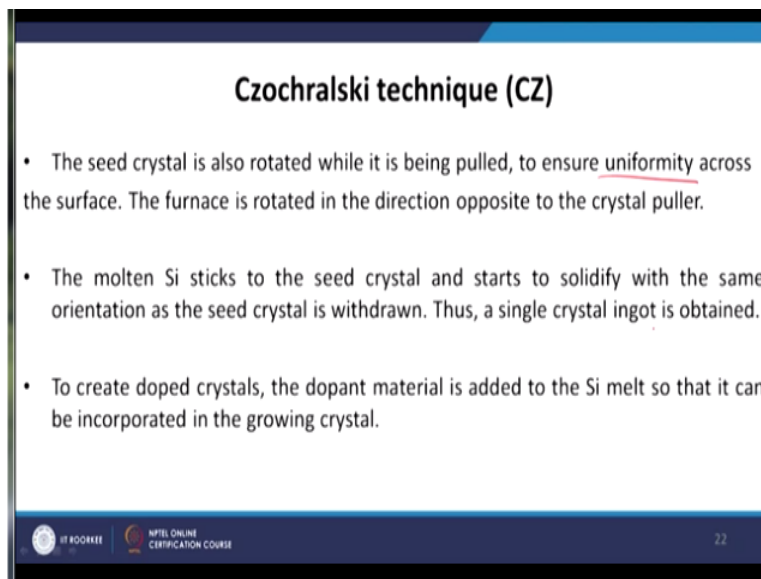
Here you can see in this flask we have the molten silicon and then the grown seed crystal is showing here. So the seed crystal is first dipped in the molten crystal and then on the top of the

seed crystal the silicon single crystal will start growing and eventually it will grow to a large single crystal, this is a crucible and this is the RF heating coil. These are schematics of the CZ growth technique the poly crystalline silicon is melted and a single crystal seed is then use to nucleate a single crystal ingot.

The ingle crystal controls the orientation of the growth of this crystal, so at it happens in a normal crystal growth. We need to have a seed and then the seed helps for the nucleation and then we need to have a growth process. Now depending upon the rate of the nucleation on the growth we can get the grain size of the single crystal. So the method is very simple, here we have a molten silicon which the molten silicon we got it by hitting the silicon at high temperature.

Then to get a single crystal we dip a molt or a seed of the single crystal inside this molten silicon and the silicon started growing on that. And depending upon the heat and temperature and the growth kinetics we get the larger or smaller side of single crystal silicon and this process is the Czochralski method.

(Refer Slide Time: 08:52)



Czochralski technique (CZ)

- The seed crystal is also rotated while it is being pulled, to ensure uniformity across the surface. The furnace is rotated in the direction opposite to the crystal puller.
- The molten Si sticks to the seed crystal and starts to solidify with the same orientation as the seed crystal is withdrawn. Thus, a single crystal ingot is obtained.
- To create doped crystals, the dopant material is added to the Si melt so that it can be incorporated in the growing crystal.

if ROOKIE NPTEL ONLINE CERTIFICATION COURSE 22

In a Czochralski technique or CZ technique the seed crystal is also rotated while it being pulled. So when it is being pulled it is also rotated, why rotation, to get a uniform distribution, to ensure uniformity across the surface. The furnace is rotated in the direction opposite to the crystal

puller, so if the crystal puller is rotated in the right hand side the furnace is rotated on the left hand side.

The molten silicon sticks to the seed crystal and starts to solidify with the same orientation as the seed crystal is withdrawn. Thus a single crystal ingot is obtained, to create doped crystal the dopant material is added to the silicon melt so that it can be incorporated in the growing crystal.

(Refer Slide Time: 09:32)



Semiconductor grade polycrystalline silicon to single crystal silicon wafers is showing at here, you see that SeG polycrystalline silicon is first melted in a crucible with trace level of one of the dopants required to the complication of the device is added. So first we take the molten silicon what is the SeG level silicon and then depending upon what kind of impurity we need to add for our final application.

We can add then aluminum based impurity or born base impurity and finally we get a doped silicon which is showing here on the right hand side.

(Refer Slide Time: 10:01)

Semiconductor – grade poly crystalline to single-crystal wafers

- For solar cells, boron, a p-type dopant, is normally used, using a seed crystal and with very close temperature control, it is possible to pull from the melt.

Seed Crystal

Silicon Chunks Molten Silicon Silicon Ingot

IIT ROORKEE
 NPTEL ONLINE CERTIFICATION COURSE
24

For solar cell boron a p-type dopant is normally used, using a seed crystal and with very close control temperature, it is possible to pull out a p-type doped seed crystal from this melt. So what happens like you know, so let us say this is a seed crystal and this is my silicon chunks or molten silicons. So the molten silicons is first dipped inside this and it is take out and you get a silicon ingot like this.

(Refer Slide Time: 10:30)

Semiconductor – grade poly crystalline to single-crystal wafers

A large cylindrical single crystal of silicon, of diameter in excess of 12.5 cm and 1-2m in length are routinely grown in this manner.

Seed
Crystal
Molten silicon

IIT ROORKEE
 NPTEL ONLINE CERTIFICATION COURSE
25

A large cylindrical single crystal of silicon of diameter of excess of 12.5 centimeter and 1 to 2 millimeter in length are routinely grown in this matter. You see the ingot like you know this is the crystal and this is a seed and this is a molten silicon and the ingot is large as 1 to 2 meter in length and the diameter is 12.5 centimeter, so this is a shape of a ingot. But this is a very large

ingot to make it useful we need to cut it, we need to cut it by a diamond saws and make it a piece of the silicon wafer from it, how can we do that.

(Refer Slide Time: 11:01)

Semiconductor – grade poly crystalline to single-crystal wafers

- Then the large single crystal is sliced up into wafers which are as thin as possible (Silicon solar cells need only be 300 μ m or so thick to absorb most of the appropriate wavelength in sunlight)






Figure 6.3. Slicing of thin wafers from a cylindrical ingot. The techniques used for this slicing process are described and compared in Ref. 6.3. About half the ingot is wasted as kerf or cutting loss in this process.

NPTEL ONLINE CERTIFICATION COURSE 26

Then the large single crystal is sliced up into wafers which are as thin as possible, silicon solar cells need only 300 micro meter thickness to absorb most of the appropriate wavelength in the sunlight. So if the thickness is 300 micron, so we need to cut the wafer in that dimension and here we are showing that starting from the silicon this ingot we cut it in a single piece to get this kind of silicon wafers.

So slicing of thin wafers from a cylindrical ingot the techniques used for the slicing process at described in the reference also and usually we use the diamond cutter to cut it. And during the cutting process also we waste some of the silicon and finally this is kept in a box which have been separated one of the wafer from the other.

(Refer Slide Time: 11:45)

Characteristic

- This present wafering technology is difficult to cut wafers from the large crystals to wafers thinner than $300\mu\text{m}$ and still retain reasonable yields.
- More than half the silicon is wasted as kerfs or cutting loss in the process
- The low overall yields of single-crystal

IT ROOKEE NPTEL ONLINE CERTIFICATION COURSE 27


The present wafering technology is difficult to cut wafers from the large crystal to wafers thinner than 300 microns and still retain reasonable yields. So far now a days we can easily cut until 300 micrometers but going beyond that is always difficult. But 300 micrometer is good for us because that is good enough to absorb the sunlight for a silicon solar cell. More than half the silicon is wasted as kerfs or cutting loss in this process.

So that means if the most of the silicon got wasted during the cutting process, so the yield is low. So that is why even starting from a single crystal to get a silicon wafer the yield is very low. So now we have single crystal wafers in our hand, the next job is to make a silicon solar cell.

(Refer Slide Time: 12:29)

Single-Crystal Wafers to Solar Cells

- After etching the silicon wafers and cleaning them, additional impurities are introduced into the cell in controlled manner by a high-temperature impurities diffusion process.
- To make solar cell, n-type impurities must be introduced to give a p-n junction, phosphorus is the n-type impurity which is generally used.



IT ROOKEE NPTEL ONLINE CERTIFICATION COURSE 28

After etching the silicon wafers and cleaning them additional impurities are introduced inside the cell in a controlled manner at a high temperature diffusion process. So we take this silicon wafer in some kind of cylindrical or rectangular chamber like this and it is made at very high temperature. And whatever the impurity we have to put like you know we diffuse that impurity inside this to make it either a p-doped or an n-doped semiconductor.

To make solar cell n-type impurities must be introduced to give a p-n junction. We have already a p-doped semiconductor but to make a p-n junction solar cell we need an n-type impurity on top of the p-type semiconductor. So phosphorus is an n-type impurity which is generally used to make n-doping, so phosphorus is usually used to make the p-type semiconductor and n-doped semiconductors, so that we get a p-n semiconductor, how can we do that.

(Refer Slide Time: 13:23)

Process to doped n-type

- A carrier gas is bubbled through phosphorus-oxychloride (POCl_3), mixed with a small amount of oxygen, and passed down to a heated furnace tube in which the wafers are stacked, this grows an oxide layer on the surface of the wafers containing phosphorus, at the temp involved $(800-1100)^\circ\text{C}$ the phosphorus diffuses from the oxide into the silicon.
- After about 20min the phosphorus impurities override the Boron impurities in the region near the surface of the wafers to give a thin, heavily doped n-type region

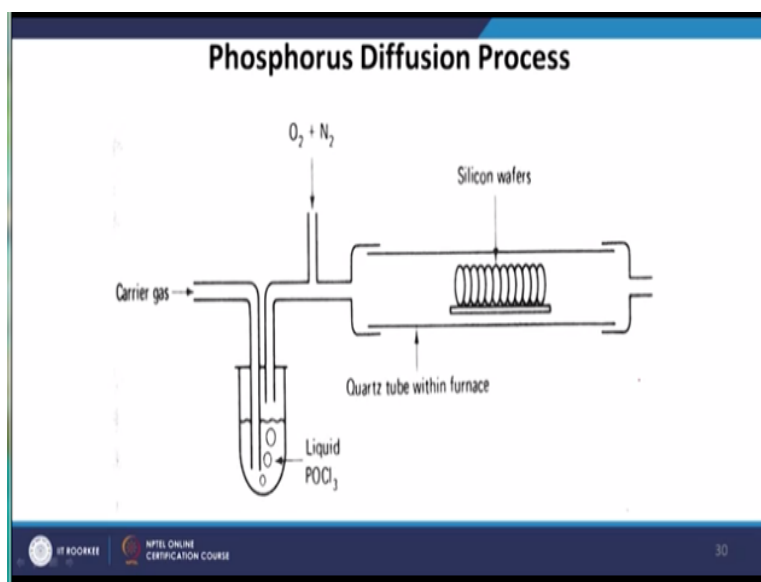
IT ROOAKKE NPTEL ONLINE CERTIFICATION COURSE 29

A carrier gas is bubbled through the phosphorous-oxychloride POCl_3 mixed with a small amount of oxygen and pass down to a heated furnace tube in which the wafers are stacked. This grows an oxide layer on the surface of the wafers containing phosphorous at the temperature involved 800 to 1000 degree Celsius, the phosphorous diffuse from the oxide into the silicon. So first if we take the chamber we have the silicon wafer and then we are putting a carrier gas, the carrier gas contains phosphorous oxychloride.

Here the phosphorous is mixed with a small amount of oxygen, what will happen they will make a layer of the oxide on top of this silicon wafer. And finally at high temperature from 800 to 1000 degree Celsius this phosphorous will slowly diffuse in the bottom of this oxide layer and it will dope the silicon. After about 20 minute the phosphorous impurities overwrite the born impurity in the region near the surface of the wafer to give a thin heavily doped n-type region.

We have learnt that for p-n junction silicon solar cell, n-type is very very thin and heavily doped, so that the depletion region extend inside the p-regions.

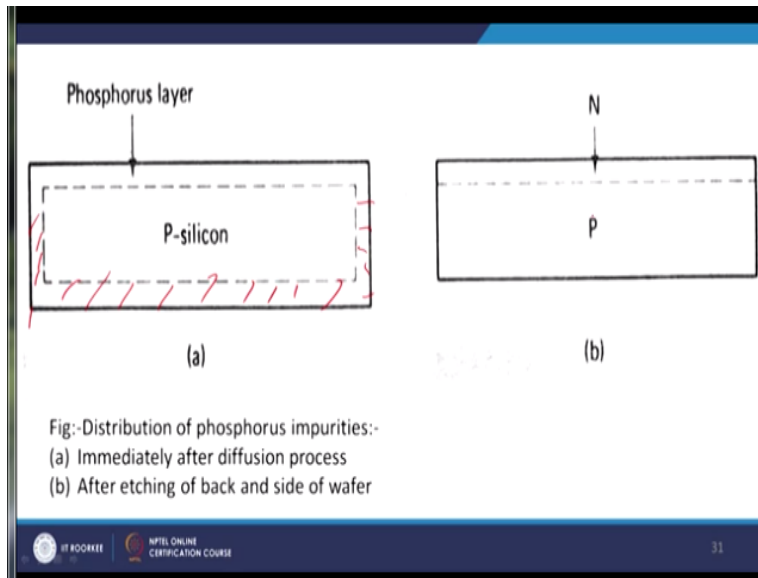
(Refer Slide Time: 14:40)



Now the phosphorous diffusion process is showing here you can see that silicon wafers which are staked here and this is a cylindrical tube, now the carrier gas comes from here. So the liquid POCl_3 that mixed in the carrier gas and comes through here, so the oxygen and nitrogen is also purge a **very slow** very small amount of oxygen and nitrogen gas. Now once it goes through this chamber, so they makes a very thin layer of the oxide which contains the phosphorous.

Now when we heat this chamber then what will happen the phosphorous will slowly diffuse inside and override the boron impurity to make a highly doped and narrow n-p junction.

(Refer Slide Time: 15:15)





So on the top of the p-type silicon we get a n-type doping or we get a n-p junction. So here in the first figure we are showing the distribution of the phosphorous impurities immediately after the diffusion process and after etching of the back side of the wafer. So when the diffusion is completed at high temperature phosphorous seeds on all the sides. But we need the nitrogen do we need the n-doping only on the top we do not need at the back.

So we need to etch this side and we need also etch this side, so when we etch the bottom side and the 2 sides to get the n-type doping on the top. So we have n-type doping on the top and p-type doping at the bottom we get the p-n junction.

(Refer Slide Time: 15:56)

Vacum Evaporation

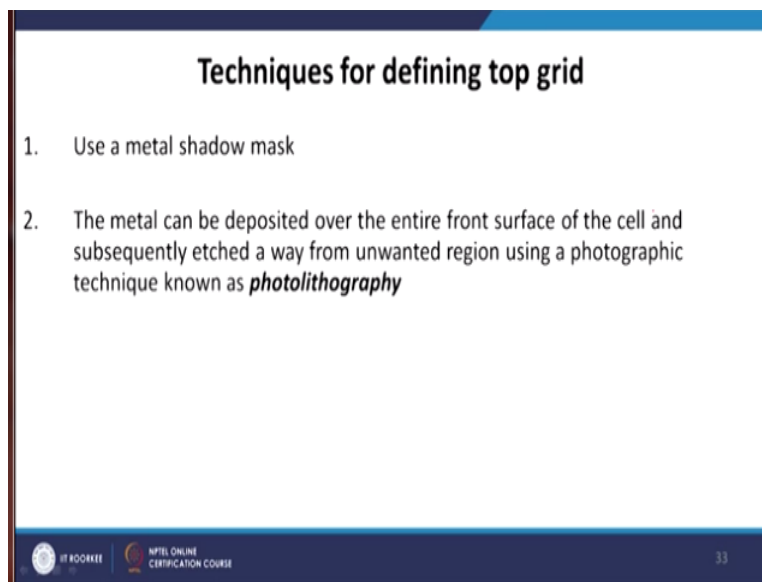
- The standard technology to metal contact are then attached to both the n-type and the p-type region, the metal to be deposited is heated in a vacuum to a high enough temp to cause it to melt and vaporize, it will then condense on any cooler parts of the vacuum system in direct line of sight, including the solar cells, the back contact is normally deposited over the entire back surface, while the top contact is required in the form of a grid.

The standard technology to metal contact are then attached to both the n-type and p-type region. So now to complete a solar cell, what we need, we need a sandwiched type of structure, we need to have 2 electrodes one is cathode another is anode. So here we have a silicon solar cell which is like a p-type and then there is an n-type semiconductor but to make the contact I have to put some metal electrode, so that the electric circuit get completed.

To the metal is deposited in a very high vacuum, the standard technology to metal contact are then attach to both the n-type and the p-type region. The metal to be deposited is heated in vacuum to high enough temperature to cause it to melt and vaporize, it will then condense on the cooler parts of the vacuum system and then directly go and deposit on this wafer. So the back contact is normally deposited over the entire back surface while the top contact is required in the form of the grid.

(Refer Slide Time: 16:50)



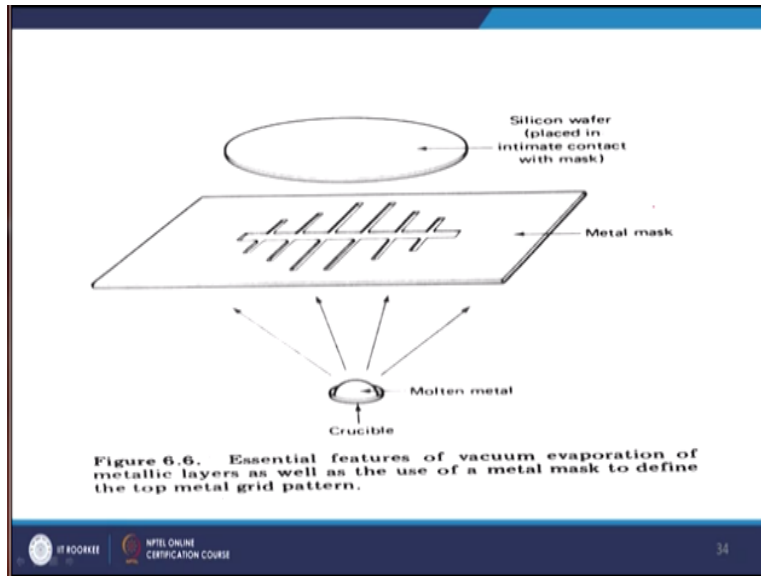
Techniques for defining top grid

1. Use a metal shadow mask
2. The metal can be deposited over the entire front surface of the cell and subsequently etched a way from unwanted region using a photographic technique known as *photolithography*

IT ROOKIE NPTEL ONLINE CERTIFICATION COURSE 33

Usually we use a shadow mask or metal shadow mask to make this grid, the metal can be deposited over the entire front surface of the cell and subsequently etched a way from unwanted region using a photographic technique called as photolithography.

(Refer Slide Time: 17:05)





So here we are showing this like this is a metal mask and we have this molten metal which is kept in a crucible. So when we heat at high temperature what will happen, let us say if an aluminum metal it will start vaporizing and the vapors the atoms of the metals they will go and start depositing on this thing. Depending upon the openings which is described by the mask and we have a silicon vapor which is the back placed in the intimate contact with the mask.

Now wherever there is an opening according to the structure of the mask the metal will go and deposited there. Now we can selectively etch or we can selectively washout that part of the metal which we need or which we do not need to make a good contact. So this figure is an essential features of a vacuum evaporation of metallic layer as well as the use of the metallic mask to define the top metal, grid pattern. We use the same technique for organic solar cell or even perovskite solar cells for metal depositions.

(Refer Slide Time: 17:56)

The contact made up of three separate layer

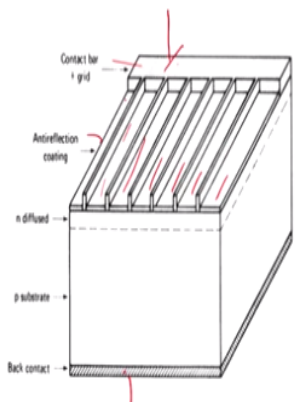
1. Thin layer of titanium is used as the bottom layer.
2. Layer of silver in the top.
3. The sandwiches layer is palladium





35

The contact made of 3 separate layers, the layer of titanium is used as the bottom layer, layer of silver is the top and the sandwich layer is palladium, so there are 3 layers we make as a contact layer.

(Refer Slide Time: 18:09)

- After deposition the contacts are sintered at 500-600 °C to give good adherence and low contact resistance,
- Finally a thin antireflection (AR) coating is deposited on the top of the cell by the same vacuum evaporation process.

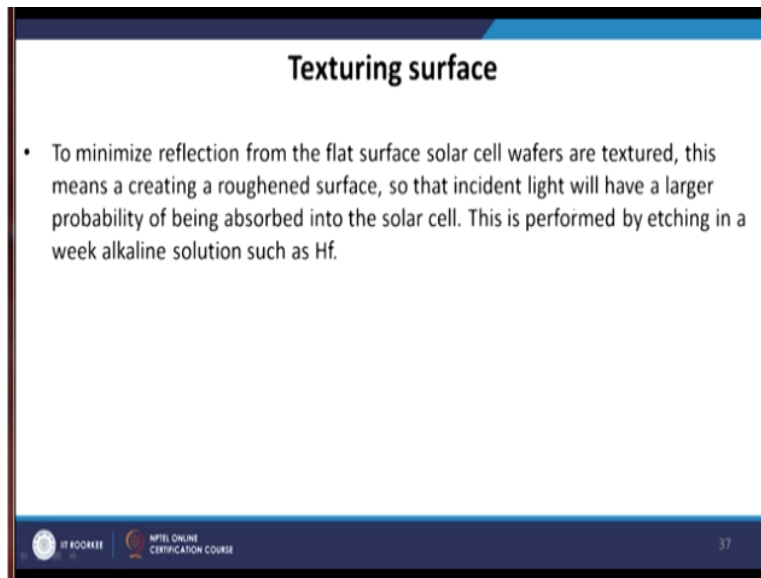




36

After deposition the contact are sintered at 500 to 600 degree centigrade to give good adherence and low contact resistance. Finally a thin antireflection coating is deposited on the top of the cell by the same vacuum evaporation method. So we have a back contact then we have a p-substrate, then we have a n-diffuse substrate and then we have this metal grid and then top of that we have a antireflection coating and we have a context bar.

So these are the grids and these are the context bar, so one contact we take from here, one contact we can take from here. And we have a p-n junction diode which is sandwiched between these 2 contact and just to reduce the light loss we have putted this kind of grid kind of structures and we also put it a anti-reflection coating.

(Refer Slide Time: 18:56)



Texturing surface

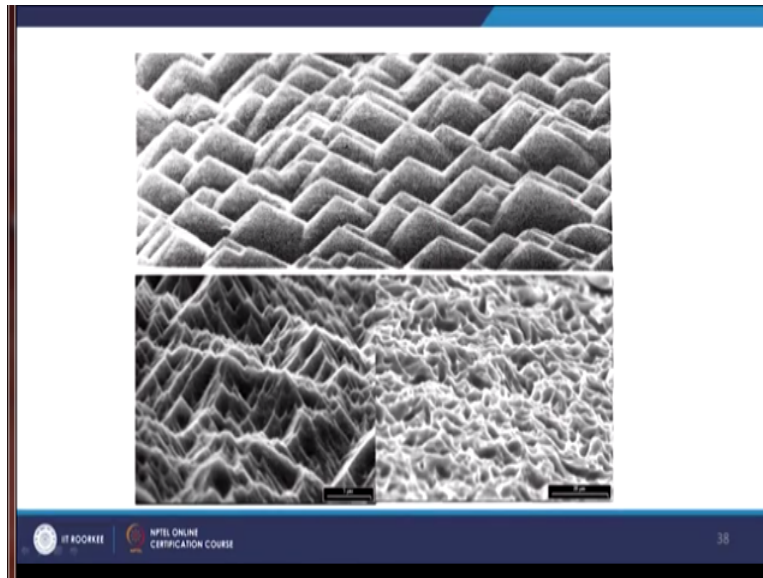
- To minimize reflection from the flat surface solar cell wafers are textured, this means a creating a roughened surface, so that incident light will have a larger probability of being absorbed into the solar cell. This is performed by etching in a weak alkaline solution such as Hf.

IT ROOKEE | NPTEL ONLINE CERTIFICATION COURSE 37

To minimize the reflection from the flat surface of the silicon solar cell we usually texture the surface. So that to minimize the flat surface silicon cell wafers these are textured, this means creating a rough surface. So that the incident light we will have a larger probability of being absorbed into the solar cell. So if we make a surface very patterned or very textured, so the probability of absorptions of the sunlight is much higher.

This is performed by etching in a weak alkaline solution such as hydrofluoric acid. If we etch the silicon wafer on the top and if we look it under a SEM microscope it looks like that

(Refer Slide Time: 19:31)



So you can see that this kind of structure which is like periodic in nature is get by the wet etching process and this helps for the light to get more and more trapped an enter inside the silicon solar cell.

(Refer Slide Time: 19:45)

Characteristic

- Yield of about 90% from starting wafers to completed terrestrial cells can be obtained.
- This make the processing very labor-intensive.
- The vacuum evaporation equipment is expensive compared to its throughput.
- the material expensive such Ag.


The yield is about 90% from starting wafers to completed terrestrial cells can be obtained, this make the process very labor-intensive. The vacuum evaporation equipment is expensive compared to the throughput the material expensive such as silver. So the material which is used in this case the contact that is silver and that is expensive and same time this process is very very labor intensive and energy extensive.

(Refer Slide Time: 20:07)

Solar Cell to Solar Module

After interconnecting between cells solar cells require encapsulation by glass to:

1. Mechanical protection ✓
2. Electrical isolation ✓
3. Chemical protection ✓
4. Mechanical rigidity to support the prattle cells and their flexible interconnection ✓

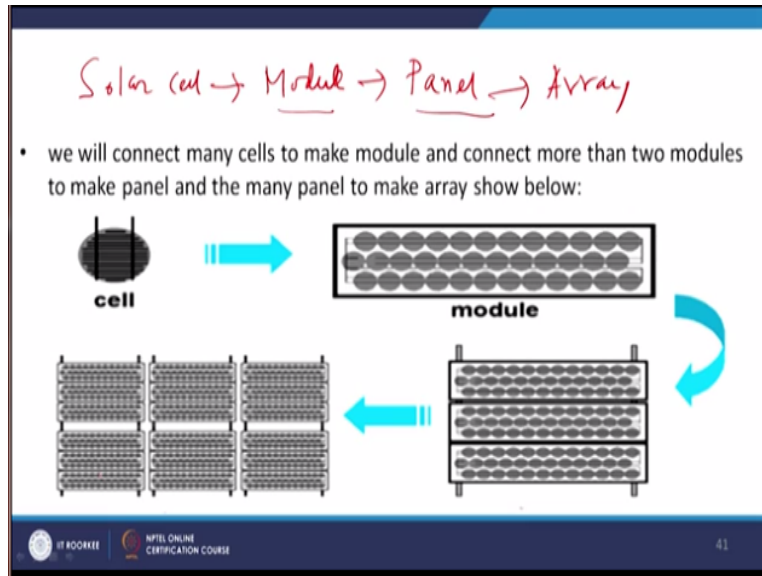
 NPTEL ONLINE CERTIFICATION COURSE 40

So that is why the cost of production becomes very high, now we have a solar cell in our hand, so what we have to make, we have to make a solar module. After interconnecting between cells, the solar cell needs to be encapsulated by the glass either by mechanical for mechanical protection, for electrical isolation, chemical protection and mechanical rigidity to support the fragile cells and their flexible interconnection.

So keep in mind that whenever we make a solar cell we need to encapsulate the solar cell and we encapsulate it by a special kind of glass, what is the objective behind encapsulation. First is mechanical protection, so that the solar cells is protected from some kind of fracture or some kind of breaking, second is electrical isolation. Let us say your solar cell is in the presence of some electrical device, so that it does not get any kind of electrical inductions.

Third is chemical protection by some mistake if somebody peel some kind of chemicals on that, so our solar cells will be protected. Fourth is mechanical rigidity to support the fragile cells and the flexible interconnections. So these are the need why we need to encapsulate the solar cell.

(Refer Slide Time: 21:12)



Now next thing is that we will connect many solar cell to make module and connect more than 2 modules to make panels. And to connect many panels to make a array, so starting from solar cell if we connect them we will get them module. If we connect that 2 or more module will get panel, if we connect 2 or more panel we get array. So the array, the solar array which we usually see that actually consist of solar panel which is consist of solar module.

And this module is made of millions of solar cells, small cells which are in a interconnected in series or in parallels. Here a single solar cell is showing here when you connected all this silicon solar cells you get this module. Then when you connect this so many modules together you get this kind of panel where 1, 2, 3 modules are here. Now if we have so many panels connected each other then we get a solar array which is useful for driving any load or giving the electricity in our room.

So today we have learn that starting from the metallurgical grade silicon how we can get a semiconductor grade silicon and the process is called the Siemens method. But in Siemens method we get a polycrystalline silicon to make a solar cell we need a single crystal silicon. Now how can we make a single crystal silicon from a polycrystalline silicon by Czochralski method, this method involves high temperature and we get a really pure silicon.

Now this silicon we can make by p-doping but for making it useful for a solar cell application we have to put a layer of n-doping on top of the p-doped semiconductor, how can we make it n-doped. So usually we use a carrier gas which contains phosphorous as an impurity and a very small amount of oxygen and at high temperature an oxide layer is formed on top of this p-doped silicon.

Then at very high temperature the phosphorous diffuses inside it and makes a layer of the p-doping all the way surrounding this silicon wafer. But what will happen like we have to selectively etch the n-type doping from the back end and from the side end. So that we get n-type doping on the top only and in this process we get a p-n junction silicon cell. Now the rest of the job is to put the metal electrode and put some contact.

This metal electrode is put at high vacuum and at very high temperature this process is a very very combustion process. And we usually use some kind of metal mask to get a desired kind of geometry, finally we put some contact and antireflection coating. The job of the antireflection coating is to minimize the reflection loss as much as possible. And our solar cell is completed by putting the p-n junction silicon between the 2 electrodes, so it is like a sandwich kind of device.

So once we have a silicon solar cell in hand then we can connect 2 or 3 solar cells to make a module. Then 2 or 3 modules come together to make a solar panel and then further 2 or 3 solar panels come together to make a solar array. So the required voltage or the required current what we get from the solar array becomes much higher than a single solar cell which satisfies our daily activities.

So today we will learn about starting from the metallurgical grade silicon, how we can make a silicon solar cell and make a silicon solar array.

(Refer Slide Time: 24:40)

References

- Microchip fabrication - Peter van Zant.
- Synthesis and purification of bulk semiconductors:- Barron and Smith
- Solar Photovoltaics : Fundamentals , Technologies and Applications by Chetan Singh Solanki



For more details you can look for the microchip fabrication every nice book by Peter van Zant nd also the synthesis and purification of bulk semiconductor Baron and smith. And obviously our standard textbook solar photovoltaics fundamental technology and application by Chetan Singh Solanki, thank you very much.