Electronics

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Module No. 05

Lecture No. 8

FETS and MOSFETS

CMOS Inverter (Contd.)

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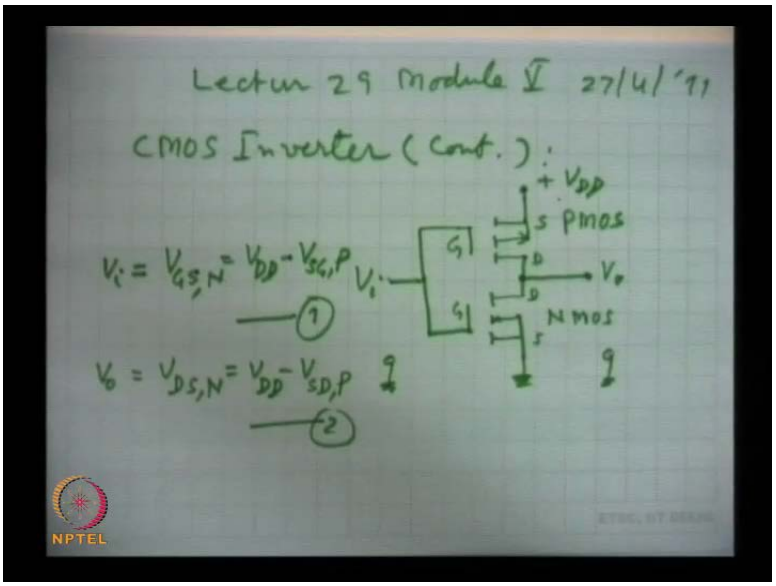

We continue our discussion on CMOS circuits just to remind you CMOS is tends for complimentary MOSFET circuits. In complimentary MOSFET circuits in CMOS, we have Pmos and NMOS simultaneously, present on the chip these are very widely used circuit and the most advanced circuits are actually, CMOS circuits and there are two basic reasons for their popularity. One is that the power consumption is extremely low in CMOS circuits, this we will show that why the power dissipation. The power consumption is very small it is in fact, the lowest of all the known logics another reason is that switching is very fast then on the previous turn we said that is an example of CMOS circuit.

We take a inverter. A inverter circuit which is also called a not circuit and a inverter circuit is when input, it has only one input and one output. So, when the input is high the

output is low and when input is low, the output is high; that means, the input voltage is inverted that is why it is called inverter. Now, this was also said that why we are taking the inverter because inverter is basic for the digital electronics. The universal gates nor gate and nand gate these can be realized by the extension of inverter circuit. So, what is the CMOS inverter the circuit is this, this is Pmos, PMOSFETs and this is NMOS, NMOSFET.

And this is the d c supplied Vdd the input is obtained by connecting gates together for both the mos, MOSFETs and the output is taken by connecting both the drains, drain of Pmos and drain of a NMOS, they are connected together and from there the V out is taken. Now, we also discuss that actually, Pmos requires a negative supply voltage that can be provided by giving a positive source voltage. So, that is with a way these N MOSFET and P MOSFETs are connected.

So, this source is connected to this supply plus terminal and this way we can get the we can bias both the MOSFETs by a single supply, then we obtained to equations one for the input, input voltage is what is the voltage here and that is we can write actually, that two equations which we got earlier this was Vi this is equal to Vgsn is tend for NMOS this is equal to Vdd minus Vsg for P this is equation one. Input is equal to this voltage which is Vgsn and that is also equal to Vdd minus this voltage, that is Vsgp and the similarly, we can write for V out this is Vdsn this is d, this is n, this is s.

So, dn for NMOS and which is equal to Vdd minus Vsd for P and this we call equation 2 this 2 equations, we obtained the other day which are simple these are simple the expressions which you have already see that V out will be this voltage.

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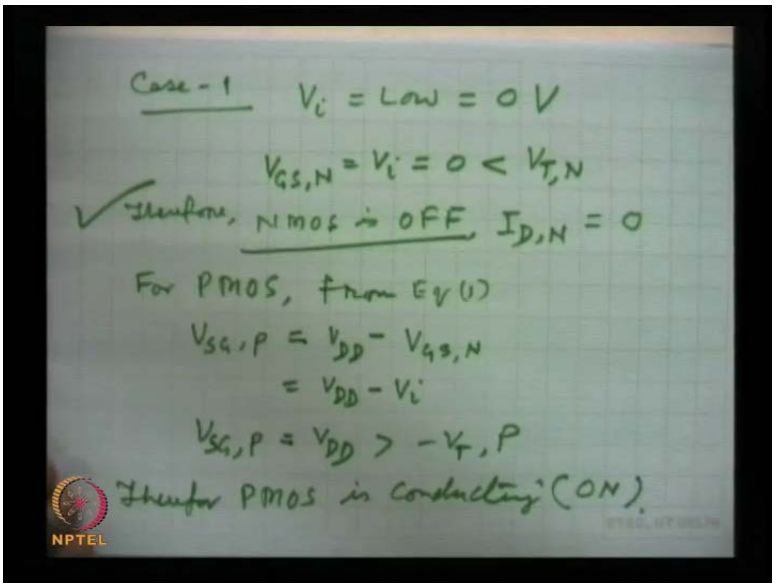

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Which is this and this is equal to this minus this. So, this two equations we will be using later also now, the two cases we can discuss and that two cases are case one, case one when input is low that is Vi is low. So, this is 0 volt. Now, you can see you will have to keep in mind this circuit, when this voltage is low; that means, this NMOS will be off because in this case Vgsn is equal to Vi which is 0 and so obviously, it is less than the threshold voltage required for the NMOS and hence therefore, NMOS is in off state is off and when the transistor is off; obviously, the drain current I d in the NMOS.

So, we write I d n this is equal to 0 and then for Pmos, for Pmos this is NMOS is off, this mos is off. Now, let us find out when input is low what of out Pmos. So, for Pmos from equation one we get this is equation 1 from there we write Vsgp which will be equal to Vdd minus Vgsn this what we write. So, Vsgp is equal to Vdd, Vdd minus Vgsn and Vgsn is Vi. So, this is equal to Vdd minus Vi and since Vi is 0. So, this is simply Vsgp this is at the potential Vdd and this is greater than the threshold voltage because of the way, it is connected the way we have connected the drain is here the source is here.

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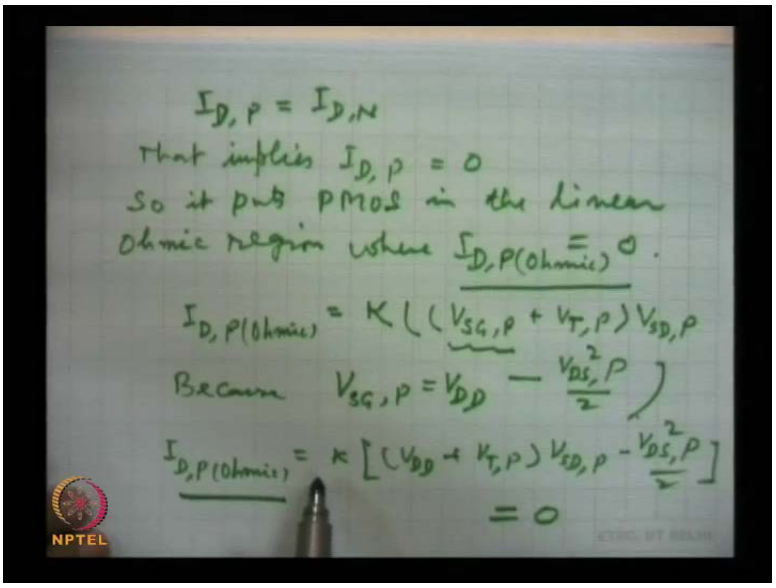

So, when Vsgp is equal to Vdd it is greater than V t for P and therefore, Pmos this was one state NMOS was off and now therefore, Pmos is conducting; that means, it is on MOSFETs they are in series. So, that will imply that drain current in the Pmos should be equal to the drain current in the NMOS because both are in the series and that implies, that implies that I d p is equal to 0. Now, it is conducting, but the, but the drain is 0 and if you look at the drain characteristics this situation is just in the beginning of the ohmic linear region. So, it puts Pmos in the linear ohmic region, where Idp ohmic is equal to 0.

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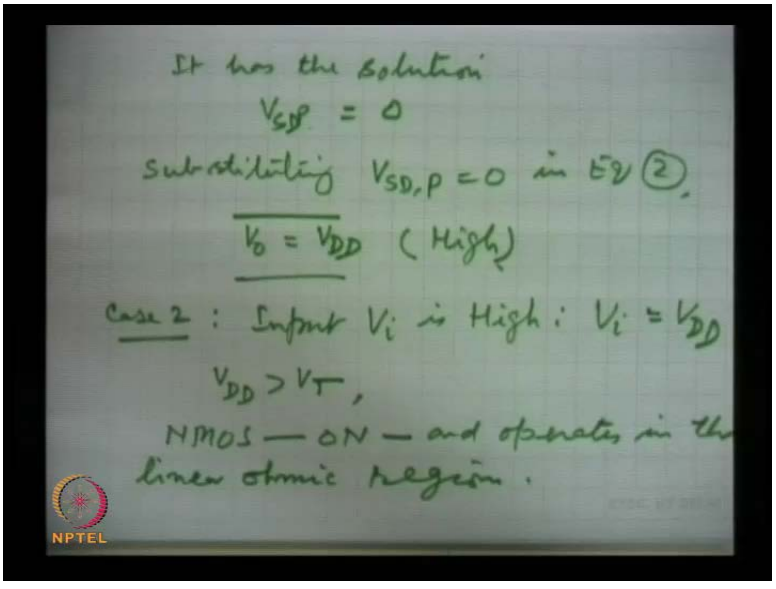

And once we write the expression which, when we talked about the enhancement MOSFET then in ohmic region the drain current is given by certain expression. So, that we use here. So, Idp ohmic is equal to k the constant, the conductivity constant and this is Vsgp plus Vtp here proper sign of Vt has been used and Vsd for P minus Vds for P square by 2 this is the equation and because Vspvsg for P is equal to Vdd here this was 0. So, this one Vsgp is equal to Vdd this is what we have written.

So, here we can replace this by Vdd. So, Idp ohmic becomes equal to k Vdd plus Vt for Pvsg for P minus Vdsp square by 2 this is, this is equal to 0 here. So, this we equate to 0. Then the solutions of this equation with this 0 k is not 0 and other parameters are not 0 this will imply that it has the solution, it has the solution Vspsdp is 0. Now, substituting this in equation two here Vsdp is 0 that will tell us, what will be the output in this equation.

So, substituting, substituting Vsdp equal to 0 in equation 2 we have V out equal to Vdd that is high. This is what we expect from the inverter in the inverter, when the input is high is input is low, the case under consideration then it results into high output and this is what we are getting. So, this is case one that completes and then we go for case two when input Vi is high, meaning Vi is Vdd we can see here also once, we say in the first case when input is low. So, this was off and this was conducting. So, what is the voltage, which you expect at output because this is conducting and this is off.

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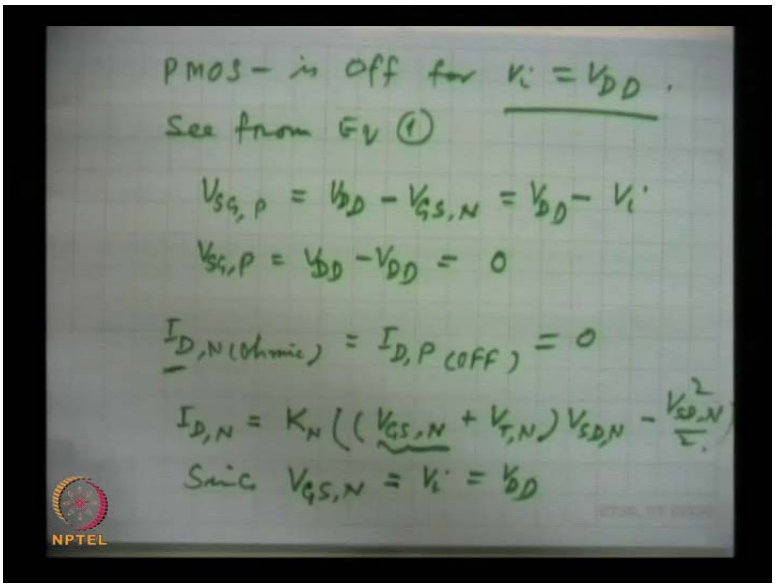

So obviously, V 0 has to be equal to Vdd and this is what we are getting similarly, in this case when this is high input is high this will be conducting and once this is conducting very low impedance. So, then this output once it is conducting, this will be very close to 0 and this is what we are going to have. So, under this condition and Vi is Vdd then and Vdd is greater than Vt. So, in this case NMOS will be on and it operates, operates in the linear ohmic region, but Pmos let us see this is the state of the N mos, NMOS is conducting then what about the P mos, P mos we will see is cut off Pmos is off for Vi equal to Vdd and this we can see from equation one, which was Vsgp this is equal to Vdd minus Vgsn and Gsn is Vgd is Vi and Vi is Vdd.

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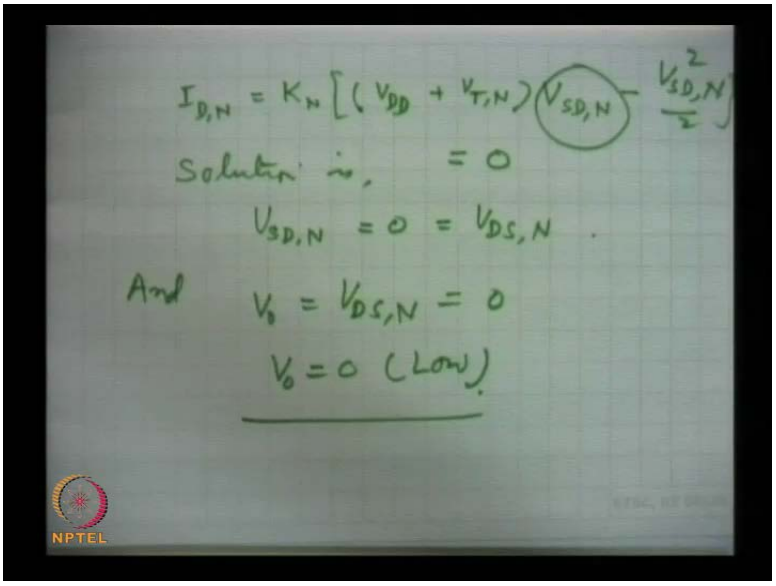

So, Vsgp this is Vdd minus Vdd which is 0 therefore, therefore, this is off Pmos is off, but because of the fact that both are connected in series Idn ohmic should be equal to Idp off and this is equal to 0 and once we write the equation for the drain current for NMOS, as we did in the previous case. Here Idn this is equal to k for N that was for the P previous time.

When we did and this is Vgsn plus Vtn, Vsdn minus Vsdn square by two and since, Vgsn that is equal to input, which is Vdd. So, we replace this by Vdd and we get Idn equal to k and Vdd plus Vtn,Vsdn minus Vsdn square by 2 this is equal to 0. And the solution of this equation is solution is that Vsdn is equal to 0, this has to be 0 only then because other quantities are not 0.

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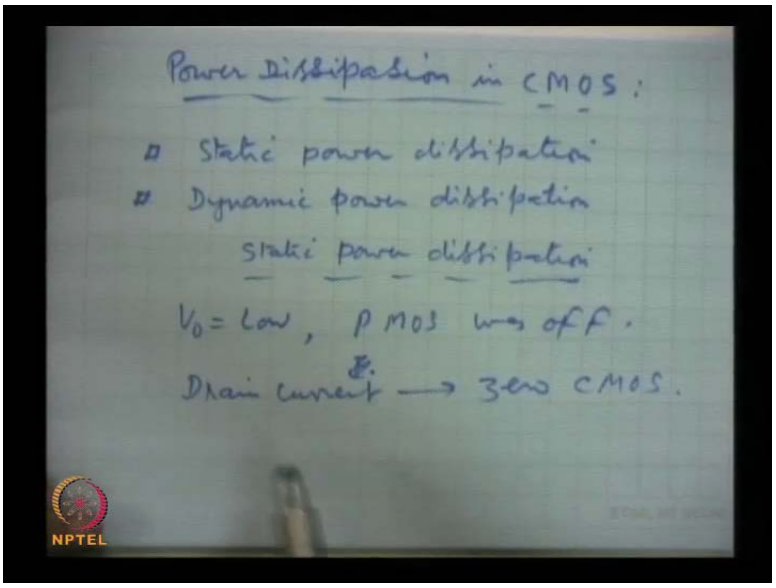

So, we ascend is 0 and this is the same as v d s n and what was output you will remember that output v 0 was Vdsn and this is 0. So, output is low this is the working of CMOS. When the input, this input is low output is high and when input is high output is low, this is what we get here and that is how a CMOS the complimentary mos inverter works. We said that dissipation in the CMOS is least. Let us discuss that point power dissipation, power dissipation, power dissipation and power consumption are one and the same thing in electronics. Power dissipation in CMOS and why power consume is equal to power dissipated because in equilibrium whatever, power that transistor is dissipating.

That is the heat which is being generated by power consumed if for example, heat dissipation is less then temperature will go on increasing and finally, there will be a thermal runway and the device will burn. So, always power consumption is same as power dissipation. So, now, we consider that why power dissipation in CMOS is least. There are two ways the power there are two types of dissipation one is static power dissipation and the other is dynamic power dissipation, dynamic power dissipation we take one by one. So, first we take is static power dissipation. Static power dissipation occurs, when these MOSFETs they have change states they have changed the states for example, from high output to low output or the visa versa.

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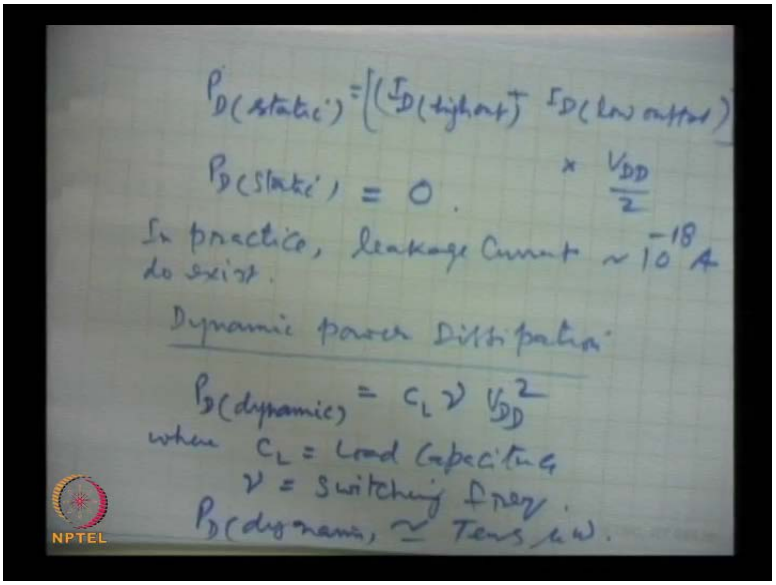

So, the states have already changed. So, what is the power dissipation at in it that in that changed state that is called is static power dissipation. Now, we have seen that in when the state changes for example, from low when V out is low in this case Pmos was off and the drain current Id in the CMOS was 0. In fact, for the total drain current 0 was 0 in the CMOS and similarly, when it changes state the other way then, then the drain current was still 0 in either case this is off this is on, but drain current is 0 or when this is off this is on is still the drain current is 0. So, the is static power dissipation P d power dissipation, we write normally as P d is static and this is the drain current in the high output case.

This was 0 as we know and Id low output. In this case as well this was 0 and this is to be multiplied by Vdd by 2. So, currents being 0 so, P d is static is 0 because the drain current, when the states have already changed the drain currents as 0, but there are in practice, in practice leakage current of the order of ten to power minus eighteen amperes very small current they do exist, this is about static power dissipation.

Now, the dynamic, the dynamic power dissipation. Dynamic power dissipation we said above that when the MOSFETs have changed the states then the drain current is 0 and that give the static dissipation to be 0, but dynamic power dissipation occurs when, both these MOSFETs they are changing its states. During that transient period when the states are being changed from on to off or from off to on then for that short period, the current drain current flows in the CMOS and that accounts for the dynamic power dissipation I repeat that in the dynamic power dissipation.

When MOSFETs are changing its states from conducting to non conducting and non conducting to conducting then during that the small transient time, the there is a drain current and that gives the dynamic power dissipation and it can be shown that P d dynamic is equal to c l mu into Vdd square where c l is the load capacitance at the output. What is the capacitance? All circuits have inherent capacitance associated with them.

So, the c l is the load capacitance and mu is the switching frequency, switching frequency and so, this is the dynamic loss and this is actually of the order of few tens of P d dynamic, this is of the order of few tens of micro watts very small. So, the static dissipation is close to 0 and dynamic dissipation is of the order of few tens of micro watts per circuit per inverter for example, and that if we combine the two. We if the total power dissipation is extremely low and this is the logic this is I am repeating this statement that CMOS logic demonstrates least power loses. Now, this is about this module on MOSFETs and fets. Let us take few numerical examples.

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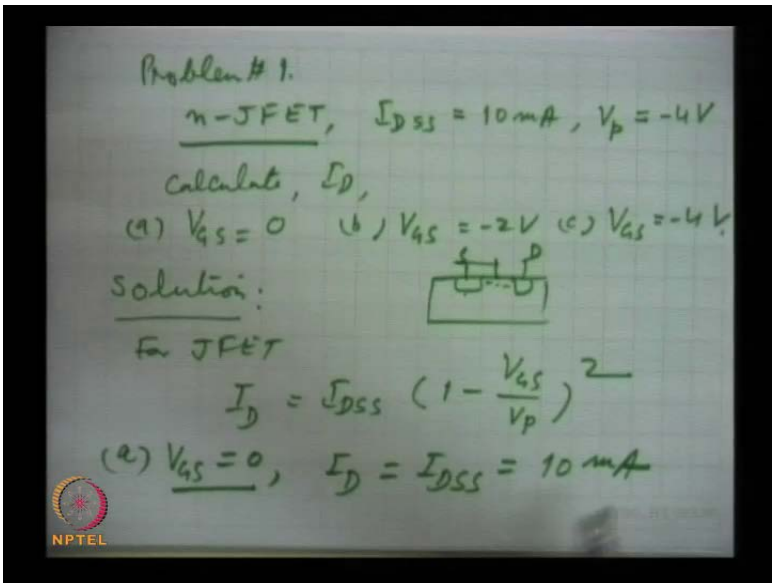

And then I will summarize, what we have done in this unit as a first example let us take problem 1 for an n junction field of a transistor, the device parameters are the source then source circuited current is the highest current in the n junction field, where transistor Id ss this is ten milliampere for the device and V p the punch through voltage is minus four volts you remember the structure of junction field there is a drain there is a source and

the channel is implanted and when the gate is shotted to the source, then the drain current is the maximum. And when we operate this with a smaller voltages more negative voltages.

Then drain current falls. So, in this n junction field of a transistor the Idss is ten milli ampere and punch through voltage is a four volts, then we have to calculate. Calculate the drain current I d for different voltages between gate and source Vgs equal to 0 this is a part b, part Vgs minus 2 volt and then Cvgs is minus 4 volts under these three conditions, we have to find out the drain current when these are the parameters available. Now, we talk about the solution; obviously, the that the device is working in the saturation region, where for JFET the drain current is given Idss 1 minus Vgsvp square.

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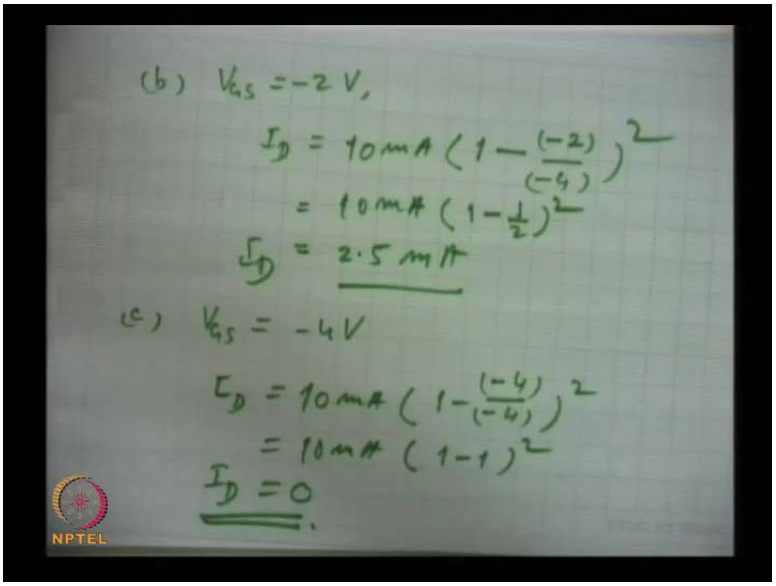

This equation, we are suppose to use we have to find out I d for various gate source voltages where Idss is given as ten milliampere and let us first see part a when Vgs is 0. So, this term is 0 and this is I d in this case the drain current is equal to Idss which is given as ten milliampere and this is of course, understood it is well understood because the gate source voltage is 0 here, this is drain source and this is drain and this is the channel then the gate is shotted Vgs is made 0 that is the maximum current which flows in the device.

So, this is this then when Vgs, b part when Vgs is minus 2 volts in that case Id again in the same expression, we put the value of idss that is ten milliampere into 1 minus the

voltage is minus 2 volts and this is minus 4 volts square and. So, this is equal to 10 milliampere 1 minus 1 by 2 square, which gives this to be drain current is 2.5 milliampere. So, when the gate was shotted to source, the drain current was ten milliamperes and when it is given a voltage of minus 2 the drain current is reduced to 2.5 milliamps and case three and Vgs is equal to minus 4 volts. In this case the same expression I d, Idss is ten milli amperes here 1 minus, minus 4 by minus 4 square.

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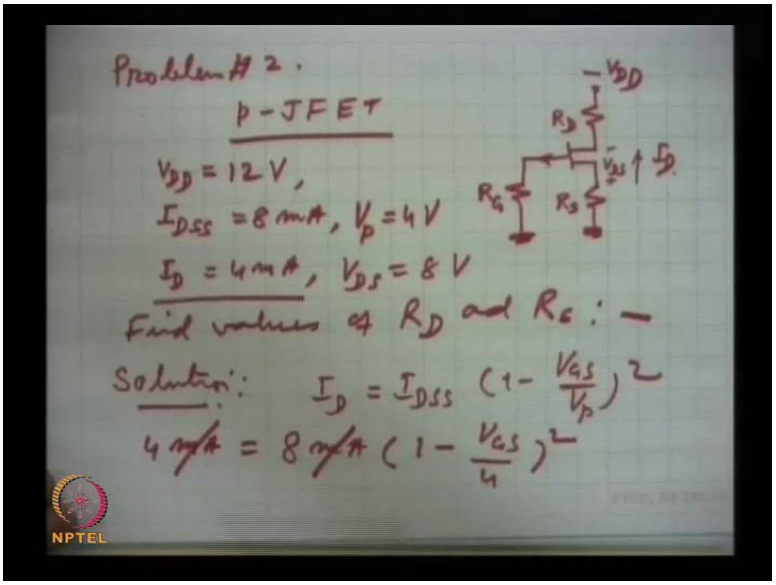

So, this is 0 1 by 1, 10 milliamperes 1 minus 1. So, this is 0 I d is 0 this is also understood actually because for the device the pinch off voltage was 4 and this is that, where the current reduces to 0. All these points you can see from the drain characteristics that when gate source voltage is 0, maximum drain current for the n type JFET flows and when this is made negative Vgs is made negative current falls and when Vgs is made equal to V p the magnitudes are same then the drain current reduced to 0. So, this is the solution of the problem. let us another problem this is problem 2 there is a circuit which makes use of P-JFET and the circuit is this is R d this is R s this is R g and this is minus Vdd.

Because it is P type junction field of a transistor and the current flows this way here. So, here what is available is that Vdd is 12 volts sign is provided here. So, it is actually minus 12 volts magnitude is 12 volts and the drain current Idss is 8 milliampere and punch through is 4 volts and I d is 4 milliampere and Vds. When the 4 milliampere

current flows Vds this voltage here this is equal to I can show it here Vds, this is equal to 8 volts we have to find out the values of these two resistors. Find values of resistors R d and R s this is the problem. Here this is the circuit and this is a P-JFET which has Idss is 8 milliampere and V p has 4 volts in the circuit this battery is 12 volts.

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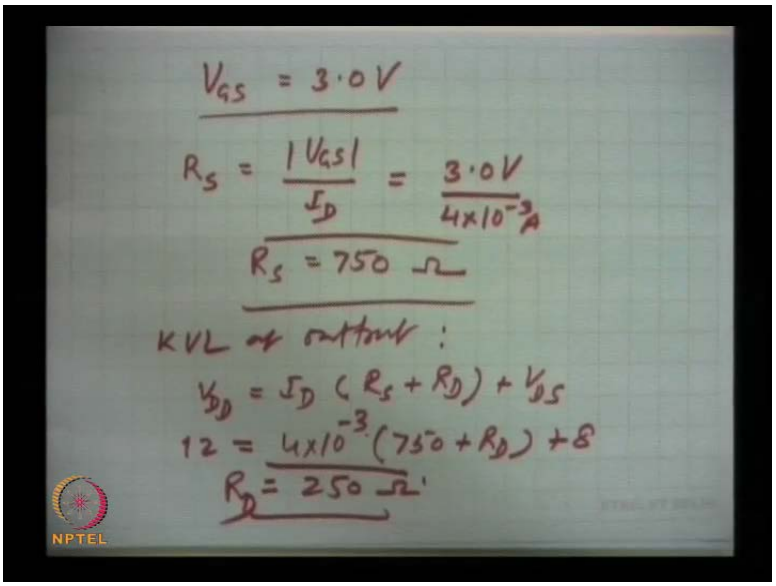

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And the drain current of 4 milliamperes gives a voltage drop of 8 volts here. So, what is the value of these two resistors R s and R d that we have to find out. So, the solution of this we again, use the same equation the drain current is Idss 1 minus Pgs minus V p square and it is given that I d is 4 milli amperes. So, 4 milli amperes Idss is 8 milliampere 1 minus Vgs minus V p is four and we can find out the value of the only unknown is Vgs. So, this milliampere, this milliampere is cancelled and is very simple calculation from here we get Vgs this is equal to 3 volts Vgs, this is 3 volts and you will remember that it say it say self bias circuit.

So, this 3 volts is to be provided by this resistor R s. So, once we know Vgs is equal to 3 volts then we can get R s resistor is equal to Vgs. The magnitude of Vgs by I d that will give the value of resistance. So, this is three volts and I d is 4 milliamperes; that means, minus 3 amperes this gives R s equal to 750 ohms, we are find out the value of R s and to find out the value of R d this drain resistor, we have to apply the we have to sum up the voltages in the output circuit. Here we sum up the voltages and that will give KVL

kirchoff's voltage law at output, when we apply we get Vdd equal to I d, R s, R d plus Vds this is given twelve, twelve this is 4 I d's 4 milliamps.

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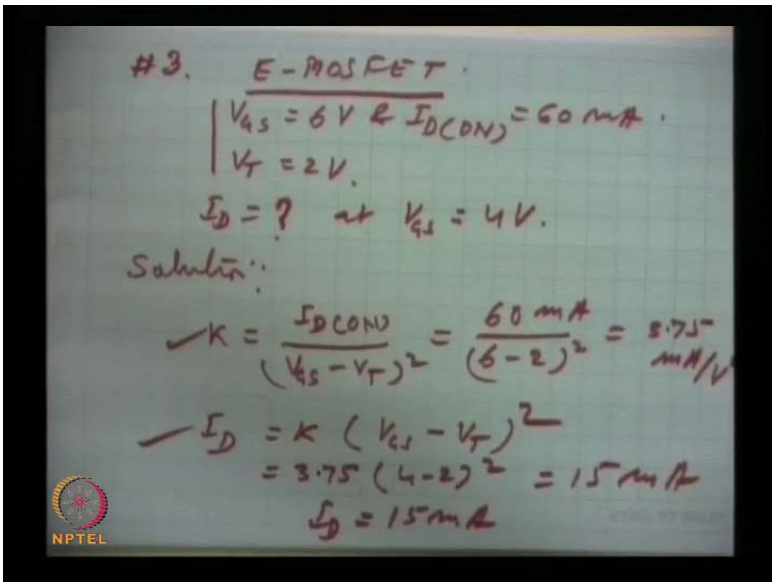

So, minus 3 amperes into 750 ohms plus R d plus this is 8 volts we solve for R d and R d comes out to be 250 ohms. This is the way we can find out the values of the two resistors R s 750 ohms and R d is 250 ohms. Let us take one more example and let us take this that a EMOS, this is problem 3 E-MOSFET the data sheet is specifies Vgs as 6 volts and I d on as 60 milliamperes V t as 2 volts. Determine the drain current, drain current we have, we have to find out at Vgs equal to 4 volts . So, this is one example we are taking a MOSFET this is the data available on the data the manufacturers give with the data sheet.

And this is what the problem is drain current is to be determined at Vgs four volts. Now, the solution this data we can use to find out the constant k the conductivity constant, conductance constant of the device of the MOSFET this we discussed, when we were talking about the MOSFETs and this constant k. 1 of the ways we can get is through this data and this was given to be I d on Vgs minus Vt square. So, we substitute the values I d on is given as 60 milliampere and this is given 6 volts this is 2 volts square and this gives 3.75 milliampere per root square this is the constant k.

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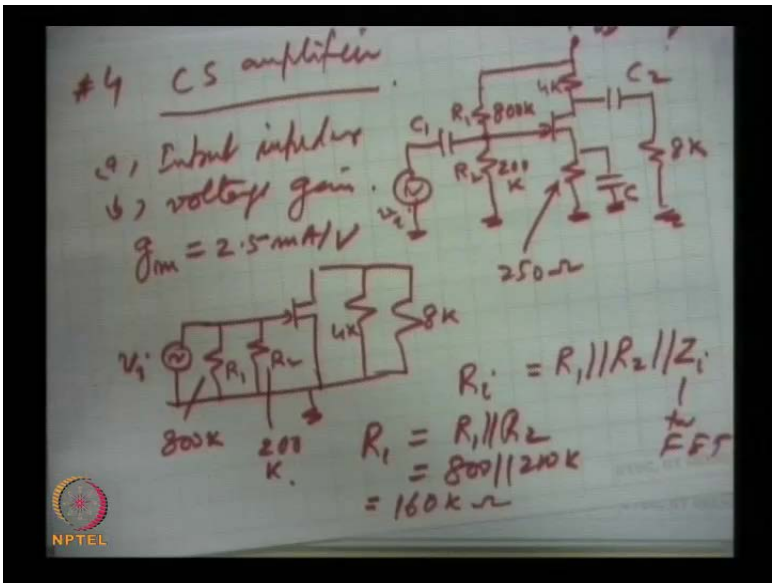

And then for the Emos, the drain current k into Vgs minus V t square. This was the expression that expresses the drain current in the saturation region. When we substitute the values this is 3.75 in milliamperes mind it, we are putting in milliamperes and this 4 volts 2 volts square, then this comes out to be 15 milli ampere. So, I d is equal to 15 milliampere this is what, we have we were suppose to determine. So, this was the problem on E-MOSFET and similarly, it can be on D-MOSFET and such expression can be used there to last example another this is on the amplifier common source amplifier last and fourth problem this is a common source C S amplifier.

This circuit is this, this is R 1, R 2 this is 800 k this is 200 k kilo ohms and this is R d which id 4 k and R d and this is 250 ohms and this is also bypassed and the output is taken here, this is the load of 8 k output is taken here and this is plus Vdd equal to 15 volts. So, here two things are to be determined this is the circuit where all parameters are known and we have to find out. What is input impedance and voltage gain voltage gain? First we draw the this is the input Vi and output is taken here first we have to draw the A C equivalent for that D C voltage source is have to be grounded and these coupling capacitors c 1 and c 2 are of sufficiently large value.

And they have to be taken as short at the frequency for which the amplifier is meant and this is bypass capacitor C that is also large and this will be shorted. So, we can draw a simple equivalent A C circuit, this is 8 k this is 4 k and this is all grounded this is the

equivalent circuit this is R 1 this is R 2 this is 800 k and this is 200 k. Now, first the input impedance, input impedance we are seeing in the equivalent circuit that they are coming in parallel and to this will be what is the impedance of the amplify of the device itself, then the input here. So, the input impedance of the amplifier is R 1 in parallel to R 2 in parallel with the Z i of the device.

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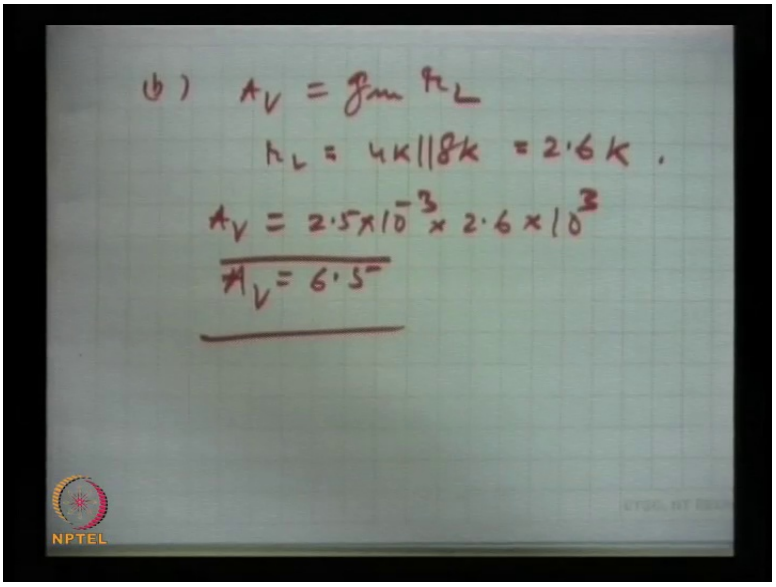

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This is for the FET which is very high and remember that in parallel combination very high resistance is can be neglected. So, this is actually R i simply R 1 in parallel with R 2 and this is 800 k parallel 200 k. So, this comes out to be 160 kilo ohms. This is the input impedance as we will measure here and then gain the g m was given for this actually, which i just forgot to write that g m for the device is given 2.5 milliamperes per volt and which is also written as a as a milimoles. So, part b the gain A v which is simply g m into R l effective load, effective load is the parallel combination of these two.

So, hence R l in the present case is 4 k and 8 k and that comes out to be 2.6 k. So, then A v becomes 2.5 into 10 to power minus 3 that is the value of g m and into 2.6 k. So, this is 6.5. The voltage gain for the common source amplifier is 6.5. So, these are the few typical examples which I took for the numerical problems that finishes our this unit. And here what we have done, we started with the junction field of a transistor, we gave how it

is constructed, what are, what is the structure of junction field of a transistor, how does it work, what are its I v characteristics, then we went for MOSFETs.

And MOSFETs the D-MOSFET depletion, MOSFETs, MOSFETs and enhancement MOSFET, depletion MOSFET can be used as indepletion mode as well as in enhancement mode and enhancement mode there is nochannel existing in the beginning, but the applied voltage at the gate creates the channel and enhancement mode then the, correct the we developed a model for the transistor.

Which is applicable for junction field of a transistors and for FET and also the we analyzed the three amplifiers common source amplifier is most widely used and common and drain is like emitter follower, which is used for matching purposes and then we took CMOS devices and we indicated that CMOS gives the lowest loses very high speed of a switch in and most advanced circuits are made in CMOS. So, this is this module is all about.