FETS and MOSFETS

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Module No. # 05

Lecture No. # 05

Self Bias (Contd.) Design Procedure

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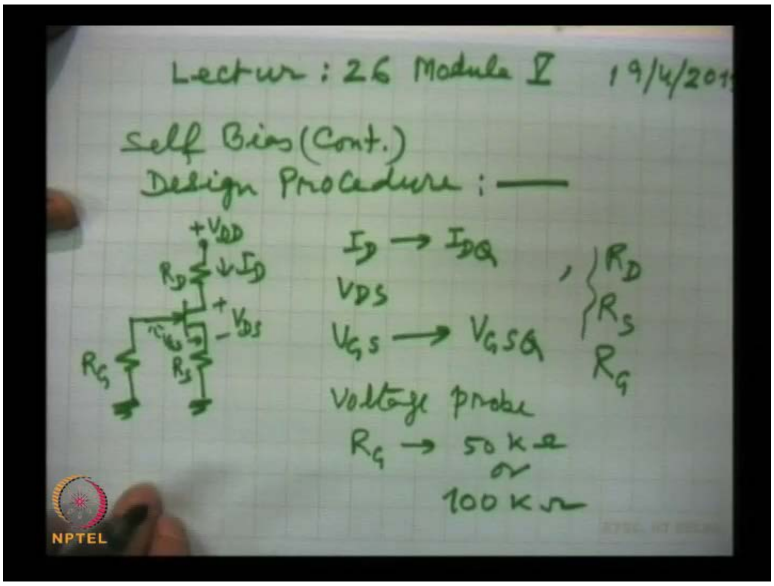

We continue our discussion, on self bias. Now, we take some design procedure that is how to know the components the values of various a resistances and voltages and current in the self bias circuit this comes under design procedure. So, let us consider first the circuit the simple circuit which we were discussing was this

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This was the self bias circuit and design implies that we should know the value of current I D at the Q point. So, this actually we write as I D Q at and the voltage V D S and this a gate source voltage V G S and at the Q point this is also to be noted and this we shall write V G S Q, Q point the quotient point or operating point. We have to decide and a since mostly these procedures which we are doing they are going to be adapted to make a amplifying circuit out of a MOSFET or junction field effect transistor. So, from the characteristics, how we arrive at this values that we will see. And then we require the value of this resistance R D R S about R G we have already talked R G is a there is no current flows through this resistance.

So, actually, R G this probe this is a gate terminal acts as a voltage probe a voltage probe has to have a very high resistance. So, normally, R G is taken 50 kilo ohms or 100 kilo ohms. So, this we say now this is known the these two resistances have to be determined for the circuit and that will be governed by the drain characteristics what are what type of drain characteristics drain characteristic tell us the amount of drain currents which flow in the circuit and what are the various voltages. So, this all comes under design procedure and we proceed to find out these values.

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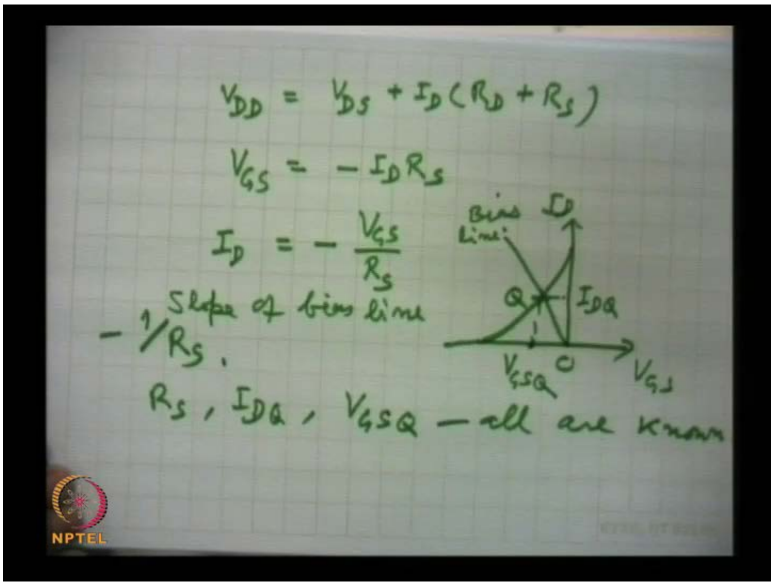

Now, the two equations we arrived earlier, by simple summing up of voltages these equations where V D D equal to V D S plus I D R D plus R S this was 1 equation, which comes simply when we sum up voltages in the output circuit. Another equation is obtained when we sum up voltages here and from there came the equation V G S equal to minus I D R S this can be return in the form I D the drain current is equal to minus V G S by R S this is the equation of a straight line. And when this a straight line is plotted on the trans conductance curves of the device. That is this is trans conductance curve and this is the line when to be plot on this is like that this is called bias line and the slope it is slope of bias line gives the this depends on the value of R s.

So, if we choose R S that will shift this slope; that means, thus base line will move across this point. So, once we choose the operating point Q than we know the slope and thus R S is known. And from these curves we also know the value of the drain current at Q point and V G S at Q point. So, three parameters are known R S the resistance in the circuit is known that will be determined by the slope and slope is dependent on where we choose the operating point. So, normally we choose somewhere, in the center enhance the slope will give the value of R S and this slope of the line is actually minus 1 by r.

So, this will give the value of R S. And at the operating point what is this drain current and what is this voltage? Now, few points we discussed, when we were discussing, the bipolar transistor and it is circuit. Than, we will recall from there that these are the DC values and normally in an amplifier we will use AC signals. So, the variation of current will occur taking this DC value at it is a center. So, the variations will be this is the DC value than AC variations will be along this. And similarly, the input voltage is the gate source voltage.

So, when superimpose AC signal on this than these variations will occur a across this Q point value of the gate source voltage. So, this way three parameters are now known the I D Q V G S Q and resistance R all are known than the this V G S and this I D this will give you actually, the value of a V D S at the Q point also let us, see the output characteristics the drain characteristics they, where like this.

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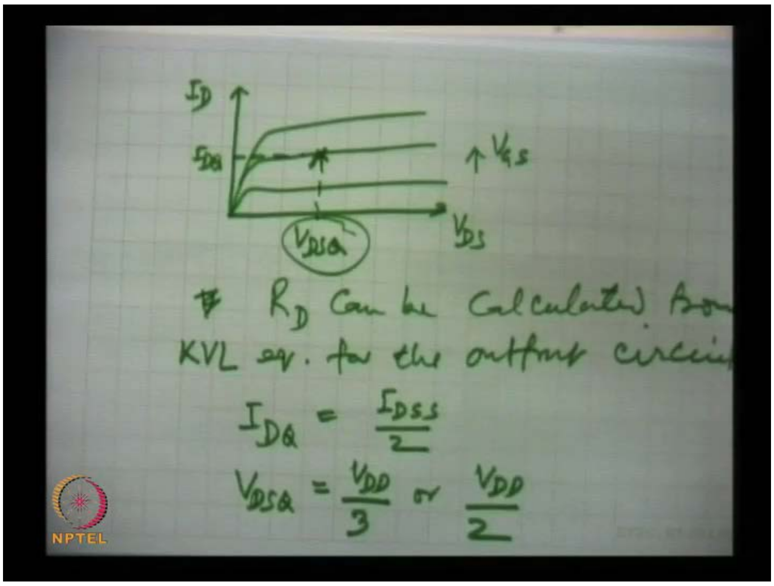

This is V G S V D S I D and if we choose the operating point say for example, here than this is I D Q the same as we have we got I D Q here. So, that we mark here and from we extended and we get V G S Q I D Q and this is V D S Q. So, once V D S Q is known the battery, which we use in the circuit this, which is the single D C source in the circuit normally for the devices. This is the currently used integrated circuits make use of V D D of 5 volts, when discrete devices are use than this voltage can be a high can be 10 or 12 15 30.

So, this way V D D is known and then we use this first equation which we have we had written this one this equation here now I D Q is known R S is known so this is known, this is known and V D S Q is known V D D that is the battery source, which we are using that we a anyway no. So, this way R D can be calculated. So, this way we find out all the parameters of the circuit the R D can be calculated from Kirchhoff's voltage law equation for the output circuit. Now, I D Q and D S Q this is I D Q this is D S Q they are taken here from the these, a drain characteristics there is another procedure, which is a often employed and that is it is the thumb rule that I D Q can be safely taken as IDSS by 2.

So, wherever, the largest current a through the device this parameter is normally, given by the manufacturer. So, once it is known, when it is safest to take I D Q as half of IDSS similarly, V D S Q can be taken as one third of V D D or even half of this. So, this way instead of a using these characteristics I D Q and V S Q can be known from here. So, we have determined all the parameters of this circuit R D R S V D S I D V D D and R G and that is the completed design of the self bias circuit. Self bias is often used for a junction field effect transistor and it can also be used, where negative V G S is required in the p MOSFETS particularly.

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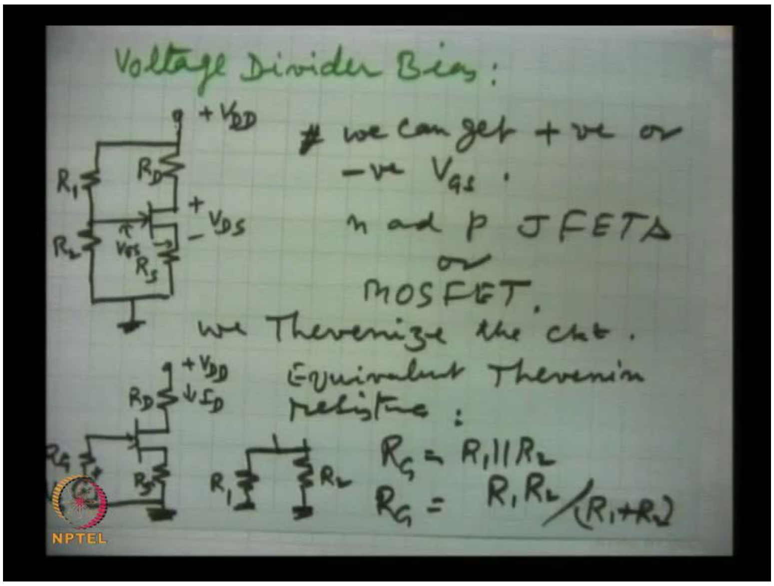

Now, the another biasing circuit is voltage divider bias it say broader circuit and infect it can be used for getting positive or negative gate source voltage both can be by adjusting proper resistances this can be use. So, this is having a wider use and of course, for e MOSFET this is the one, which is used. Now, the circuit is this is a V D D this is R D R S R 1 and R 2 here this voltage V D D is divided this network R 1 R 2 this x as a voltage divider. So, that is why the name voltage divider here this is V D S and this is V G S and this can be used, because we can get this an important. We can get positive or negative V G S therefore, it can be used for n and p JFET'S or MOSFET'S any kind of MOSFET, this circuit first we Thevenize it and the Thevenized by applying.

Thevenize theorem we Thevenize the circuit and what we get is this the Thevenized circuit is this. This V D D and this is the resistance we will equivalent the Thevenize equivalent of this two resistances we will tell that how this is determined and this is the voltage source V G this is I D R D and this is R S. This is Thevenize equivalent circuit and here the value of a equivalent thevenize resistance. Just you remind you that by applying Thevenize theorem we can find out this resistance than this resist for this resistance this D C source is to be grounded now, what is the equivalent resistance between these points between this and ground.

So, that is to be determined now once we ground this terminal also this terminal also than this is like this. This is R 1 this is R two so, as for as this point is concerned this Thevenize resistance are this is equal to the parallel combination of this two resistances, which is R G is simply, R 1 R 2 by R 1 plus R 2 this is thevenize equivalent resistance. The voltage is what is the voltage? Which this, V D D produces between gate and source.

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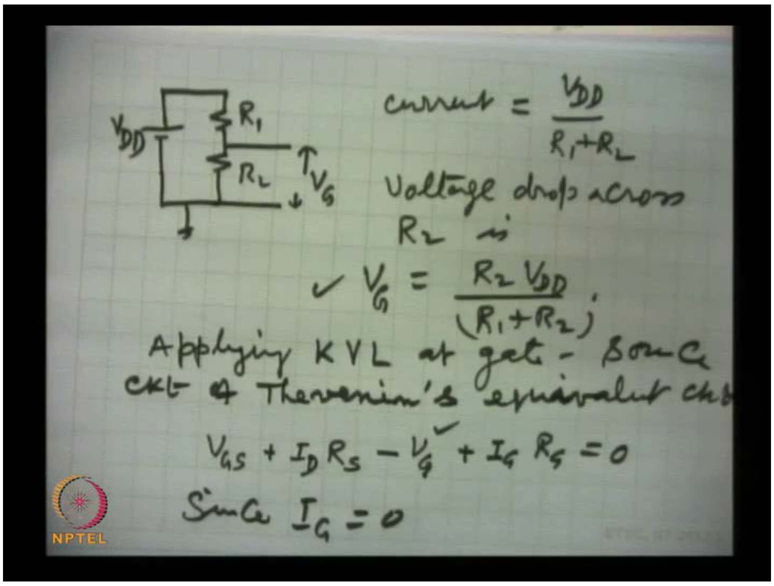

So, the equivalent circuit actually, will be this, this is V D D and this is the two resistances this is R 1 this is R 2 and here we have to find out this is V G. So, obviously, the DC current through this circuit is the current is V D D by R 1 plus R 2. And the voltage drop across R 2 is simply, that is V G is simply R 2 V D D this current into this resistance so R 2 into this current so R 1 plus R 2 this is V G. Now, once this is a there this current we take as I G and we apply the summation of voltages that is Kirchhoff's voltage law in the gate source circuit of this. So, applying Kirchhoff's voltage law at gate source circuit of Thevenize's equivalent circuit we get the equation V G S plus I D R S minus V G plus I G R G is equal to 0, here this is V G S.

So, we start with we are finding out the summation of voltages we are writing the equation for summation of voltages in this circuit. So, V G S than I D into R S than minus V G plus I G and R G equal to 0 where this V G is given by this expression and a I G here is a 0. Since, why I G is zero? Because all gates are operated in reverse bias, so, I G is 0 and then we get from here when we put.

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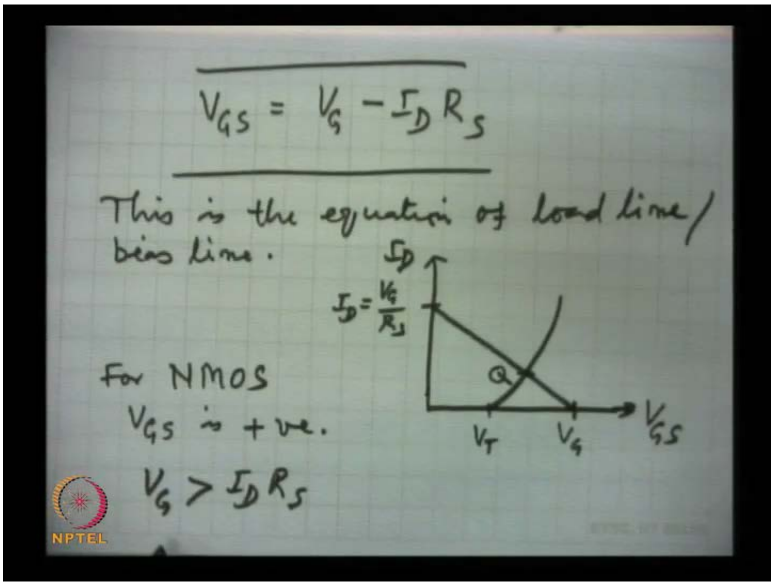

So, this term goes and we simply get V G S is equal to V G minus I D R S this is the fundamental equation. And this clearly shows, that V G S the gate source voltage can be obtained either negative or positive, if it is to be positive than V G must be greater than I D R S the drop across this resistance should be smaller than V G that will give positive value of V G S. Or if negative value is decide than the drop across resistance R S has to be higher than V G. So, this is actually, this is the equation of load line or call it bias line and this is to be plotted on the transfer characteristics of the device to find various important parameters. So, when we plot these here these are the characteristic this is V G S I D the output current and input voltage gate source voltage.

And this is the equation of a straight line from here at this point V G S is 0, when V G S is zero than current I D from here we will get I D equal to V G by R S this is the point and to get this point here I D is 0. So, this is the point, which gives the value of V G and where this a load line crosses cuts the transfer characteristics this is the Q point. And a now we will proceed to find out for example, what is how to get negative and positive voltages first let us take for N MOS on N MOSFET where, V G S is positive and for positive from this equation base line equation load line equation V G has to be greater than I D R S. We substitute here the value of a V G value of V G is here in this equation. So, this we substitute here and let us, see what we get.

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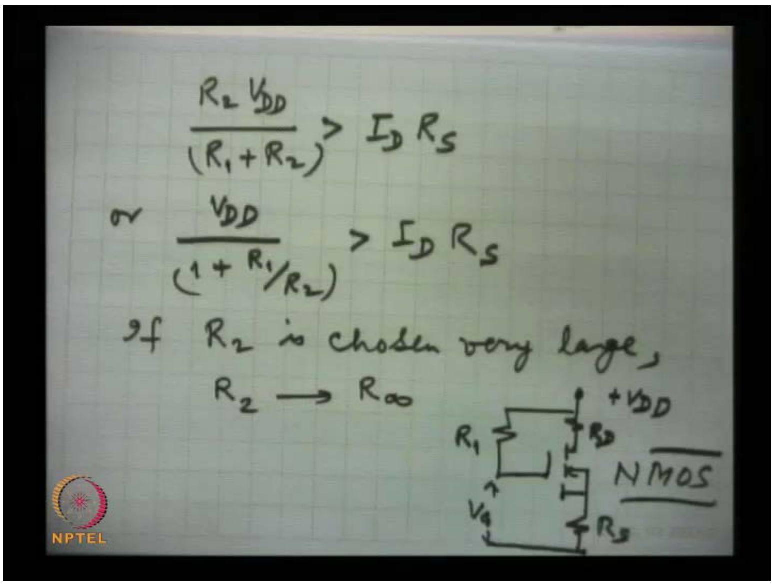

So, when we substitute the value we get R 2 V D D by R 1 plus R 2 this should be this should be greater than I D R S or V D D by 1 plus R 1 by R 2 should be greater than I D R S. This in equality can be satisfied; obviously, if R S is choosen very large, if R S R 2 is chosen very large than this in equality can be easily satisfied in the limiting case R 2 in this circuit in the voltage divider circuit R 2 can be taken as infinity. Almost approaching infinity and infect it can be taken as infinity a approaching R infinity in what is R infinity, the absence of the resistance. If R 2 is removed from the circuit, than we satisfy this in equality easily.

So, the circuit is reduce to this we remove from here R 2. So, that the circuit is this is N M O S this is R S and this is R 1 this is V D D and this is R D. Here we will absorb V G this is the circuit biasing circuit just one resistance here instead of in the self bias the resistance was here. So, we can bias we can get a positive gate source voltage, which is required for example, for N M O S here this is N M O S and if we intent to get a negative voltage.

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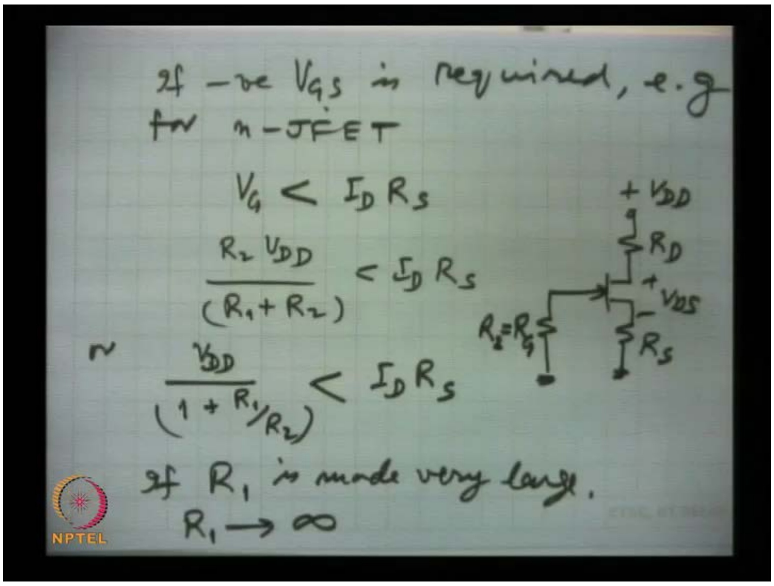

When negative gate source voltage is required negative V G S is required for example, for biasing n JFET or p MOS than, V G has to be smaller than I D R S and when we substitute for V G. We get is less than I D R S or V D D 1 plus R 1 R 2 this is this has to be less than I D R S this equality in equality can be satisfied, if R 1 is very large, if R 1 is made very large and in the limiting case R 1 can be infinitely high. That means, if we remove R 1 than we will get a negative gate source voltage and the circuit will be the same as we have got for self bias that is the this circuit will be reduced voltage divider bias, if we remove this resistance R 1 here to make it infinity that will reduce this circuit to this form.

We are this is V D D, R D, R S and this voltage this is of course, V D S this is V G S and this is R 2, which is same as we have taken earlier R J. So, this is the circuit to get a negative gate source voltage from the voltage divider bias and we can get the positive also as we have seen in the previous case. So, this way this voltage divider bias can be used and this is the one, which is a quit widely used with the most devices and a thus we finish the biasing of the FETS and MOSFETS any kind of FET junction field effect transistor or MOSFET can be biased in by using these two biasing networks.

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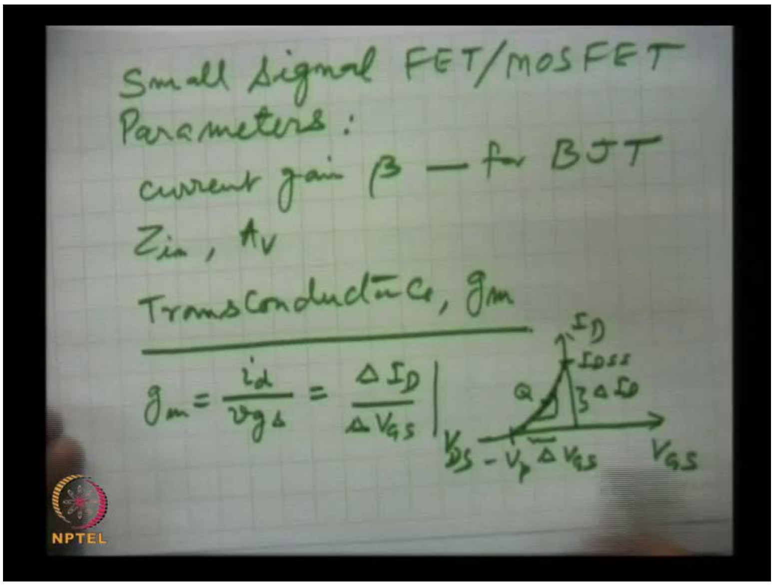

The next thing, which we are going to have that is a small signal of parameters, a small signal F E T or MOSFET parameters this we are going to a study now for V J T. We have seen that a beta the current gain beta for bipolar junction transistor B J T was most popular and this was the ratio of output current to input current. This parameter beta appear in the expressions for input impendence z in or voltage gain and. So, on field effect transistor or MOSFETS they are voltage operative device here the important parameter is Trans conductance of the device, which is written as G M.

So, G M Trans conductance parameter is a most important parameter for a junction field effect transistor or for MOSFET. And first we will define it and then we will go for other is no signal parameter. So, Trans conductance G M this is defined as, because we will be concerned with the ac operation of the device. So, we can define the AC drain current by a c. So, when on the Q point when we superimpose the signal what is I D and V G S the ratio of the two, which can be shown equal to let us, see for first for A F E T the J F E T here this is the Trans conductance curve and a this is a V p and this is I D this is V G S.

So, this curve is the Trans conductance curve and at the operating point, we draw a small tangent and we find out, this is change in the drain current I D and this is the change in a gate voltage. So, this ratio can be return as change in ID by change in V G S at constant V D S this is the way it is defined. Now, this is obvious that, if we choose Q point here here here here than every where G M is changing and G M is highest near this I D D S show circuit drain source current when gate is shorted to source. This is the highest value and the slope is highest here. So, he re this G M will have highest value the highest value of G M is a designated as a g m o this is the highest value of G M.

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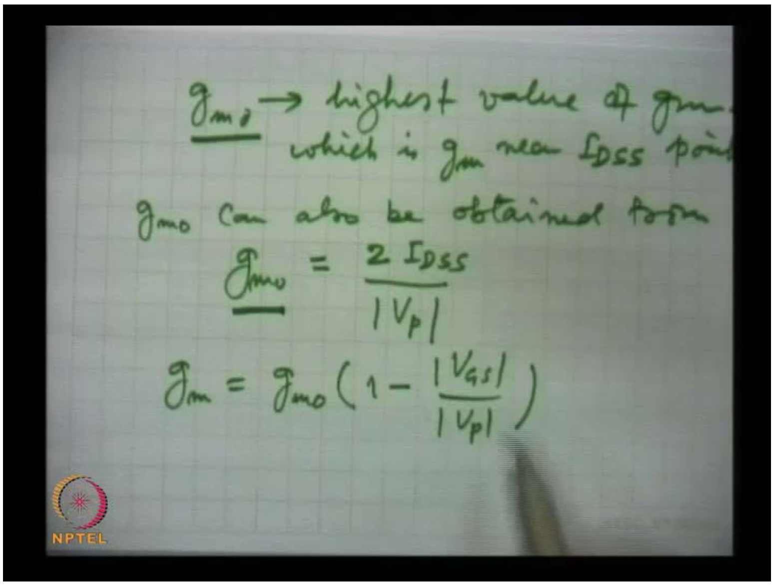

Which, is actually, which is the Trans conductance value near IDSS point on the trans conductance curve. Now, g m o can be determine as we are seeing from the trans conductance curve here by taking this operating point in the visinity of IDSS or it is g m o can also be obtained from the simple relation g m o is equal to 2 IDSS by V p from here also g m o can be obtained. Now, once g m o is known either from that graph directly or by using these two parameters. Than we require Trans conductance value at the operating point and as I said because the slope is changing. So, G M is changing quite a bit along the Trans conductance curve.

So, for accurate analysis at the Q point the value of G M the Trans conductance is required and. So, from g m o the maximum value, which is either, provided by the manufacturer or can be obtained from the data provided by the manufacturer. We can find g m for any value of V G S depending on our Q point. We can get from here this is the equation, which can be used to get value of trans conductance parameter from g m o by substituting the value of at what gate source voltage we require this value. We can get from here where here this is the pinch of voltage.

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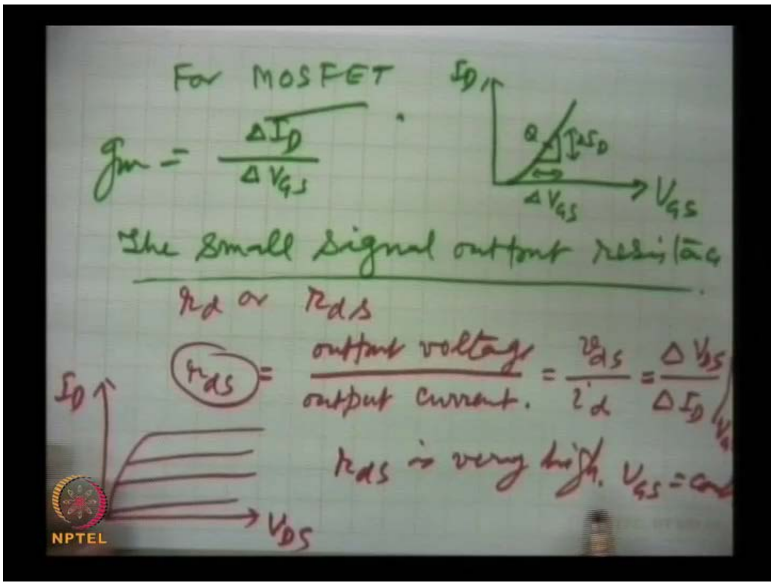

This example we took for is graph we took for a J F E T for M O S F E T the curve will be like this and here we choose the operating point and we draw. So, the same thing we get the value of I D change in I D and this is the change in V G S the ratio will give g m for M O S F E T at the Q point. The another a small signal parameter, which we require and that is the small signal output resistance this is a defined, as it is return as either R D or as R D S. This is actually, the resistance of the channel in the circuit and this is defined, R D S is equal to output voltage by output current that is V D S AC value of the drain source voltage and the AC drain current, which is same as changes in V D S by changes in the drain current at this is constant V G S constant. This is actually, if we look at the drain characteristics this was I D and this is V D S than this resistance represents this slope of the drain characteristics in the saturation region.

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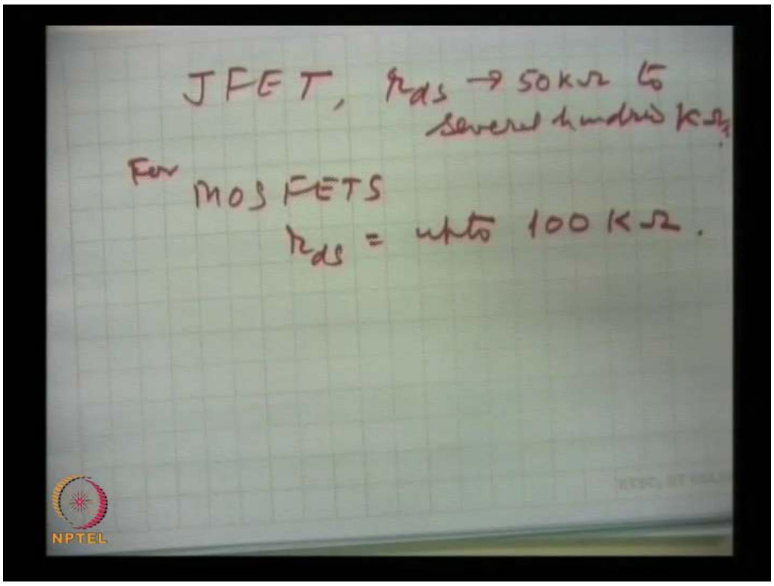

Which is a nearly, horizontal and that state that r d s is very large very high and for J F E T, R D S or simply R D this is 50 kilo ohms to several hundred kilo ohms and for M O S F E T S r d s is up to 100 kilo ohm. Actually, when we take the circuit actual analysis we will see that normally, a smaller resistance will be put in parallel with this r d s. So, r d s effect that way will be negligibly a small. So, this two most important parameters we discussed, one was trans conductance, which will appear for example, we want to know what is the voltage gain of a M O SF E T amplifier than their essentially one of the parameters, which will appear is a trans conductance parameter. And then we discussed, about the a small signal output resistance of the device and that is normally, very high for J F E T or for M O S F E T the next thing, which we take that is a small signal F E T model.

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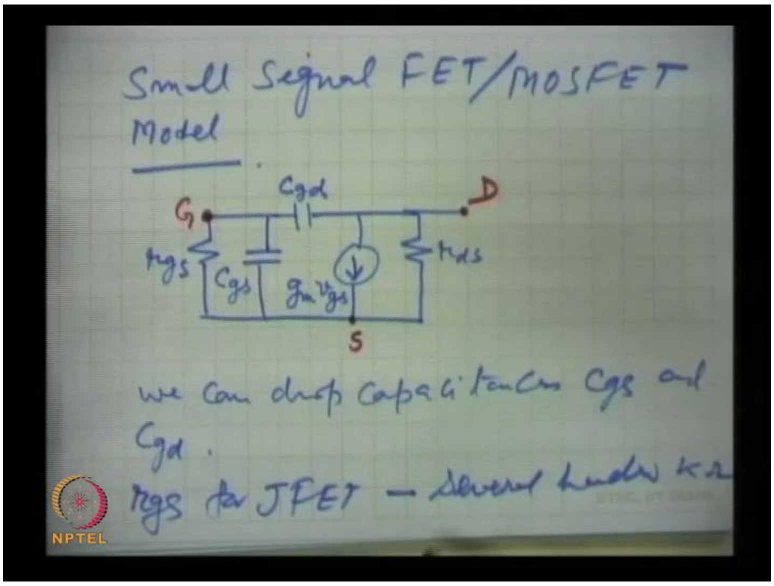

A small signal F E T and also the same model for M O S F E T, when we were discussing, the bipolar transistor and it is a model we have already seen the utility. In a circuit, when the device is replaced by it is modal that unables the analysis by using simple algebraic equation summation of voltages etcetera or current. We can find the value of output voltage versus input voltage, which will be the voltage gain similarly, if input impendence is to be determined or any other parameter is to be determined than a small signal modal is very useful.

So, we are now developing a small signal modal for F E T, which also applicable for M O S F E T S. Now, any two conductors when separated with a dielectric insulator there is a capacitance associated. So, when we talk of the exact modal of the device there are several conducting paths in the device there will be capacitances. For example, between gate and source there will be a capacitance similarly, between gate and drain there will be a capacitance. So, if we talk of the exact module, which we will simplify of course, we will have to take into a account these capacitance and all kinds of resistance. So, the modal for the device will be this.

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This is the gate terminal gate terminal here and this is this whole is source and here is drain this is that a output is resistance. Which we talked R D S and this is the current source and this is g m into v g s and this is the capacitance between gate and drain and this is the capacitance between gate and source and this is the resistance between gate and source. This is the exact modal, but we can simplify for example, we are taking of moderate frequencies and this frequencies will be normally up to few tense of kilo Hertz. They are these impendence offered by this two capacitances they are very high and very high impendence’s becomes almost they can be taken out from the circuit.

So, we can drop capacitances C g s and C g d this capacitance’s we can drop for the frequencies, which are currently presently under discussion. Also this resistance between gate and source is very high for j f e t this is hundreds of kilo ohms r g s for J F E T. This is several 100 kilo ohms and for M O S F E T S for M O S F E T S at least two orders of magnitude higher.

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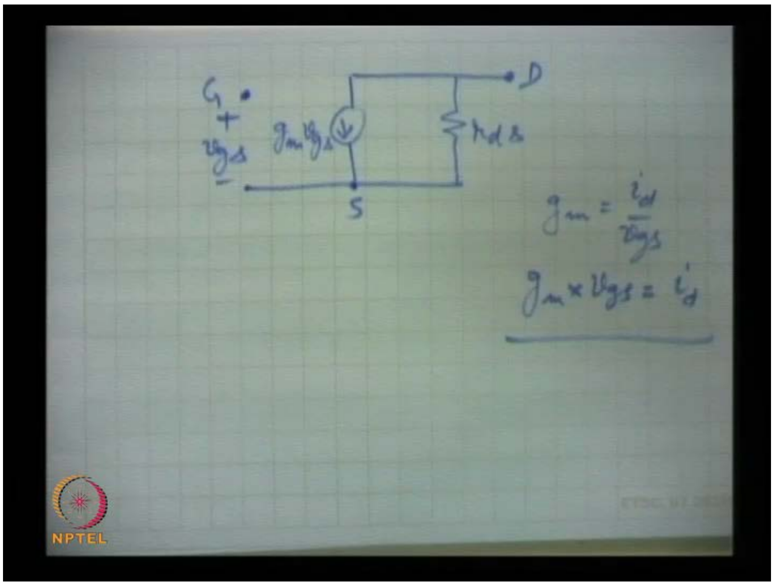

So, this resistance can be also taken out than what we are left is this modal, this is gate terminal, this is source, and this is drain and this is R D S and this is the current source. This has the dimensions of the current source, because g m we know g m is I D versus v g s. So, g m into v g s is equal to I D. So, this is the current source and here and this current source is that the magnitude of this current is dependent on the gate source voltage whatever, voltage we apply here v g s. So, this is the modal, which we will be using and remember it is very simple modal this is one resistance, which we will see when we put actual resistance here, than the two resistances in parallel one very high resistance one low resistance than the effective resistance of the parallel combination will be closer to the a smaller resistance.

So, this will also disappear and so the current source remains and this we are going to use for the analysis of F E T amplifiers. We are going to a study three amplifiers the common source amplifier, the common drain amplifier and common gate amplifier like B J T can be used in three different configurations. So, is the case, with F E T this can also we used for three different configurations. So, we will drive the useful parameters for all these amplifiers using this modal. And we will see that we will come to a net conclusion that like common emitter amplifier in B J T common source amplifier with MOSFETS and a with the FET'S is most widely used and we will be is studying that.