Electronics

Fets and Mosfets

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Module No. #05

Lecture No. #02

FETS and MOSFETS (contd.)

In the previous lecture, we studied the working and fabrication of a junction field effect transistor and we continue the investigations for any electronic device. One of the most important characteristics are current voltage characteristics of the device.

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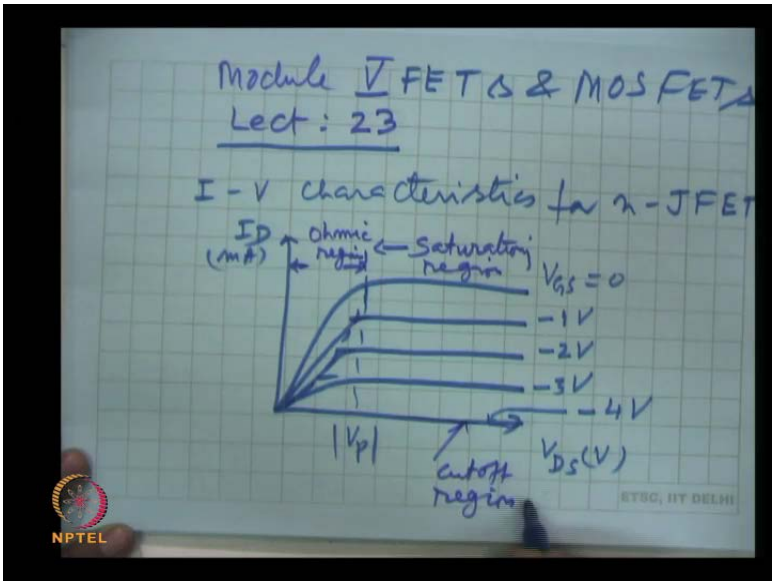

So, we take I V characteristics for n type JFET, we will not a spend time, we will not duplicate their studies by taking P type JFET, because they are identical except at few places as I. Discussed in the previous lecture that the gate source voltage will be positive in the P type junction field effect transistor, while it is negative in the case of n type JFET. So, the characteristics which we have already drawn, they were this.

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This is drain current and this is V D S in volts and this is in normally mill amperes and these are the characteristics. This was V P, the pinch of voltage. And these are the characteristics for V G S equal to 0, this is minus 1 volt, minus 2 volt, minus 3 volt. And here these characteristics we will get for example, for minus 4 volts. these I-V characteristics, the drain characteristics of a the junction field effect transistor, they can be divided into 3 different regions. One is, this region from here to here, this is a ohmic region. From here to here this is saturation region and here this is the, where the drain current drops to 0, that is the CUT-OFF region.

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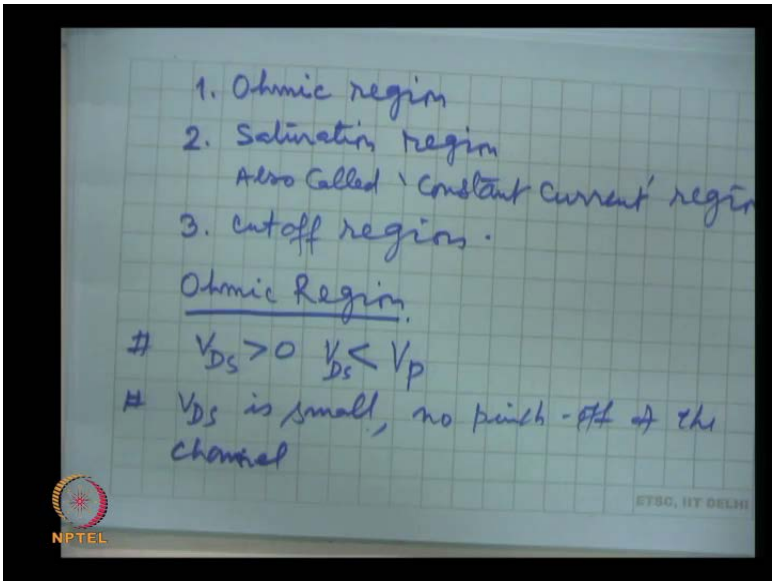

So, the characteristic has three regions, ohmic region, saturation region. Saturation region is also called actually constant current region, here current is almost constant so, also called constant current region. And third is CUT-OFF region, these are the three regions. This region where the current is starts saturating before that the region is called ohmic region. So, first we take ohmic region, ohmic region obviously, is of a V D S values greater than 0 and less than V D S, less than V P, the pinch of voltage. And here the we have, we are seeing from the plot, that current is varying from linearly with the change of V D S voltage.

So, in this region V D S is a small and it is below pinch. So, there is no pinch off of the channel and the current increases. Now, when we increase the gate source voltage, then

the resistance increases the changes slope. You see, slope is changing, this is voltage, this is current. So, the slope gives inverse of the slope gives the resistance.

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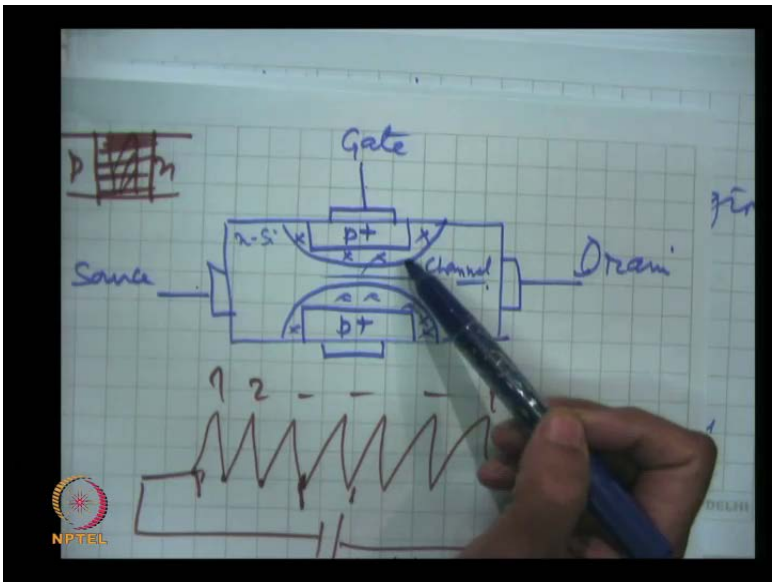

So, here the slope is changing and this you understand that when we increase the gate source voltage. This gate source voltage when we increase, this a channel conductance false, the resistance increases. For the reasons which we have discuss that, by increasing negative potential on the gate the depletion regions will a spread more, making the channel narrower.

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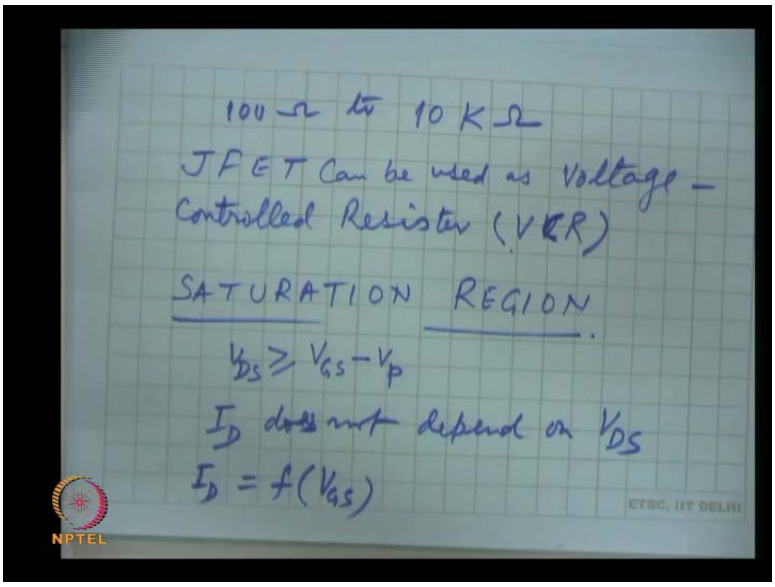

So, pinch off does not occur, but the resistance varies on the gate source voltage, the resistance in the ohmic region varies from 100 ohms to almost 10 kilo ohms. And obviously, this is a voltage controlled; it is a voltage controlled resistance, this voltage V G S, this is controlling the resistance. Here the slope is changing and which is a function of V G S and in this JFET, junction field effect transistor can be used as a voltage controlled (No Audio From: 08:20 to 08:29) resistor.

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V C R, voltage controlled resistance and so, this is about the ohmic region. And then we go for saturation region. In the saturation region; and this saturation regions is starts from this point and this point is actually V D S, the drain source voltage has to be higher than V G S minus the pinch off voltage so, this line. Here this is at, the point V D S is greater or equal to V G S minus V P is what I have written here, that saturation region is starts when V P S is equal or greater than this value. In this region, the drain current I D depends entirely on the gate source voltage. V D I drain current I D does not depend on drain source voltage V D S, but it is a function, drain current is a function of V G S gate source voltage.

Here, this current is varying as we are changing the gate source voltage, it is a constant with respect to change in V D S. These are almost horizontal lines, the drain current is not changing when we are varying the V D S in this constant current region and that is why, it is called a constant current region. Here, the dependence of a drain current on the gate source voltage has a non-linear relationship.

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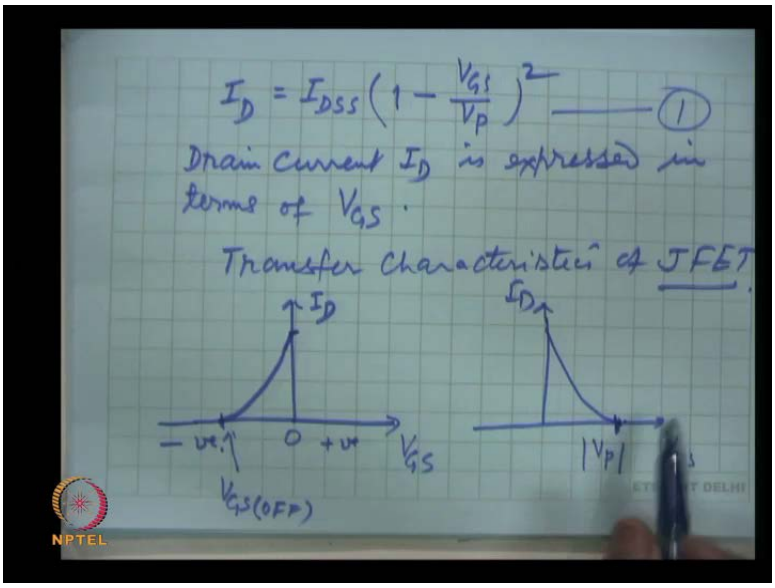

And this relationship cab be expressed by a square law and that is I D, the drain current is equal to I D S S into, 1 minus, V G S by V P, square this is an important equation. And this gives the relationship between drain current I D is expressed in terms of gate source voltage by this equation and from this we will use this equation very frequently. Now, very important thing when the device is to be used, when a junction field effect transistor is to be used as a amplifying device to amplifies signals. Then, JFET is operated in this region in the saturation region, it is operated.

And this relationship, non-linear relationship between I G and V G S gate source voltage dependence I D, this has a this relationship as express by this equation is parabolic in nature. So, we can get actually the transfer curves, transfer characteristics of JFET, why transfer? This is the drain current and this is the gate source, the true are, they not the part for example of the output current is I D, but this is a gate source voltage so, transfer. So, the curve is a parabolic, this is I D and this is V G S gate source voltage, 0 positive and here it is negative.

And this expression when V G S is 0, here the maximum current I D. Here, this is I D S S drain current, when gate is shorted with the source, that means, gate is at 0 potential, that is I D S S. And so, this is that current and as we are changing V G S more negative more negative, drain current is falling and here it is OFF. So, this is the parabolic plot and this value where this drain current drops to 0, this we call as V G S great source

voltage OFF, these are the drain characteristics for the n type JFET. The curve will be in the appose, because for a P type JFET, the gate source voltage is positive. So, it will be this way, this is drain current and this is V G S and this is this. And this is the magnitude equal to this which is also V P.

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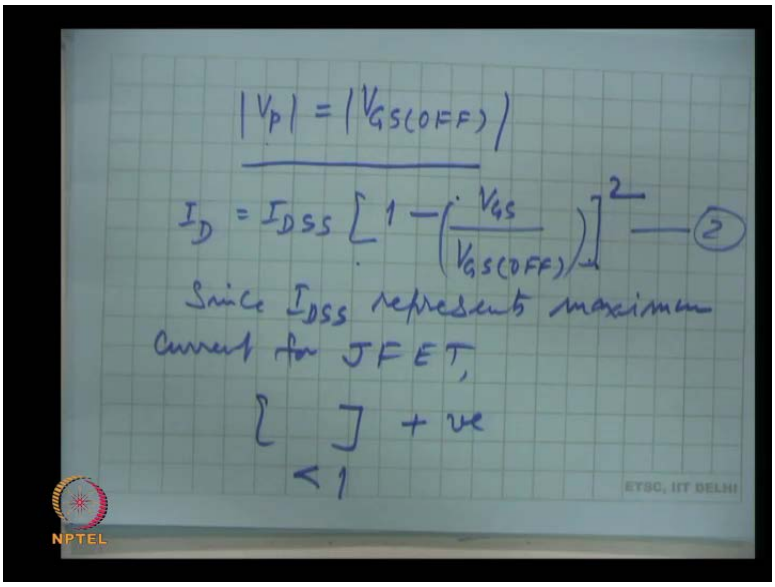

The pinch off voltage here. And so, from here, from this transfer curve, we get that the magnitude of V P is the same as V G S OFF, what is V G S OFF? V G S OFF is that voltage, gate source voltage which puts drain current to 0. And we can see from here, from this curve when drain current is 0, then V G S OFF is equal this relationship, we get write from this equation 1 by putting id equal to zero. Then from here we get V G S, the magnitude of a V G S OFF we will call, because that will put the drain current 0 and that come that will come out to be V P, that is why, I have written here V P or it is same as V G S OFF followed.

From this curve we are getting this plot and if we plot changes in I D as a function of changes in the gate source voltage, then this is parabolic behavior, which is expressed by this equation. We also see here that V G S OFF makes I D zero and that gives right from this equation V P equal to V G S OFF. So that, equation 1 can also we written as I D, I D S S, V G S, V G S OFF, we can write that equation let us call this equation 2. Now, one thing is certain that since, in this equation IDSS represent the highest current in the JFET. So, this quantities here in the bracket, in this bracket; this has to be positive and

less than 1. So, what have said is this that, since IDSS represents maximum current for JFET, the quantities in the bracket, this has to be positive and it has to be less than 1.

Now, why I am saying this, that we can just substitute V G S for any voltage at which if that gate source voltage at which we want to know, the drain current for the device. We put the value of this V G S OFF or V P, either we substitute this just numerical values of V G S and V P can; and if we know the current, drain current when gate is shorted with the source, that current is known. Then we can find out the amount of drain current with the any value of gate source voltage. And then so, this is all about the constant current region or saturation region, I repeat that the device is operated in this region when its purpose is to amplify the signal. We will see when we will develop the module for the JFET, we will use and we will use the analysis and derive an expression for the voltage gain.

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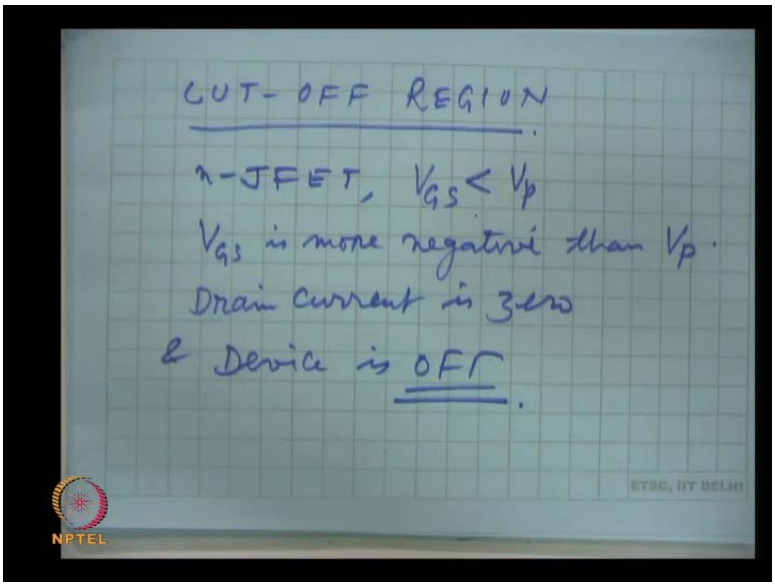

Now, the CUT-OFF region, (No Audio From: 21:01 to 21:14) CUT-OFF region is this region where the drain current is 0. So, for n-F E T; n-JFET, V G S is less than V P; that means, more negative, V G S is less than V P means, is more negative than V P and in this case the drain current is 0, in this region drain current is 0 and the device is OFF this region. In This region, this is; in this particular case minus 4 volts and V P was also 4 volts, this with voltages also 4 volts, V G S OFF is equal to V P this is what a we have said ever. And we say that for the CUT-OFF region V G S is to be lesser than V P; that

means, more negative than V P, a magnitude of V P has to be lesser than this so, that will put the device into OFF.

So, this is about the working and the I V characteristics of a junction field effect Transistor to make you familiar more about the device. Let us take one or two examples numerically problems on the device and they will clarify some of the doubts which you might we having.

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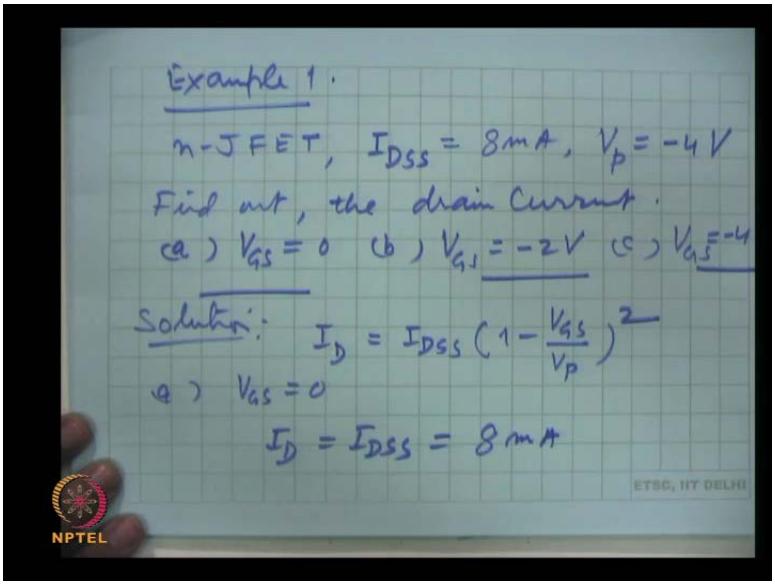

So, example 1, this is for a n junction field effect transistor, the parameters of the device are that I D S S. When the gate is shorted with the source that the maximum current in the n junction field effect transistor, this is 8 mill ampere and V P is minus 4 volts. Then find out the drain current, number one when V G S is 0, (b) when V G S is minus 2 volts and (c) when V G S is minus 4 volts, under these 3 values find out the value of drain current. This we can do simply, with the help of that expression for the drain current interms of the gate source voltage. So, I D is equal to I D S S, 1 minus, V G S by V P, square. Now, (a) V G S is 0 in that case I D comes out to be equal to I D S S when V G S is 0 this is a definition of the current I D S S and this is given as 8 mill ampere.

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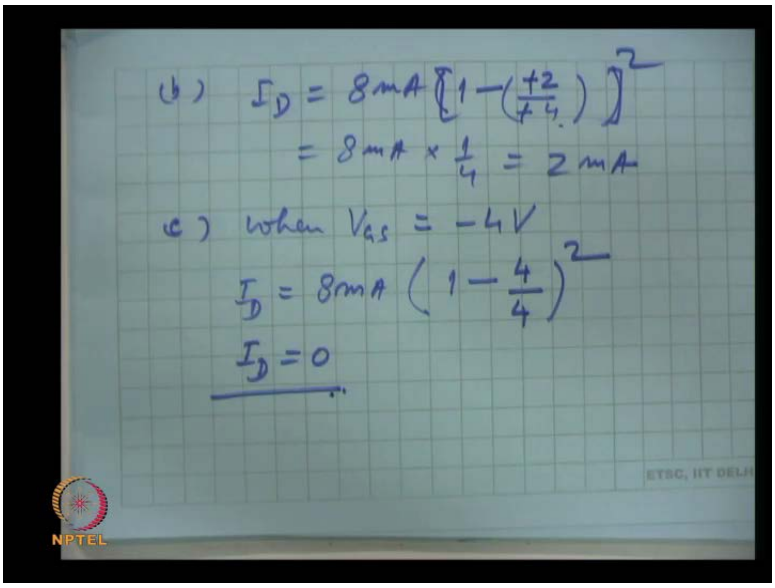

So, this is 8 millie ampere. Then for I D is 8 millie amperes that is the value of IDSS, I have substitute it in that expression and 1 minus; I said that either use both with proper sign for just substitute magnitudes this is one in the same thing. So, if I take with proper sign just this is minus 2 and this is minus 4, this whole square. So, you see here this is the same if I have just substituted the magnitudes. So, there is no confusion about sign, it is better just we talk in terms of magnitude, we have substituted the magnitude of VGS and V P also.

And so, they; this results in a current of 8 millie ampere into 1 by 4 which is 2 millie ampere. This is what, is expected when we increase the gate source voltage to minus 2 volts, the current will decrease from its value I D S S, I D S S was 8 millie ampere and this is a 2 millie ampere. And then C, when V G S is equal to minus 4 volts, then I D will be 8 millie amperes by 1 minus; I am just substituting the magnitude 4 and V P is also 4, this is square and that makes I D equal to 0, that is expected also, because of the plots if you remember. Here I D is 0 when V G S of which is minus 4 volts and V P is also 4 volts, then our substituted any way, the given values then id is 0. So, at three different gate source voltages, we have calculated the drain current with the help of this expression.

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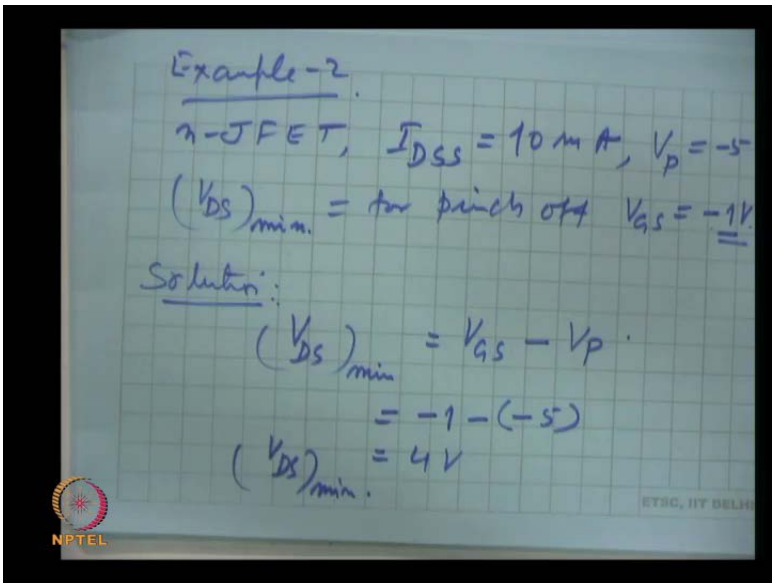

This is an example 2, again n-JFET which has I D S S as 10 millie amperes and V P, the pinch off voltage as minus 5 volts, then we have to find out VDS the minimum value of drain source voltage for pinch off when VGS is equal to minus 1 volt. I repeat n type junction field effect transistor which has the maximum current then IDSS as 10 millie ampere, the pinch off voltage of minus 5 volts. And we have to find out the minimum value of a V D S for pinch off at minus V P. So, now the solution you remember, we have written V D S minimum is equal to V G S minus V P. And so, this can be easily found out, this is given as minus 1 volt and this is given as minus 5 volts so, this is 4 volts the. In this, under these conditions, a drain source voltage of 4 volts will pinch off the channel and if we have to find out the drain current here at the pinch off.

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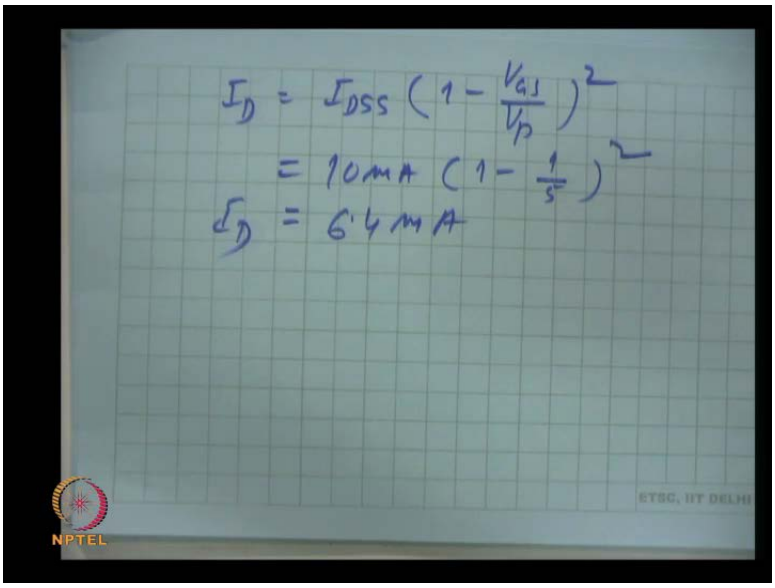

Then, the drain current again we can find out I D S S, 1 minus, V G S by V P, square. And this we can find out 10 millie amperes, 1 minus, 1 by 5, square when we solve it, it comes out to be 6.4 millie ampere, this way the problems can be handled. So, this is, about junction field effect transistor, we will return to junction field transistor again and when we talk of biasing and other things, let us talk of other devices.

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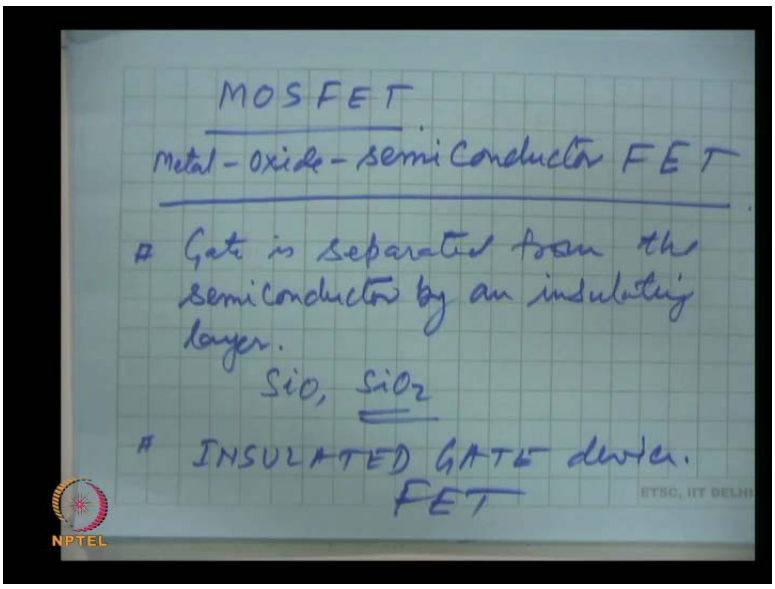

The next device in this module, which is very significant most important device today in Electronics is M O S F E T. In the beginning I have said that M O S F E T is tense for

Metal Oxide semi Conductor field effect transistor, this is M O S F E T. Sometimes in the interview, it is asked elaborate for what M O S is tense in M O S F E T. So, you should know Metal Oxide semi Conductor, as the name suggest. Here, the gate, this very important and a basic difference and that gives all the differences, the basic difference between a junction field effect transistor and a M O S F E T is that here, gate is separated by a insulating layer, Oxide layer.

If we are talking of Silicon, then a thin layer by thin I mean, for example, 50 Armstrong thin, then this is oxide layer separates the semi conductor with the gate electrodes. So, gate is separated from the semiconductor by an insulating layer. And as I said that insulating layer, when we are talking of a; normally, the Silicon is used. So, Silicon Oxide or Silicon dioxide is the layer which is used and that is one reason that why this M O S F E T is also sometimes call insulating; insulated gate M O S F E T, insulated gate F E T. We will see, that there are two types of construction and; that means, how through the field induced from the gate through the in this a insulating layer how the conductance of the channel is affected the whole working depends on that. And there are two kinds of a M O S F E T, one is Depletion M O S F E T.

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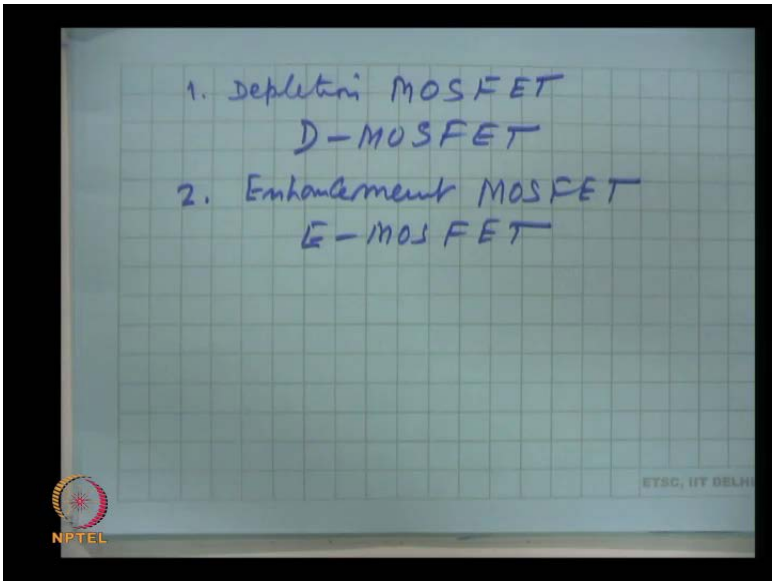

Depletion M O S F E T S, often written as D M O S F E T, D for depletion, depletion M O S F E T and second one Enhancement M O S F E T or simply E M O S F E T. There is a insulating layer which separates the gate from the semiconductor, I will give you the

construction. But there are two possibilities, one is the Depletion M O S F E T that is D M O S F E T and other is Enhancement M O S F E T that is E M O S F E T, both are very widely used. And first we take the depletion MOS FET.

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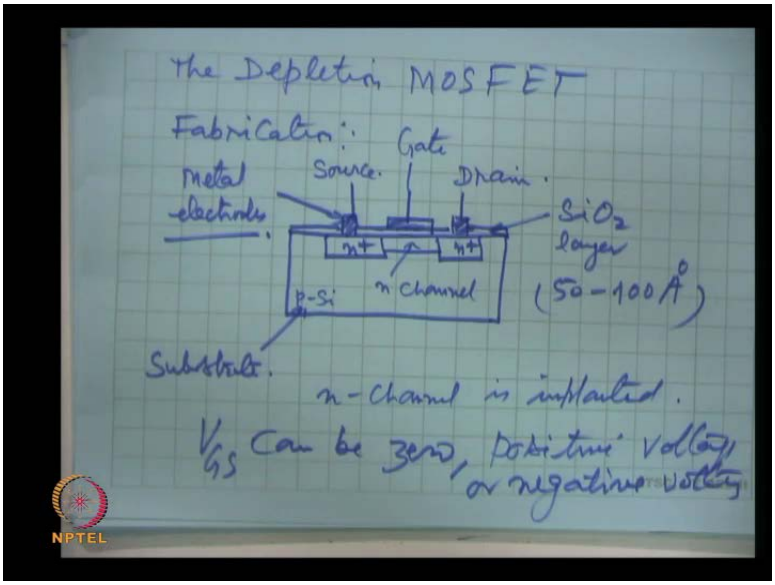

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Depletion M O S F E T, first the construction Fabrication; here is a small crystal of say P type Silicon, which is a substrate, on that we generate two heavily doped n regions, n plus, n plus. And then; let me first complete that drawing and then we will talk, this is the insulating layer S i O 2 layer, it is very thin say 15; 50 to 100 thick, very thin layer. How it is achieved that this silicon on which we are making the device, if fresh pure Oxygen, this is kept at a temperature and that flows it is all computer control. So, how thin Oxygen Oxide layer we need that this control and hence the oxide layer is obtained.

Then two windows are obtain by edging; that means, from the two regions here and here, the oxide layer is edged and metal electrode circuit and one electrode. These electrodes normally are of Aluminum and one electrode is put here and before all this is done a channel is implanted. Here this is n channel, which is implanted and these are the three electrodes. This is source, this is gate and this is drain, these are let we do like this, these are metal electrodes, this is a depletion M O S F E T. I repeat all what I have done that, P type silicon is taken as substrate over which two regions are created by heavily n type dope; doping and in between this n channel is implanted.

These are sophisticated techniques of creating n or p type region said a specified places very precisely, because this dimension I will draw a still bigger to make my points clear. But actually, these dimensions is a fraction of a millie meter, the total dimension is a very small 100 of a milli meter or a still a smaller. So, the channel is implanted and Oxide layer is put so that, the gate and the semi conductor they are separated by this Oxide layer. This, I will to put my points clear I will make a bigger figure, but let me point out one big difference with JFET.

In JFET in the n type, the gate voltage was negative necessarily through reverse bias the junction. Here below the gate, there is no P n junction. Therefore, the gate source voltage V G S can be it is very significant point; can be 0 or positive voltage or negative voltage, all possibility. We can give gate positive potential with respect to source or we can keep it at a negative potential. So, positive, negative or 0 potential, all are possible in this device, it is a big difference. Why we do not operate a field effect; a junction field effect transistor with A?

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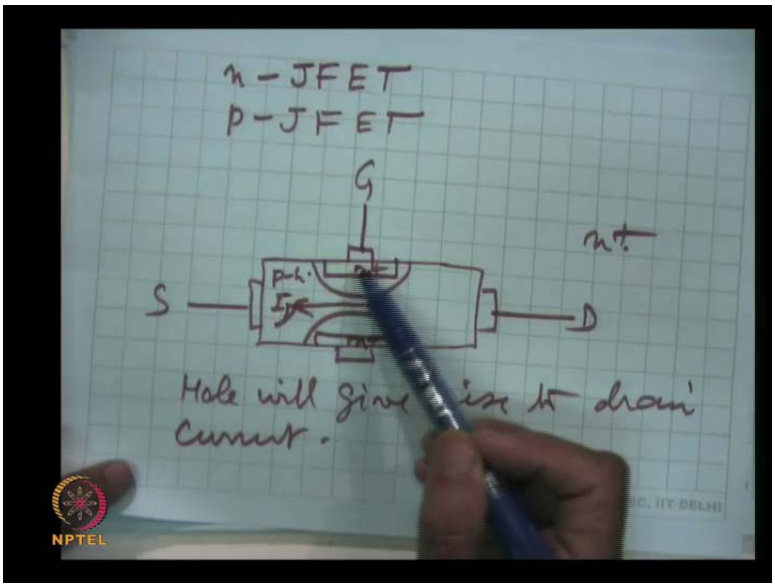

This was a F E T, this is of course P type, but it is all right. So, here now to forward bias it, we will have to give a positive potential, positive potential will forward bias the P n junction lot of current will flow so, that will not be operated. That is for n type JFET a figure must be ya.

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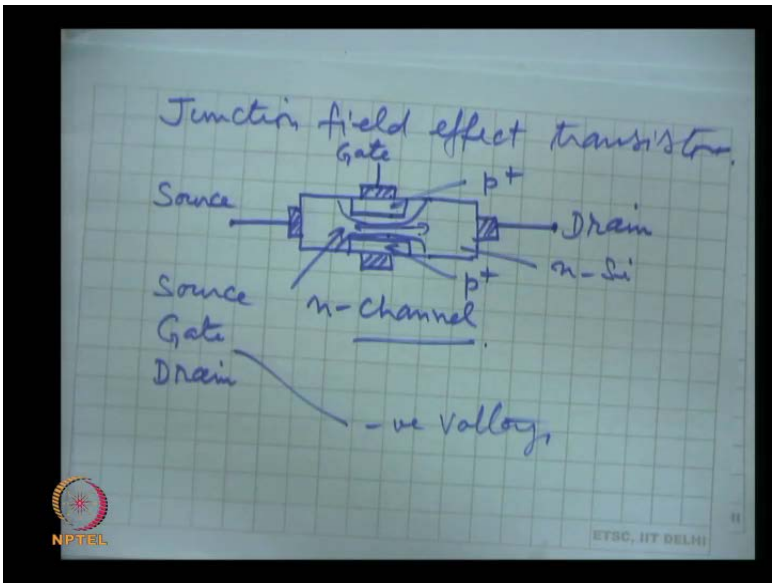

This is gate, this was P type material, this is n and we have said that gate in the n type JFET is always operated with the negative voltage. And we draw the characteristics where the gate source voltage is negative, more negative, more negative and so on. Because making it positive will make the junction forward bias, lot of currents will flow and different phenomena will occur and will create problems. In this case, in the M O S F E T, there is no direct; there is no P n junction. Hence it permits the voltage at the gate with respect to source either positive or negative or 0.

Now, let me redraw this figure and show you, that how the charges induced through this a dielectric layer will change the conductance of the channel and hence will control the current. I will make a bigger figure and.

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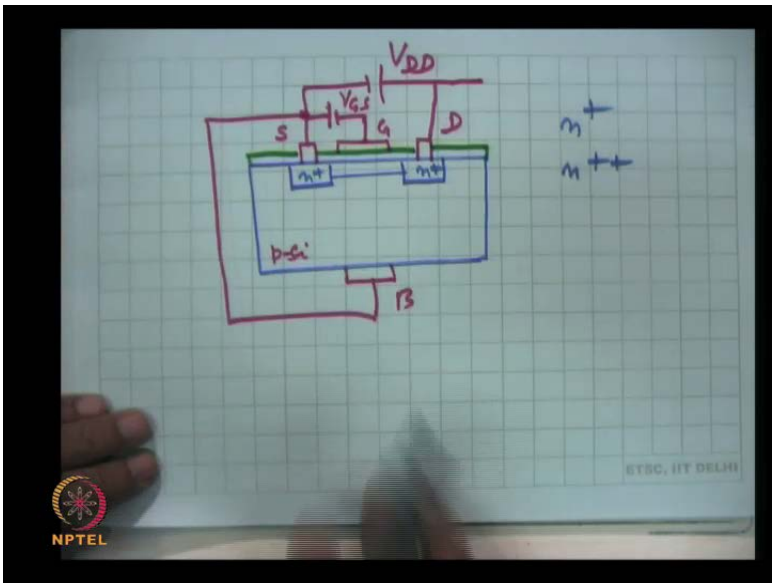

This is oxide and here is the gate electrode and this is the semiconductor, which is P Silicon and here is the body b, which is shorted to internally shorted to the source. And we apply a positive voltage, here between drain, this is drain, this is source and this is gate. And we apply to the gate for example, we start with a negative voltage this is V D D and this is V G S. Now, let us see, how the channel is n type, the channel is n type, this is n region, this is n region heavily doped. And heavily doped is represented by plus sign is still more heavily and 2 plus signs, this is heavier then this doped. So, how the field will induce and the depletion region it will create, for that let me just draw this portion much larger. This is the (No Audio From: 46:58 to 47:04) this is that S i O 2 layer and (No Audio From: 47:06 to 47:17) these are the Electrodes.

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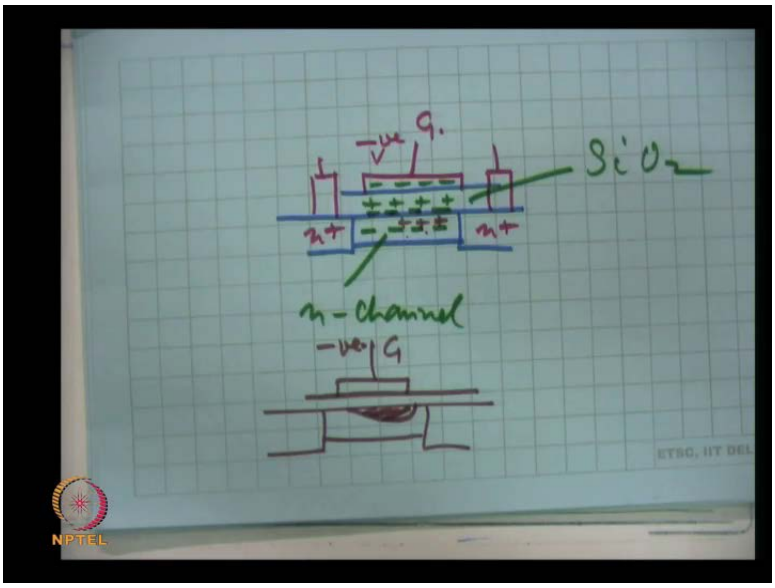

This is a heavily doped n type, this is source, this is drain and this is gate. Now, when we apply a negative voltage to the gate, then these look at these charges, this is negative charge and this is n type channel, n channel. And so, here are the electrons, this is the S i O 2 layer, a dielectric this field at the gate very important, the field at the gate will polarize. This S i O 2 will induce positive and negative chargers, they are bound charges in the insulating. It is S i O 2 is insulator, they are a low free chargers. So, that field at the gate will induced the opposite chargers.

This is you must have a studied, how the capacitance of a capacitor is increased by introducing a dielectric. Dielectric get popularized and that, they are in the case of a capcatior some charges of the plate so the capacitance increases. In this case, this will induced some positive charges, here this negative just at the surface, just above the channel this positive charges will be induced. And these induced for the positive charges will recombine with some of the electrons. So, therefore, in this region, this is the channel, now, this is the depletion region which will occur. And this is of course, the Oxide and this is the gate negatively charged, I think I have made clear what will happen.

Look here, that this is the geometry we are talking. The gate I am taking negative with respect to source and this negative field at the gate through the dielectric will induced some positive charges in the channel region. Channel was n type; that means, negative

charges, the electrons were there. Now, this induced positive charges, will recombine with some of the electrons and a depletion region will be formed. And hence this depletion region, depletion region is always a region divide of mobile charges; that means, high resistivity region. So, by this depletion region, depletion region will increase the resistance, will decrease the conductance of the channel.

If now, we keep this constant, there will be a current in the in that; these will be the characteristics here, this is V D S volts, this is I D when there is; if there is this.

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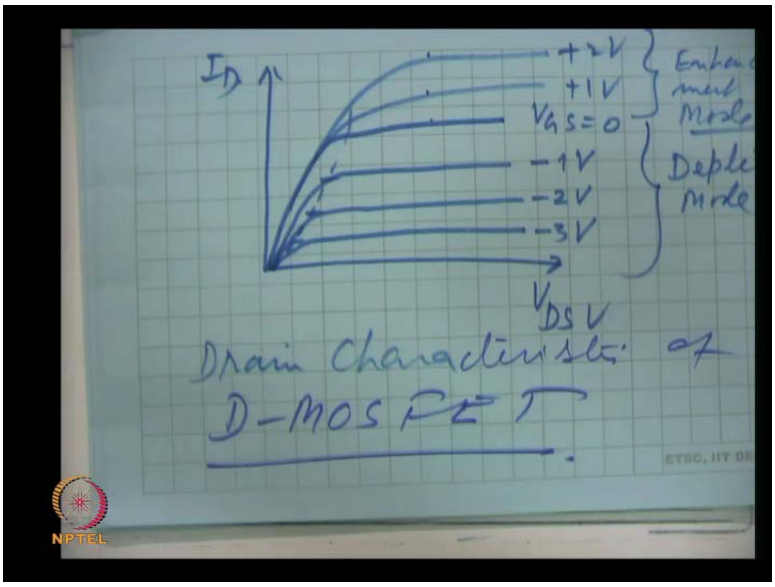

Voltage gate source, voltage is kept to 0. Then this is the channel when we change this voltage V D D, that is, V D S we change between source and drain, the current will flow because of these electrons, this is n channel, current will flow. So, this current will be this and now, this is V G S equal to 0. Now, we have given a negative voltage that reduces the conductance so, for the same voltage same drain source voltage the current will fall and this way, we will get these characteristics.

(No Audio From: 52:24 to 52:39)

This is at V G S of minus 1 volt, minus 2 volt, minus 3 volt and so on. And a voltage may come where this channel may be completely the depletion region has completely taken over and there is no continuity there is no conductance between drain and source. So, here device is OFF, this is the depletion mode for the device. Now, if I give a

positive voltage, if you have followed this, that negative voltage induces a depletion region. Because positive charges will be induced in the channel and that will take some of the negative charges of the channel, mobile charges of the channel and hence the conductance will fall.

If we give a positive voltage to the gate, which is possible and that will enhance the conductivity. That will induce more negative charges in the channel and hence the conductance will increase. So, the currents will change and here this is plus 1 volt V G S, plus 1 volt, Plus 2 volts and so on. And this is known as depletion mode is now working in a enhancement mode. Remember, enhancement mode is different than Enhance E type M O S F E T. A Depletion M O S F E T can be operated in the 2 modes, depletion mode or enhancement mode simply by changing the nature of polarity at the gate.

If gate is negative with respect to source and keep on increasing that negativity current will fall, because depletion region will penetrate more and more in that channel region. And by giving a positive voltage, more charges negative charges will be induced by the field in the channel region and the conductance will increase. So, for the same voltage more and more current will appear here. This is higher than this and this is higher than this. So, this is these are the characteristics of a Depletion M O S F E T, drain Characteristics of D M O S F E T. We will continue our discussion on MOS FETS.