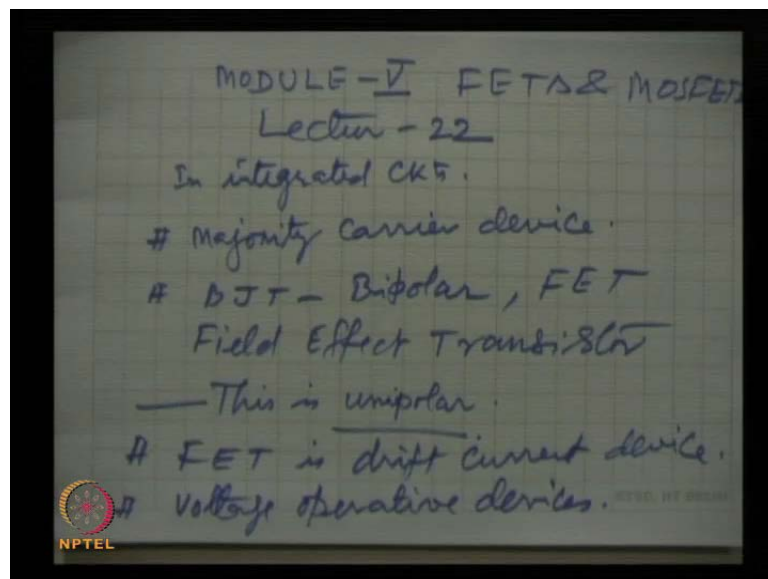


Electronics
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Module No # 05
FETS and MOSFETS
Lecture No. # 01
FETS and MOSFETS

We now start the next module, module five, which is on field effect transistors, field effect transistor. After BJT bipolar transistor, it is the 2nd generation transistor. BJT is the bipolar transistors, were developed first and FETs, as popularly they are called, they came later. FETs are very widely used, particularly in integrated circuits.

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Today, if we look for the total volume of electronic circuits, then Ith, I mean, rough estimate is that more than 75 percent circuits, they are of FETs. FETs are very different as compared to the bipolar transistor. Some differences I can specify right now, that field FET transistor, it is a majority device, majority carrier device, majority carrier device and you know, that bipolar transistor, the main function on which the total operation of the transistor depends, that is, when the carriers are injected from the emitter to the base.

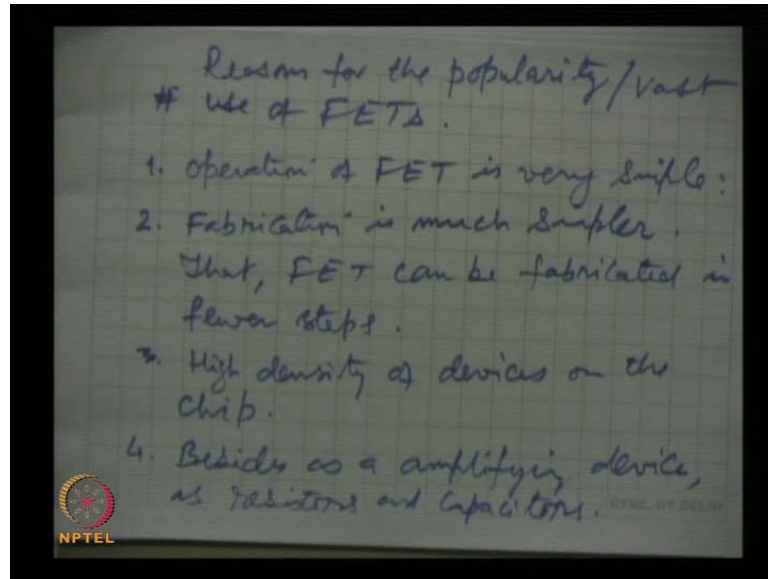
Now, in the base the charges, which are injected from the emitter they are in minority. For example, if we talk of NPN transistor, then emitter is N type, N basis, P type. So, in the p type base, electrons are injected from the carrier. So, electrons are in minority in the basic region and that is the reason, that bipolar transistor is called a minority device, minority carrier device, and in contrast FET is a majority carrier device. This is one difference.

Then, the whole operation, I do not want to go into details, we have finished that earlier, that the BJT is a bipolar device. BJT is bipolar, that means, for the operation of a bipolar transistor, the transistor, we need holes and electrons both. For example, in the base region the recombination of charges takes place, which gives rise to the base current, which is very essential for the operation of the transistor. So, that is, that is the reason it is called bipolar device. We will see, that FET, FET, field effect transistor, FET, which is field effect transistor, this is unipolar. Unipolar, meaning, either we need electrons or holes, not both, in the same device. So, this is a unipolar device.

In the BJT we always talked about currents: the emitter current, the base current, the collector current and the currents flow within the device because of largely, because of diffusion. Diffusion, as you know, that diffusion of charges occurs because there exist a concentration gradient and that gives rise to diffusion. Obviously, diffusion is a slower process. We will see in the, in this field effect transistor, this is a drift of charges. The operation depends not on diffusion, but, but drift of charges under applied field. So, it is a drift device, FET is drift device, drift current device.

And we will see here, in the BJT everything is controlled by the current and every time, even in the analysis we saw, that we have to calculate the currents here, the voltage, particularly as, as, as we go through the device, the voltage at the gate will control the current flowing in the circuit. So, it is a field effect, field device, it is not current device, it is a field device, FETs are field devices or voltage operative in contrast to the BJT, which is a current operative. Now, what are the reasons?

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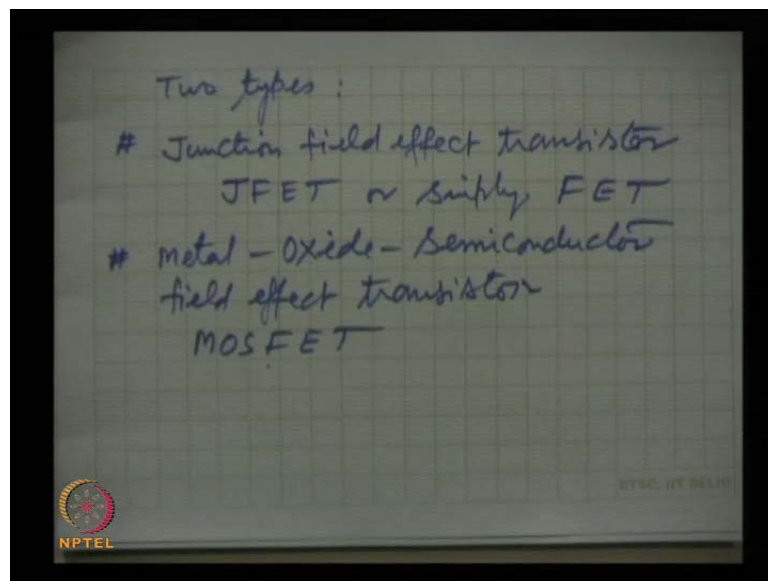
Let us talk of some features that make FETs very popular today, these are, I can, head, give headlines, reasons for the popularity and by popularity here I mean, vast use of FETs. One reason is that the operation, as we will see, the operation is very simple, operation of FET is very simple. When I say it is simple, that means, we are comparing it with BJT; as compared to BJT, the operation of FETs is much simpler.

Second reason is design. The fabrication, fabrication is much simpler, it can be fabricated in fewer steps, that is, FET can be fabricated in fewer steps; in fewer steps. And the next point, which is very, all these points are very important from integrated, the technology point of view, but this next point is very significant, that a FET device takes one-fifth or lesser area for one device on the chip. I repeat, the area required for a single FET on the chip is at least, one-fifth of BJT. As a result, very high density, high density of devices on the chip, high density of devices, very large number because the area, which a MOSFET device, this FET device takes is very small, at least one-fifth and hence, the density is very large. You will be surprised, that now in one square by one square chip, there can be a million transistors that mean FETs.

And another kind of FET, which we will study, MOSFETs and they can be fabricated, all properly connected. Very surprising, our imaginations fail to imagine the size when on a chip a million FETs are there, what will be the size of each FET, and all working, well connected?

The next point is, which is also very significant, that FETs, field effect transistors can be used besides as an amplifying device, besides as an amplifying device, FETs can be connected as passive components like resistors and capacitors; resistors and capacitors. So, often, the circuits will contain only FETs where some FETs will be simply, they will be functioning in the circuit as resistors while others will be active devices and some as capacitors.

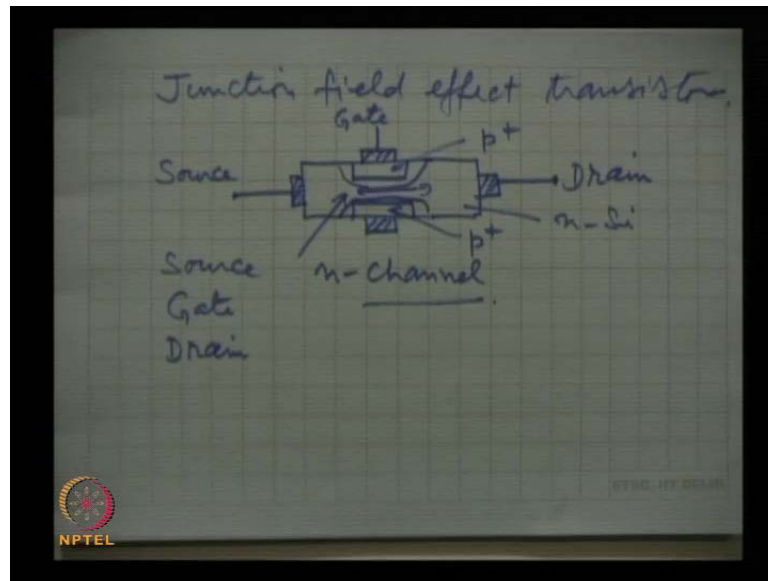
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Broadly speaking, FETs are of two types, two types; one is junction field effect transistor, junction field effect transistor, which is abbreviated as JFET, junction field effect transistor, JFET or simply FET, or simply FET. When we say FET, normally we mean junction field effect transistor.

Now, then, we have the another kind, which is metal-oxide-semiconductor field effect transistor, metal-oxide-semiconductor field effect transistor, field effect transistor, that is written as normally, and in fact, always we write it as MOSFET, MOSFET, metal-oxide-semiconductor field effect transistor, MOSFET. These two types are very widely used and in integrated circuits, mostly we will see these will be the MOSFETs. First, we will study the junction field effect transistor, having introduced I am sure you have followed the basic difference is, as compared to BJT and the reasons for popularity, why FETs are so widely used in circuits.

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Now, we go for junction field effect transistor, junction field effect transistor. The construction is like this. Here, let me at the beginning remind you, that since we are talking of a different device, now the terminology used will be quite different and it is better, that you should get familiarity with the terminology used in FETs.

So, here, this is a substrate, a n-type substrate, this is n substrate, normally n-silicon, n-silicon. About dimensions we will talk about later, let us just take, it is a chip of n-silicon on which two regions of heavily doped p-type, this is p plus and this is also p plus, they are developed, they are fabricated, they are grown heavily doped p regions on the two sides of a small crystal of n-type silicon. And one electrode is deposited here, the other electrode is deposited here and then, there are these two electrodes, these are all like aluminum and these both are internally shorted.

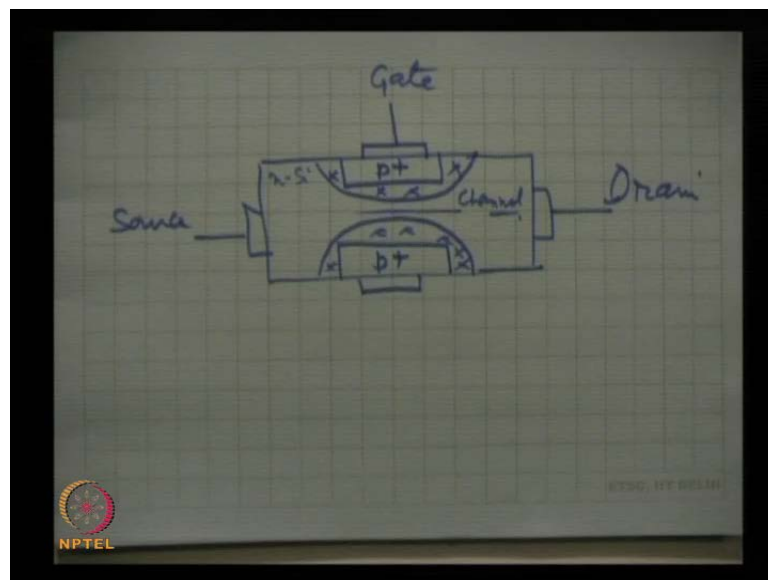
The two p-type regions, which have been form on the two sides of a small crystal of n-type silicon, they are shorted internally and now what these are called? This is called source, this electrode is called source, this is called drain and this one is called gate, there we have emitter base and collectors in FETs.

And of course, for in the MOSFETs, the same terminology is, we have source gate and drain. Just for the sake of comparison only, that source is almost like the emitter, gate is like base and drain is like collector. Now, this is called the channel, in between the two gates is called channel. This is n-type channel, n-channel. What will happen when this is

n-type silicon, n-substrate over which we have grown two p, heavily doped p regions for the reasons, which we have discussed in the p-n junction? Wherever n and p type semiconductors meet, that means, if there is a, there is a structural continuity, then the natural processes, which will you start from diffusion and followed by drift, that means, a depletion region will be formed.

I repeat, this is the substrate n-type and this is p-type region, this is p-type region and this is heavily doped. So, p-n junction kind of thing will occur, of course, but more important than that is depletion region will be deposited here; here, this is a depletion region and here also, there will be a depletion region. I draw a more neat and clean, a bigger size figure and then I explain what will happen when we apply voltages.

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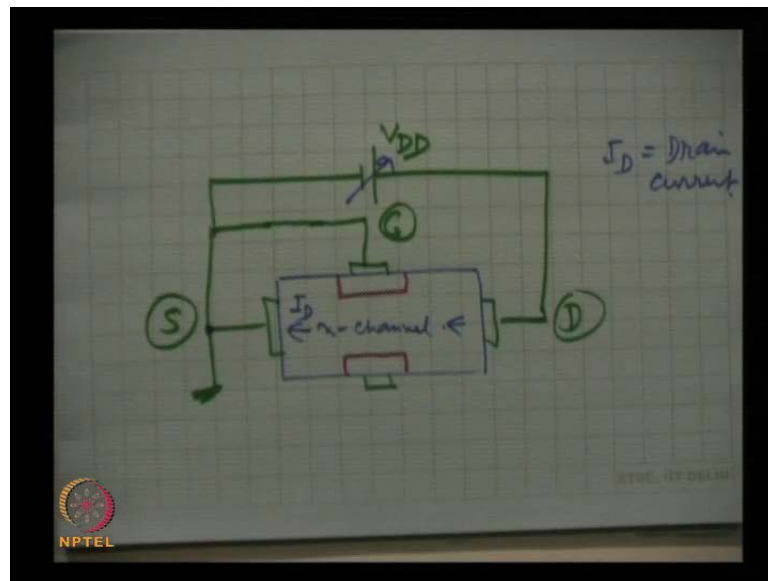


This is the device in equilibrium here. This is source, this is, **gate**, drain, these are the p type regions, this is p plus, this is p plus and here is the depletion, this is depletion. Similarly, a depletion region will be found here, this is depletion and here, we put an electrode, here we put another electrode, these two are internally shorted, that means, they are connected together. When we apply a voltage, the voltage will apply simultaneously on both the gates and this is gate, this is I think very clear. Now, this is the p type region and this is the depletion region and here, this is n-type, n-silicon substrate and this is the channel, this is channel, this is channel, channel, this is about the construction of a junction field effect transistor.

Now, to understand its operation I will first consider the case, that gate is kept at a ground potential, it is at a zero-potential, it is grounded. In fact, source is also grounded and between source and drain we apply a voltage keeping drain side as positive. Let us see what will happen.

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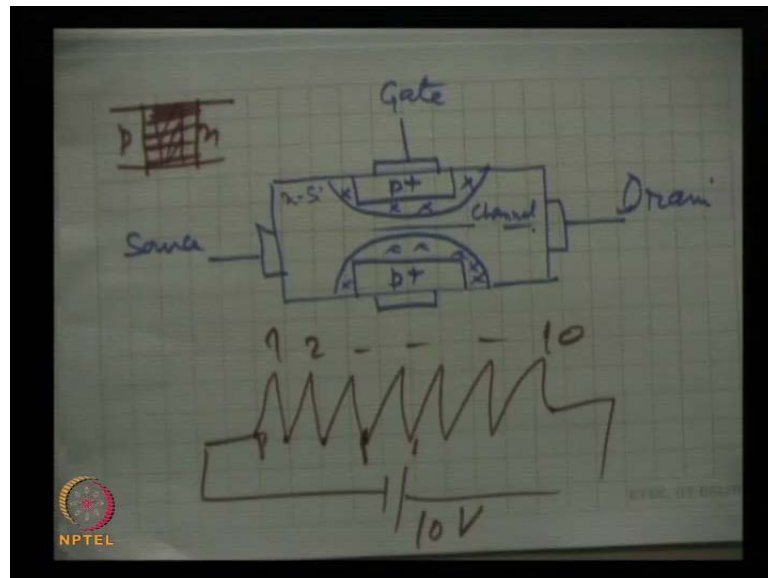
This is a battery V_{DD} , this is the source, which is written as S, this is drain and this is gate, gate is at a, gate is at zero-potential, at ground potential, it is grounded and we have applied the positive voltage to drain with respect to source. Now, what will happen?

This is the channel. When we apply a voltage between the two ends of a semiconductor, then charge carriers will flow and a current will start flowing here because this channel is n-type, n-channel and this is the positive electrode drain. So, electrons will flow into this, they will come out and they will enter from here and drain current. Current flows in this direction, here in this direction, the drain current written as I_D , I_D is the drain current, drain current, which will flow. So, as we start this, let us keep this varying, as we start this, a source drain voltage from 0, then as well as we move further, the current will start flowing and larger the voltage, larger will be the current.

Now, what happens to the depletion region, that is very interesting and I will show, that this current will start rising, but will not continue to rise indefinitely. There is another

effect, which comes into play and that when you stop that rise and after a certain value the current gets constant. What happens? The depletion region, this was the depletion region, depletion region will be widened in (()) base.

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You remember, we said, that depletion width of a p-n junction increases on reverse bias. Remember, that in the p-n junction, if this is p-type, this is n-type and this is the depletion region, if we increase the reverse bias, that means, p region is given a negative potential and n given a positive potential, then this is widened. This is, this is the new depletion width. Now, here depletion width can be changed in two ways, both ways of course. We are reverse biasing the p-n junction, so there is a widening of the depletion region and both are, there are two gates, so widening will be from both sides. Now, what is, what are the two ways?

One is, if we give, this is p-type gate, if we give a negative potential to the p-type gate, then depletion region will increase, it will be widened, number one way. Another way is, you see, that here this is a semiconductor having a finite resistance and that resistance is dropped all over, between these two points resistance is different, these two points it is different and so on. Accordingly, the field is spread all over; it is maximum positive here and least positive here, like here.

For example, if I take a simpler, to make my point very clear this is very essential what I am going to say, that how the shape of the depletion region changes is, it is an oblique, it

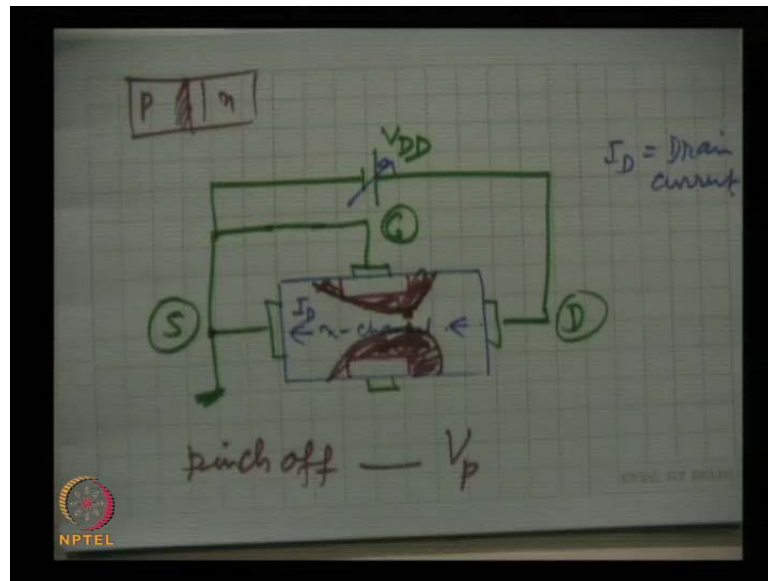
is a different shape and what happens, that for example, suppose these are, there is a resistance wire and these are 10 loops and we apply here a voltage of 10 volts. If we measure, now these are, roughly are not done all the 10, but let us see these are 10 in number, 1, 2 and 10, if we measure the voltage between these two points it will be 10 volts; if we measure between this point and this point, it will be 1 volt, 2 volts, 3 volts, between this and this it will be 3 volts, between this and this 4 volts and so on it will go on increasing.

In the same way, in the same way, here, the voltage when we have applied V_{DD} , which will be largest here and least here, between this point and the very close to this surface, the potential will be almost 0, between source and middle it will be roughly half of the voltage, which we have applied. If we have applied 10 volts, between center and here it will be 5 volts, between the source and this end it will be 10 volts. Now, we can reverse bias the junction either by giving a negative potential to the p-type material or very important, a positive potential to the n-type region.

I repeat, we can reverse bias the p-n junction by providing, suppose one is grounded, then we provide a p-type negative, more negative, more negative with respect to that grounded terminal, maybe, n-type. Then, broadening of the depletion region will occur and, or if we keep this at zero-potential by grounding the gate, if we increase this potential, which is increasing this way, decreasing this way, so in this region in the drain, now very important, in the drained region the depletion width will be larger than in this region for the simple logic, that in this region closer to the drain, the p-n junction, p-n junction is more reverse biased as compared to this region.

Now, another important region, in fact, that I said, these two regions, they are heavily doped, heavily doped p regions.

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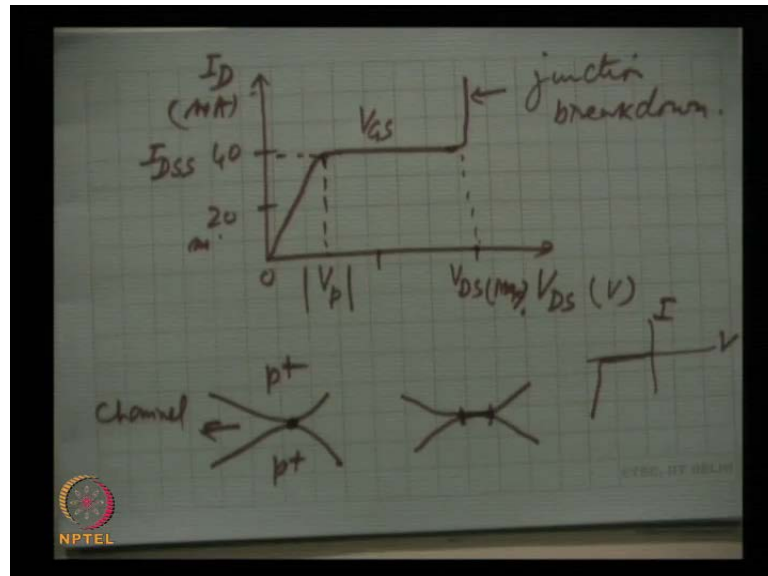
I am sure we will recall, it was said, that if one region out of these two p and n regions, this is p region, this is n region, if p region is heavily doped, then the broadening will occur, then the broadening will be spread much more in the less doped region and so, this channel region is less doped. Hence, the most of the broadening will occur into the channel region. If you have followed what I have said, then there is no difficulty in understanding, that earlier this was depletion region was symmetric. Once we apply a voltage between source and drain keeping the gate at zero-potential, then increasing this voltage will give this shape, this shape of the depletion region, this is the depletion region.

Now, when we keep on increasing this voltage, these two points, there the depletion regions will come closer and closer and the shape will be maintained and obviously, a situation will come where one point, at one point the two will meet, that voltage will be called pinch off and it is return as V_p , pinch off voltage. What is pinch off voltage? That minimum voltage between drain and source at which, which will make the two depletion regions, the lower gate electrode and the upper gate electrode regions touch at one point, that will be called pinch off.

And now, this is not difficult to follow that because of, this is spread of the depletion region, the channel conductance, the conductivity of the channel is changing, it is falling depletion region. I am sure you have not forgotten, that depletion region is a high

resistivity region, high resistivity region and so, the channel width falls, channel width is falling and the resistance will increase. So, the current levels of it become constant.

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Now, what I have said, if I plot the drain current as a function of drain source voltage, that is, this plot, this is drain source voltage in volts and this is drain current, this is 0 volts and this 5, 10, 5 and here, this may be 20 milli-amperes and 40 milli-amperes and so on, 20 milli-amperes and this is in milli-amperes, 20, 40, 60 and so on, depends on the device. This can be 100, 200, 300 milli-amperes and the voltages can be 30, 60 and so on. So, now, from 0, I said this voltage we are changing from 0, so the drain current will increase and it will keep on increasing. With this increase what is happening, that this is a depletion region, is spreading more and more towards the channel and the moment the channel, they are the two channels, I mean, the two depletion regions touch each other, pinch off occurs and by then, the extent of, of conductance, that unifies the effect of the raising voltage. So, at that the current is levelled off, it does not increase further and this voltage, this is V_p , the magnitude of the pinch off voltage, by here the pinch off has occurred.

Now, you may ask, that once the pinch off has occurred, why the current is constant? By further increasing this voltage why the current is not increasing? Very valid question and let us try to understand this again.

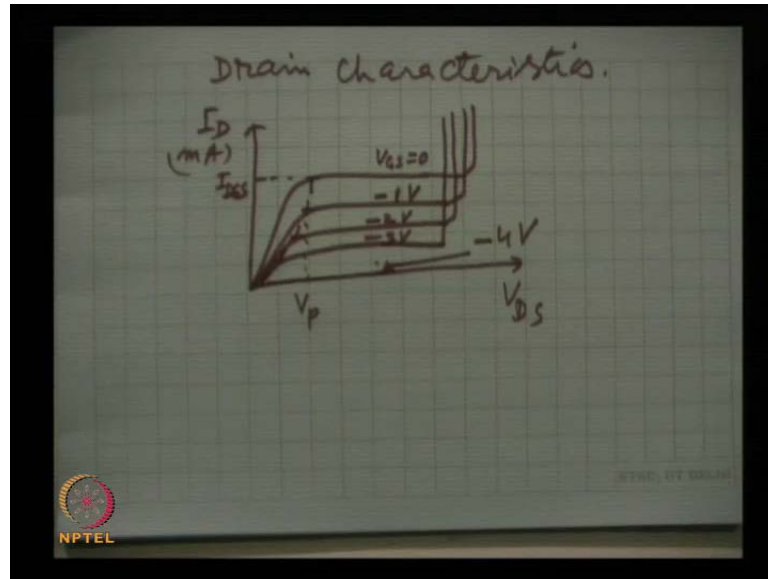
Once at this point the pinch off has occurred, that means, this is the channel through which charge carriers are flowing to form the current. Now, this is the depletion region and at the pinch off here, at only at very small region at one point, the two depletion regions are contacting. As we increase this voltage, then this contact region increases, that means, that this voltage, the channel is like this, it is here, it was touching at one point and here it is touching all through this region and hence, it stops the rise of current.

The, the effect of increased voltage to increase the current is levelled off by this rise in the resistance of the channel. The conductance falls, as up to here, it, gradually the current is increasing, the channel is not pinched off, but here pinch off starts at one point only and then, when we further increase, than the more and more region length-wise, the channel comes in touch, is touching with one another. The two depletion regions touch along the line and this width of the line of touch increases with this voltage V_{DS} . So, this is this. Now, if we further increase V_{DS} , then suddenly, there will be erasing in the drain current. This is because of the junction break down, this is junction break down.

We talked about a process in the case of a p-n junction, that junction break down occurs when the reverse bias voltage increases during the certain point. You remember, that I-V characteristics of a p-n diode, this is I, this is V, this is very small current and suddenly, the current increases, this is the break down region. Same thing happens here and this is called, this voltage is called $V_{DS\ max}$; max means maximum.

We are not supposed even to operate in this limit. The voltage has to be less than $V_{DS\ maximum}$ value, which is prescribed by the manufacturer on the, in the data sheet. Now, this current, maximum current, this is known as I_{DSS} , when this is the maximum current in a JFET. Let us, this was, if I am sure you have followed this characteristic and this is when V_{GS} , that means, gate source, gate source voltage is 0 because we grounded the gate. What we have drawn, these are known as drain characteristics of a field effect transistor; drain characteristics. We get plots when we change the gate voltage from zero to more and more negative.

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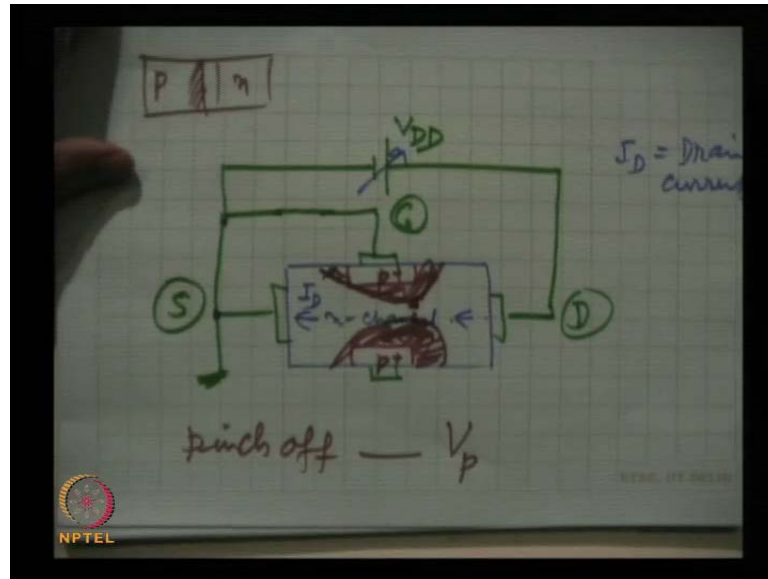


That means, the total, the, what we call the drain characteristics, drain characteristics can be obtained and these are, we will not, anyway it is alright, this is this.

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This is drain current in milli-ampere, this is V_{DS} and this is I_{DSS} , the maximum current and these are, this is at V_{GS} equal to 0, this is minus 1 volt, minus 2 volt, minus 3 volt and so on. And then, finally, this will be at minus 4 volts, for I have taken numerical values. This may be true for a particular JFET, for all JFETs we will get a similar plot, only difference maybe, that these currents may be different, these voltages may be different and this is the pinch of voltage, these are the complete drain characteristics for... Now, why, when we made the gate more negative, why the current falls?

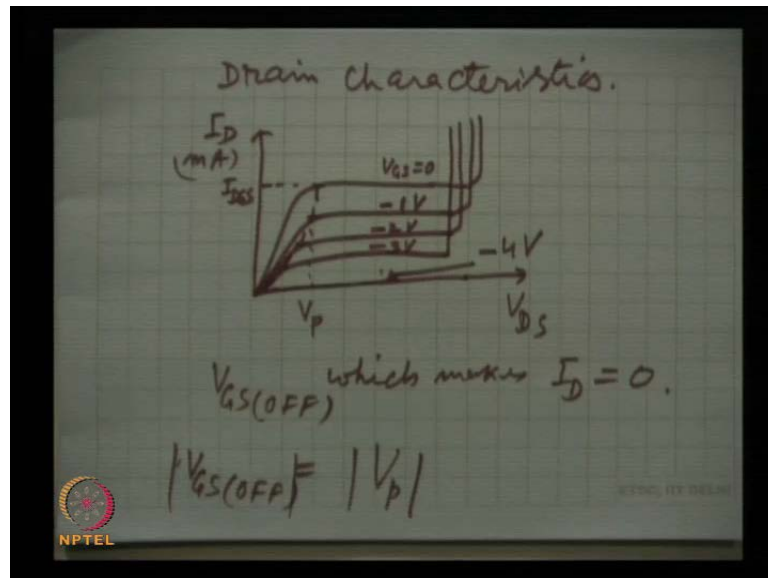
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If the discussion, which we have made earlier, if you have followed that keeping this drain source voltage fixed, if we change the gate voltage make it more negative. Making gate more negative means what? We have reverse biasing this p-region and this p-region depletion will increase and it will increase towards the channel.

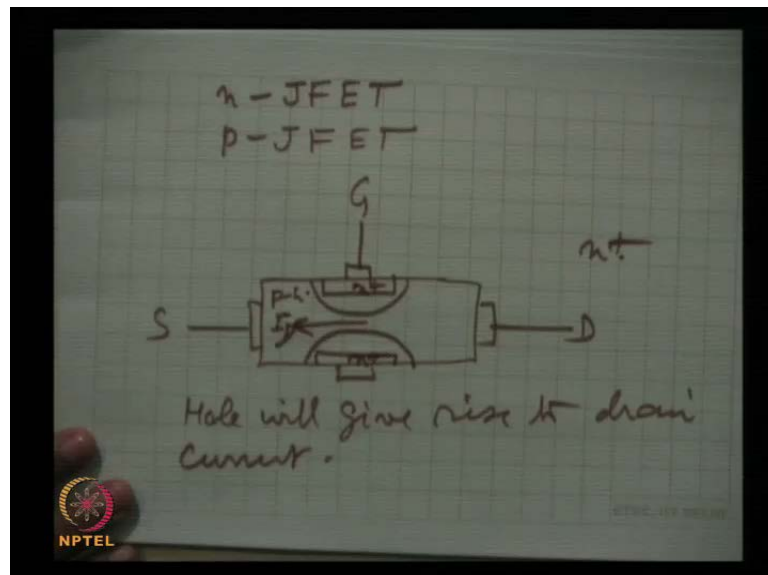
So, instead of 0 volts when we make it minus 1 volt, then keeping this constant, the conductance of the channel will fall because in the channel, now more portion of the depletion region exist and hence, on increasing the gate voltage, the drain current will keep on, fall, falling. It falls, it decreases and a situation comes when the drain current will be 0.

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And this is known as $V_{GS\ off}$, when, which makes, that gate source voltage, which makes drain current equal to 0 and obviously, we will see this, that $V_{GS\ off}$ is equal to, magnitude-wise is equal to the magnitude of V_p . Now, the device, which we have been talking so far, this is the channel, was n-type.

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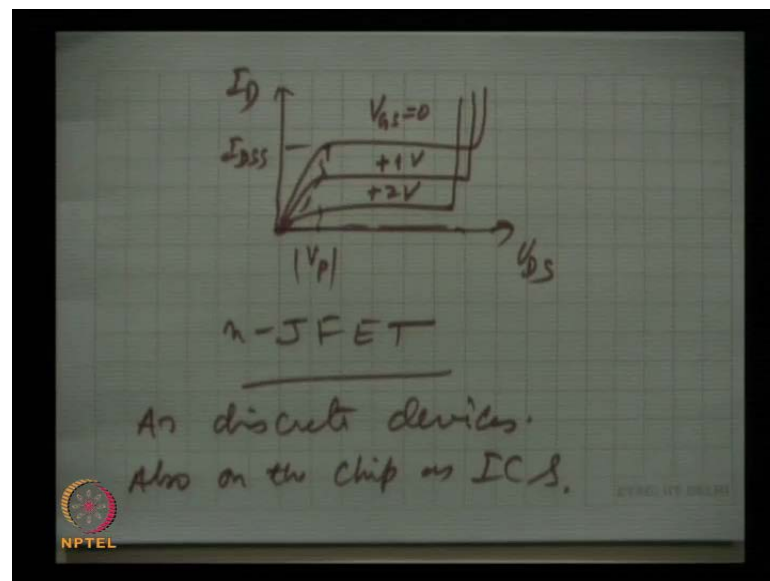


We started with the n-silicon and the channel was n-type and this is actually a n-type junction field effect transistor, n-JFET. We can have a p-type junction field effect transistor as well, for that we will have to start with a p-substrate, a p-substrate, p-silicon

and n-type regions. These are the n-type heavily doped, n-type gate region, we will apply the electrodes and these two gates, they will be internally shorted to each other, so that externally only one lead is available. And this is gate, this is source and this is a drain and same thing, depletion regions will be here. This is now p and this is n region, this is n region, heavily doped n regions. Here, same thing, expect now when we apply a positive voltage at the drain with respect to source, then holes will, will take part in the current process.

So, holes will give rise to drain current. This is positive, this is negative, holes will flow in this direction and so the direction of the movement of holes is the direction of current. So, this is the drain current here. To reverse bias, this is n-type, mind it, to reverse bias the junction, the gate has to be positive. So, the characteristics will be identical, only the polarities will be different. Here, we have taken $V_{GS} = 0$, $V_{GS} = 0$ here also will be the same, but here, these voltages have to be positive.

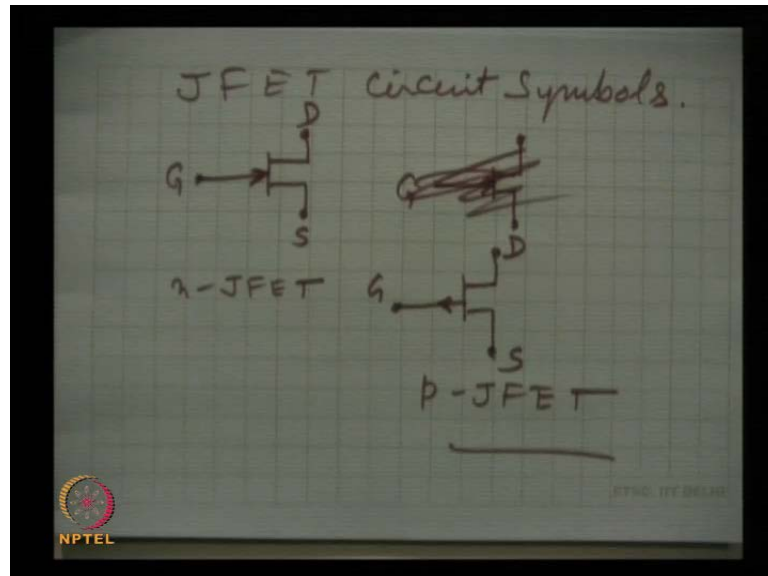
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So, the characteristics, the drain characteristic will be exactly the same. This is I_{DSS} , this is V_P , this is V_{DS} and this is I_D and this is V_{GS} , gate source voltage 0. Now, here this is different, plus 1 volt, plus 2 volt and, and so on. So, everything is same, but obviously, the mobility of electrons is higher. So, n-type JFET is more popular as compared to the p-type JFET. JFET is junction field effect transistors are fabricated in

discrete devices, as discrete devices and also on the chip in the integrated form; also, on the chip as ICs they are available.

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Now, about the circuit symbols, the circuit symbol for FETs, JFETs circuit symbols. This arrow gives a distinction, this is the circuit symbol for FET, this is gate, this is drain and this is source. This arrow, this gives, as in the case of n-p-n transistor, the arrow gives the direction of the conventional current, so on, that it has been derived. This is for n-type JFET and for p-type, except the arrow direction is reverse. So, this is gate, sorry, I am sorry, the direction has to be reverse, this is gate, this is drain and this is source. So, this is the circuit symbol for p-JFET.

We started with pointing the major difference of BJT as compared to FET, of FET as compared to BJT. Then, we talked about why FETs are so popular, that a much larger share in electronics is of the field effect transistors as compared to BJTs. There is one thing, which is, which is higher for BJT; the amplification factor is higher for BJTs as compared for FETs. So, BJTs are still very much in the pictures in the circuits, but there are several other features, which make these FETs much more popular.

We will continue, we will draw the I V characteristics and then, explain everything, which we studied about a BJT, same now it says different transistors and we will have to do the same way. So, we will go for I V characteristics, then we will talk MOSFET and

then we will develop other things, the modal amplifying factor we will determine and what are the parameters, which are significant in FET that we will see.