

Electronics
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Module No. # 01

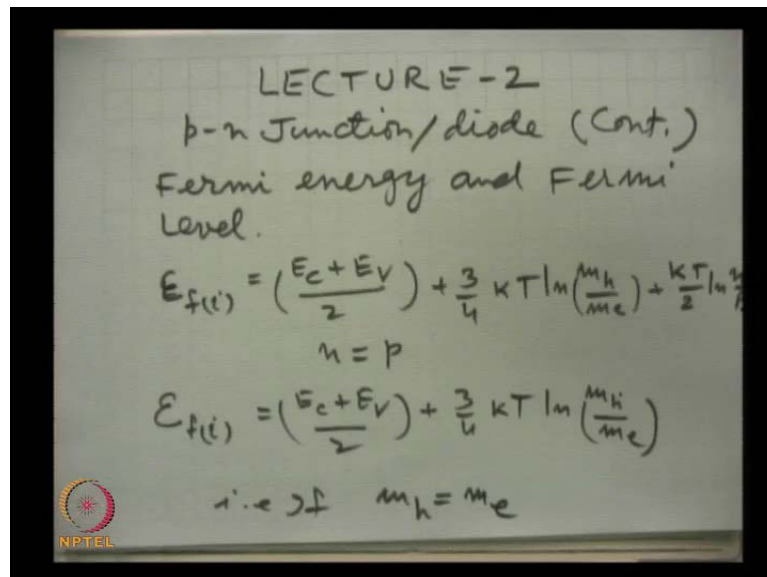
P-n Diode

Lecture No. # 02

P-n Junction /Diode (Contd.)

In the previous lecture, we discussed that how a p n junction is formed when one side of the semi conductor crystal is doped with p type, in the other side is doped with n type impurity, and the process is starts with the defusing of charges, and then because of the uncovering of the ionized impurities a field is established which gives raise to drift current taking equilibrium is established when diffusing current is equal to the drift current. Now, we move further we look on this currents in a diode, and the formation of the junction from a different angle.

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LECTURE-2
p-n Junction/diode (Cont.)
Fermi energy and Fermi level.

$$E_{f(i)} = \left(\frac{E_c + E_v}{2} \right) + \frac{3}{4} kT \ln \left(\frac{m_h}{m_e} \right) + \frac{kT}{2} \ln \left(\frac{n}{p} \right)$$

$n = p$

$$E_{f(i)} = \left(\frac{E_c + E_v}{2} \right) + \frac{3}{4} kT \ln \left(\frac{m_h}{m_e} \right)$$

i.e. > $m_h = m_e$

To understand that we must look at the concept of Fermi energy, and Fermi which is popularly known as fermi level. How we define Fermi level Fermi energy, this is the energy state for which the probability of occupancy is half. Now, for a semiconductor the

expression for fermi energy is this first, we consider for the intrinsic material and it is in this expression E_c is the lower edge of the conduction band and E_v is the upper edge of the valence band and KT ; T is the temperature; K is a Boltzmann constant; n and p are effective masses of hole and electron respectively and $\ln n$ by $\ln p$ is the concentration of electron density and this is the hole density.

Now, in intrinsic semiconductor as you know that each electron which has moved to the conduction band has left behind the hole. Therefore, the electron concentration electron density is equal to the hole density and therefore, this last term gets this becomes zero because n and p are equal and the expression for fermi energy. Fermi level is this E_c plus E_v by 2 plus $\frac{3}{4} KT \ln \frac{m_h}{m_e}$. If we further assume that the effective mass of hole is equal to the effective mass of electron, that is m_h is taken actually they are different because the electric field response is different for electrons.

And for holes but for the time being this is not they are not too widely different. So, we can assume that the effective mass of hole is equal to the effective mass of electron, then this term also vanishes and for the intrinsic semiconductor.

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$$E_{f(i)} \approx \frac{E_c + E_v}{2}$$

For n-semiconductor

$$n = N_D$$

$$n \cdot p = n_i^2$$

$$p = \frac{n_i^2}{N_D}$$

The fermi level exists in the middle of the forbidden band that is this is E_c , this is E_v , then almost in the center is the Fermi level. We can write the expression for n and p type semiconductor, because finally we have to deal with n and p materials. So, we write this expression of fermi level for n and p type material. So for n semiconductor we know

that electron concentration is equal to the donor density, donor concentration where we assume that all impurity atoms which have been added they are ionized that means each impurity atom has given one electron to the conduction band. Then this is true and for we can find out the hole concentration in n type material, and for that we use a very useful relation and that is $n p$ is equal to n_i squared where n is the electron concentration and p is the hole concentration in the same material and that means, if we are talking of n type material then these concentrations are in n material.

So, this is majority concentration **this is minority concentration** and the product of the two is equal to the n_i square, where n_i is the density of the intrinsic carrier concentration. So, from here we can find out how much will be the p since n is equal to n_d .

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The image shows a whiteboard with handwritten equations and an energy level diagram. The equations are:

$$E_{F(i)} = \left(\frac{E_c + E_v}{2} \right) + \frac{3}{4} kT \ln \left(\frac{m_h}{m_e} \right) + \frac{kT}{2} \ln \left(\frac{n}{p} \right)$$

~~~~~~  
Intrinsic position

$$E_{F(n)} = \text{Intrinsic position} + \frac{kT}{2} \ln \left( \frac{N_D}{N_i} \right)^2$$

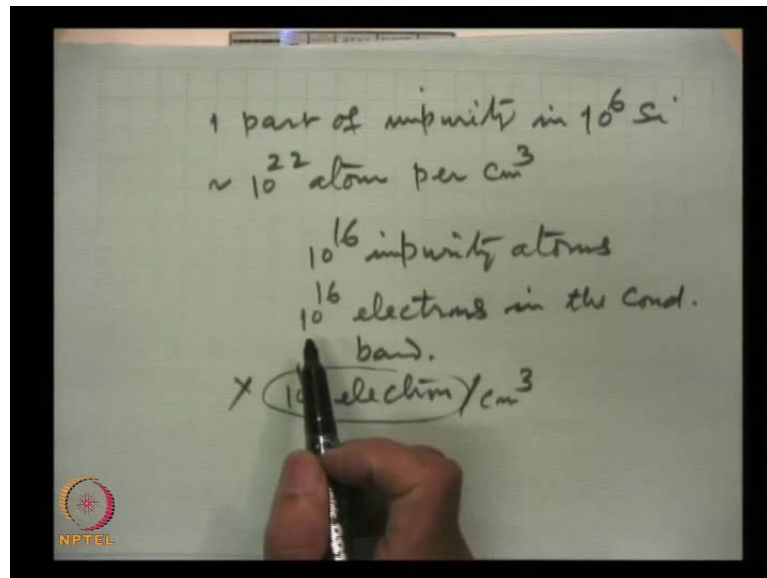
$$= \text{Intrinsic position} + kT \ln \frac{N_D}{N_i}$$

Below the equations is an energy level diagram. It shows three horizontal lines representing energy levels:  $E_c$  (top),  $E_v$  (bottom), and  $E_{F(n)}$  (middle). The  $E_{F(n)}$  level is positioned above the intrinsic level  $E_{F(i)}$ , which is indicated by a dashed line. The NPTEL logo is visible in the bottom left corner.

So, obviously  $p$  is equal to  $n_i$  square by  $N_D$  we substitute these values of  $n$  and  $p$  in the expression which we have earlier talked which is  $E_F$  this was for intrinsic material and this was  $E_c$  plus  $E_v$  by 2 plus 3 by 4  $kT \log m_h$  by  $m_e$ . This is actually as you know is the intrinsic position plus  $kT$  by 2  $\log n$  by  $p$  it was  $n$  by  $p$  and we substitute for  $n$  this is intrinsic position **intrinsic position** of Fermi level and here for  $n$  we substitute  $n_d$  and for  $p$  we substitute  $n_i$  squared by  $n_d$ . So, then the expression will become this is for n type material. So, we put it  $n$  here this is intrinsic position plus  $kT$  by 2  $\log N_D$  over  $N_i$  whole squared are substitute or substituted for  $n$  is equal to  $N_D$  and  $p$  equal to

$N_i$  squared by  $N_D$ . So, it is this and we can take this 2 here, so this becomes intrinsic position **intrinsic position** plus  $KT \log N_D$  by  $N_i$ ; that means, the Fermi level for n type material is because this is for intrinsic semiconductor. This is for  $f_i$  then here; that means, closer to the conduction band edge; this is the **this is the** fermi energy for n material. As we increase the doping concentration of the n type impurity, it will move more and more towards the conduction band edge.

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One more important thing if you remember, we said in the earlier that there is no positive contribution for the charge carriers which are present in the intrinsic material. We can see it here if we mix a impurity of the order of one part of impurity in one million host atoms in; that means, 10 to the power 6 silicon atoms for example. Then, there are you know from Avogadro's number, that there is roughly 10 to the power 22 atoms per cubic centimeter. Therefore, if one part of impurity is mixed in 10 to power 6; that means, one million silicon atoms, then you will have in the crystal one cubic centimeter 10 to the power 16 impurity atoms **impurity atoms**.

And, when we assume that all the impurity atoms are ionized, then one each atom has giving one electron to the conduction band. So, there are 10 to the power 16 electrons in the conduction band **in the conduction band**. Now, if you remember in silicon at room temperature that is 300 degree Kelvin, there are roughly 10 to the power 10 electrons per cubic centimeter. Now, this number 10 to power 16 is six orders of magnitude

higher. So the contribution of these electrons is negligible and the electrons which had been obtained by doping this are important. So, we remember that the fermi energy level in the n type material is closer to the conduction band, and similarly we can write the expression for the fermi energy level for the p type material.

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p - semiconductor

$$p = N_A$$

$$n = \frac{n_i^2}{N_A}$$

$$E_f(p) = \text{Intrinsic position} + \frac{KT}{2} \ln \frac{n_i^2}{N_A^2}$$

$$= \text{Intrinsic position} - KT \ln \frac{N_A}{n_i}$$

—  $E_c$

---  $E_f(p)$

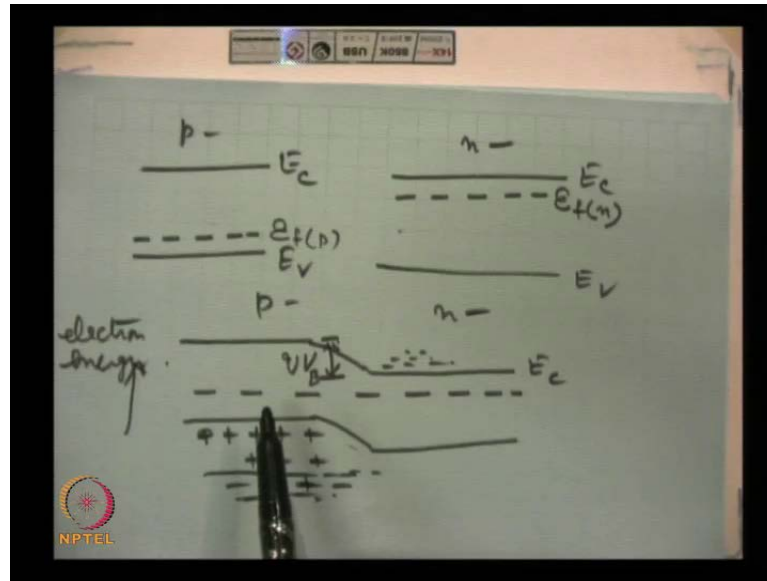
—  $E_v$

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For that the whole density will be equal to the acceptor atom impurity and this for p type material p semiconductor **p semiconductor** and this is equal to  $n_i^2$  by  $N_A$ . And then fermi energy for p type material this is equal to the intrinsic position **intrinsic position** plus  $KT$  by  $2 \log n_i^2$  by  $N_A^2$  and that gives this is equal to intrinsic position **intrinsic position** minus  $KT \log N_A$  by  $n_i$ . Now, look at this sign; this shows that it is for p type material. The fermi energy is below the conduction band and below the fermi energy for the intrinsic material and as we increase the acceptor impurity, the edge moves further into the valance band region here. This is the fermi energy for p type material; this is fermi energy level.

So, we understand that for the n type material, the fermi level is on the **on the** side closer to the conduction band and for p type. So, we can draw true because now what we are going to discuss? We will be discussing the energy band diagram potential energy diagram and for the p n junction. And that will enhance our understanding that what happens when we forward bias the junction; what happens when we reverse bias the junction. All this can be very well understood if we understand this.

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So, here is the p semiconductor and this is **this is** the fermi level for the p type material. Similarly, here is n semiconductor when they are separate. This is the position when they are separate and this is  $E_c$ ,  $E_v$  and this is the fermi level for the n type material. Now, when p n junction is formed; that means, when one side of the crystal is n type doped and the other side is a p type doped, then as we have discussed diffusing of charges occur. Now, till how long this diffuse on of charges and drift they will continue? It continues till the fermi levels on two sides get aligned. How? Let us see here. This is p side; this n side and here is the this is the fermi level throughout the crystal is aligned and it becomes same. Now obviously, this is the electron energy **electron energy** and a barrier has been formed in the height of the barrier this is an energy. So, if the contact potential is  $V_B$ , then this is  $q$  into  $V_B$ .

This is p type material majority are holes here **majority are holes** and here this is n type material, so there are electrons. These electrons do not have enough energy to cross over to the p type, because there is a potential energy difference. They should have this much energy at least, then only they will be able to cross over into move towards the p side. Similarly, this is uphill for holes; it was said earlier that electron energy increases upward then hole energy are downwards, so this is a uphill for holes. Holes also cannot move **cannot move** to the n side. This is the picture of the p n junction in equilibrium in the absence of any external field. From here actually, we can find out the expression very easily for the melting voltage, the contact potential as we call it or the barrier height, this

all can be calculated. If we subtract the difference, we have got the expression for the fermi level on the p side, fermi level on the n side, if both are subtracted then the difference should be equal to this potential height in that we do now.

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$$E_{f(n)} - E_{f(p)} = qV_B$$

where  $V_B = \text{Contact Potential.}$

$$V_B = \left(\frac{kT}{q}\right) \ln\left(\frac{N_A N_D}{n_i^2}\right) \text{ Volts.}$$

Ge,  $V_B \sim 200 \text{ mV}$  at  $300 \text{ K}$   
 Si,  $V_B \sim 500 \text{ mV}$  " "

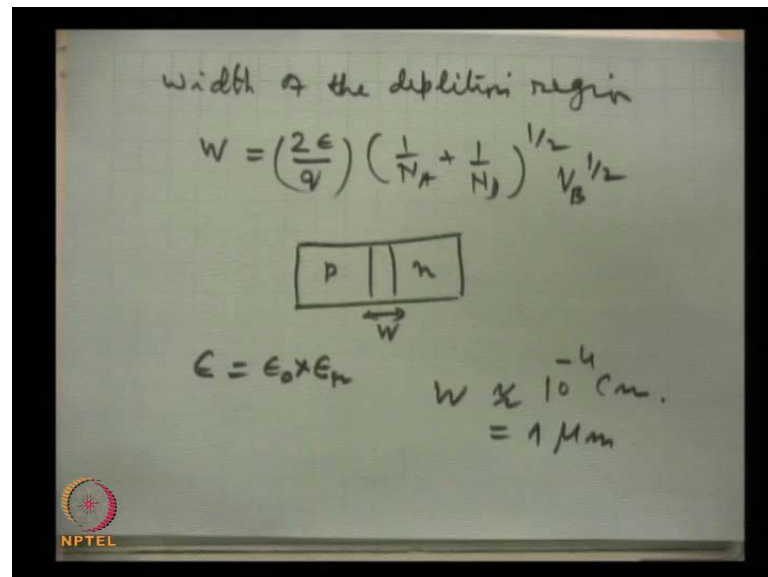
$\frac{kT}{q} = \text{voltage equivalent of temp.}$   
 $T = 300 \text{ K}$   
 $\frac{kT}{q} = 26 \text{ mV or } 0.026 \text{ V}$

If we subtract then we get the expression  $E_{f(n)} - E_{f(p)}$  that is fermi energy for the n type material minus fermi energy for p type semiconductor a line that they have a line; that means, difference of the two should be equal to where  $V_B$  is a contact potential. And when we substitute the values of this fermi energies, then this expression works out is simple you just substitute here the earlier expression what we have obtained for Fermi energy in the n type energy here; fermi energy for p type region and by substituting these values, we get the expression for contact potential  $\frac{kT}{q} \ln\left(\frac{N_A N_D}{n_i^2}\right)$  by  $n_i$ . This is in volts. For germanium  $V_B$  that is contact potential is of the order of 200 mille volts and for silicon this is around 500 mille volts at room temperature at 300 degree Kelvin and this also at 300 degree Kelvin. This term  $\frac{kT}{q}$  is volt equivalent of temperature **volt equivalent of temperature** and at room temperature at; that means, at  $T$  equal to 300 degrees Kelvin, this works out to be  $\frac{kT}{q}$  is equal to 26 mille volts or 0.026 volts.

So, will remember that these are roughly the values of the contact potential and this have n p explain that why the majority charge carriers in equilibrium will not be able to cross over? Because they do not have energy equal to or in access of this energy barrier height, and so the process is stops here. And we get this contact potential equal to 200 mille

volts for germanium in 500 mille volts for silicon. Depletion width is also a function of the applied voltage and the expression for that can be actually obtained. That is width of the depletion region  $W$ . This is given by  $2 \epsilon q N_A + 1$  by  $N_D$  half and this is built in voltage here.

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width of the depletion region

$$W = \left( \frac{2\epsilon}{q} \right) \left( \frac{1}{N_A} + \frac{1}{N_D} \right)^{1/2} V_B^{1/2}$$

Diagram of a p-n junction with depletion width  $W$  indicated.

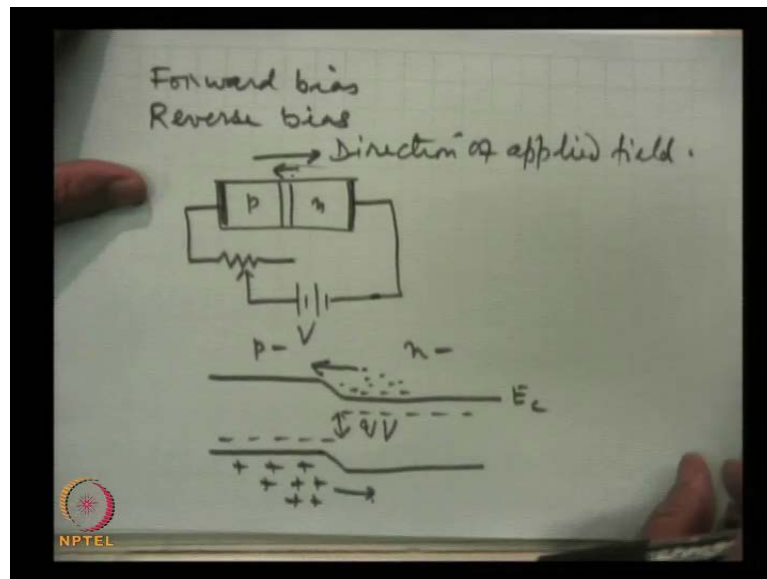
$$\epsilon = \epsilon_0 \times \epsilon_r$$

$W \approx 10^{-4} \text{ cm.}$   
 $= 1 \mu\text{m}$

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This is P material; this is n material; this is the depletion width  $W$  which is given by this expression, and it obviously depend on the impurity concentrations. And of course, the permittivity epsilon is the permittivity and which is equal to the permittivity of free space in to the real part of the dielectric constant for silicon this is around 11.5. And so we can calculate the value of the depletion width. This is around  $W$  is of the order of  $10$  to power minus 4 centimeter which is 1 micron 1 micro meter, this is the order of the depletion width. Now, depletion width also becomes a function of applied voltage which we will soon see.

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Now, we continue and we talk what happens when we bias the junction. By biasing we mean, we apply external voltage. There are two possibilities; one is called forward bias; the other is called reverse bias. Forward bias is when we connect the positive terminal of the d c source to the p type semiconductor, and the negative is connected to the n side, that is this is the situation. These are the (( )) context on the two sides and then we apply a voltage source, this is forward bias. You will recall that the built-in field has this direction.

This was if you look earlier loads, you will find that this is the direction of the built-in field. This voltage you know what is field? Field is voltage per unit length of the specimen. So, the two are directly proportional, they are related. Now, when we apply a voltage you forward bias the junction with voltage  $V$ , then this will give rise to a electric field opposite to the direction of the built-in field. This is the direction of the field we always take from positive to negative. This direction because here, there were positive ions on the p side, there were negative ions, so this was the direction. Now, here is the positive terminal; this is the positive terminal; this is negative.

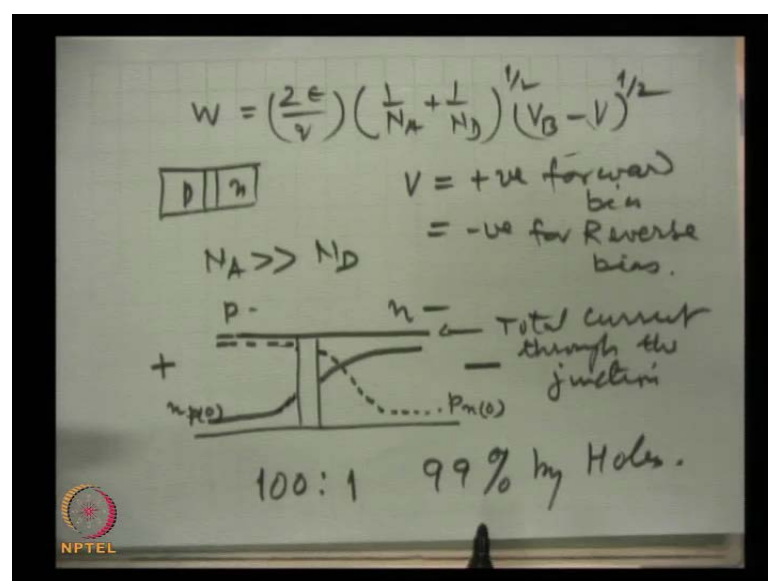
So, this is the direction of applied field in terms of the potential energy diagram. In equilibrium, we have seen that the fermi levels were aligned, but that is true only in the absence of any external; that means, any biasing. Once we bias it for example, as in this case then those fermi levels are again they become different in the two sides, and you see here that, this is n side; this is p side and the two levels gets separated again.

This extend of separation depends on this applied voltage; this is  $qV$ , where  $V$  is the applied voltage. Now, this applied field will be because this is more than the built in field, then it will take over and this electrons will be able to diffuse towards the p side. And similarly, because of the reduction in the **in the** barrier height these holes will also be able to cross over to the n side and this way a current will flow. The current will be mainly of this majority carriers holes from the p side to the n side; electrons from n side to the p side, they will constitute current in the same direction.

We have said it earlier that the direction of current is taken as the direction of hole motion, so electrons holes are moving in this direction. Hence, this current will flow from p towards n. Now, there are several interesting points. I said that depletion width also depends on applied voltage and the expression for depletion width was written. Here by simple my simple logic we can understand, because in forward bias lot of majority charge carrier like holes from the p side will be injected into the base region and then of course finally, they will move to the n region.

Similarly, lot of electrons are injected by a base region towards the p region and hence, the depletion region is suppose to decrease. Decreased with applied voltage and as applied voltage becomes higher and higher, depletion width will be decreasing. In the expression the dependence can be shown like this.

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This is the expression for... This is the applied voltage and this is biasing. Now, this is to be put  $V$  is positive for forward bias and negative for reverse bias. So, we have to substitute in this expression  $V$  with proper sign.

At the moment we are discussing the forward bias for that it is positive. So, we will decrease, but one point is to be noted that this term will never be negative, because when we increase the voltage then current becomes higher and higher making this term never zero or never negative. Depletion width return to be zero, but it will not be zero and but it decreases with the forward bias. And we can also discuss the flow of current, how the currents flow in the forward direction through another useful description in terms of the another diagram. We should take note of one thing that in devices normally  $s_m$  is a symmetric doping is used; that means doping in the p side and n side are not equal.

One doping is much higher as compare to the other doping. So for example, if we take a case when the doping on the p side is very large in comparison to the doping on the n side and then, we draw a picture that this is a n side; this is p side and we have applied the forward bias, then electron holes will diffuse from here towards the n region. In n region, they will meet lot of electrons so they will combine and they have exponentially the density decrease and finally, this is the hole density in the n region in thermal equilibrium. This is how we write  $P$  hole density  $n$  in n region and this zero indicates that it is in thermal equilibrium; what does it means? It means, if you look on the on n side like here, this is n side; this is p side. Now, n side has electrons in majority, but holes are also there in minority so that concentration is this. So finally, the hole density on the n side settles here. Now because of... Now, this is diffusing current mind it diffusion current.

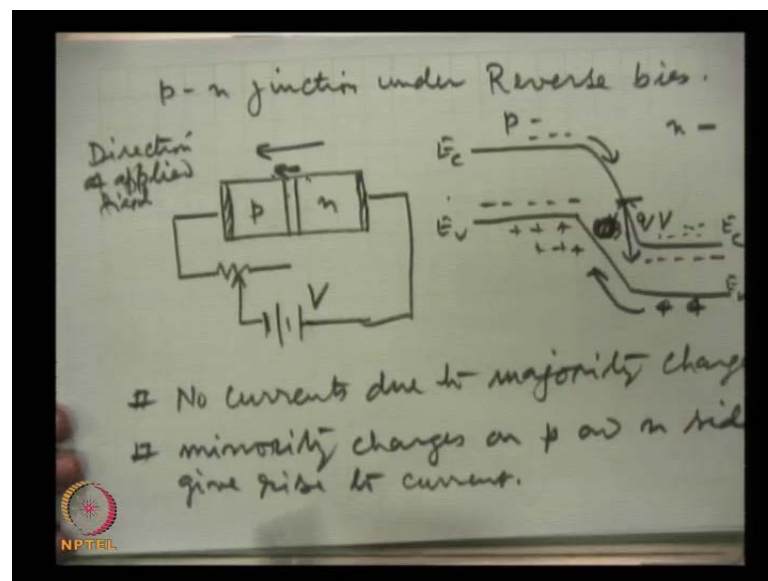
And we are discussing a case where acceptor density is much higher than the donor density. So, when this electrons the electron density near the junction will fall and there will be electron drift. This is the electron drift and this will in move through here and this is the current because of electrons; hole current here is mainly diffusion. This is electron current which are in minority; this is because electrons will drift here and then they will be dragged they will drift here.

And finally, it will settle at electron concentration in p region in thermal equilibrium. And because of this recombination, there will be a drift of in this region holes will also

drift. This is p side of the battery; this is the n side. So this is finally, this will be holes will also drift in this region. The total current is the sum of hole current in electron current. This is the total current **total current** through the junction **through the junction** and where major position will be of diffusion. But partly here this electrons because they will the carrier concentration in the region near the junction will fall so they will drift. Similarly, the electron concentration will fall in this region and electrons will drift under the applied field and they will form the current. So, actually there are both components of a current diffusion current and drift current, but major portion will be of diffusion current.

If we take that this  $N_A$  and  $N_D$  concentrations, they are in the ratio hundred verses one, then 99 percent current will be by holes and only one percent will be of electrons and most major portion of current is by holes. So major portion of current is diffusion current. This is how the currents flow in a forward bias p n junction and we could see that how useful is the concept of this potential diagram energy diagram.

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Then, we can discuss the p n junction under reverse bias. Here, we will see that this is our p n device. These are no contacts and this is the voltage and we have applied such that the negative of the battery is connected to the positive side p side and the positive of the battery is connected to the n side. Now here, the direction of the field which the applied voltage creates is this; this is the direction of applied field and this was also the

direction of the electric field; that means, two are in the same direction. So how the energy band diagram will become in this case; this is this is. This is  $E_c$ ,  $E_v$  fermi level in the p side this is p side.

This is n side and this is the fermi level and this is the potential barrier height which has gone up drastically and this is equal to  $qV_b$   $qV_{\text{barrier}}$   $qV$ . Now, we can discuss which electrons in which holes will form the current in this situation. It is clear that majority carriers were unable to cross over even when there was no field and the p-n junction was in equilibrium, because holes did not have energy which is required for the crossing over of the barrier potential barrier. Similarly, electrons did not have; now this barrier height has become much larger as compared to the earlier two cases. So here, these electrons and these holes they will not be able to move to diffuse at all in the on the opposite sides; that means, electron will not be able to move to the p side; holes will not be able to move towards the n side and hence, majority charge carriers do not take part in the current.

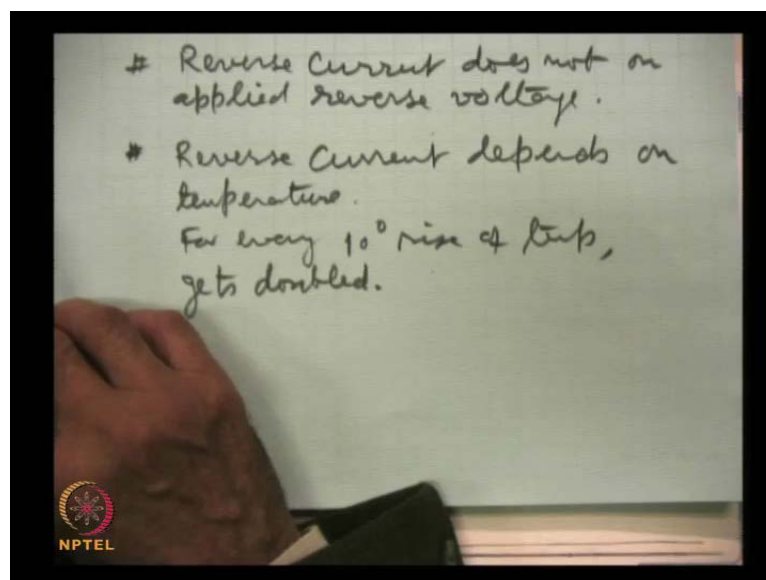
So, first thing we can conclude is no currents **no currents** due to majority charges. But let us now we will bring about the minority carriers. In the p material, there are besides majority of holes, there are electrons in minority. Similarly, in n type region there are holes in minority; that means, holes are here, but they have of course, they have fewer in number. Similarly, there are electrons here. These electrons which are minority charge carrier, these electrons will simply move downhill and will be able to go towards the n region. Similarly, these holes here they will be able to because this is again a downhill for holes.

So, the minority charge carriers constitute what is known as reverse saturation current. Minority charges on p and n side give rise to current. Now few things are important to note. All the charges by electrons in the p region the minority charges will not be able to contribute towards this current, because this region is full of the p type material is full of holes. So, electron far away from the junction when it tries to move towards the junction there is a it is highly probable that it will recombine.

Only those electrons which are in the depletion region, because making and breaking of bonds is a continuous process and so the electrons which are near the junction on the p side or in the junction, they will be over to cross over. And similarly, the electrons which are near the junction, they will be able to cross over near the junction and within the

depletion region. They will be **they will be** able to drift to the side, because of the so look at the polarities that holes from here they will be attracted by this side and they will constitute the current. Another thing is these charge carriers thermally generated charge carriers, the minority charge carriers they are they depend their concentration depends only on the temperature. So, by changing this reverse voltage the current is not going to change. This is there important point to remember that current reverse current is almost independent of the applied voltage, because the reverse voltage will change the barrier height. If this height is made more or less that does not make a difference, electrons any way will fall and similarly, these holes will fall to the p side.

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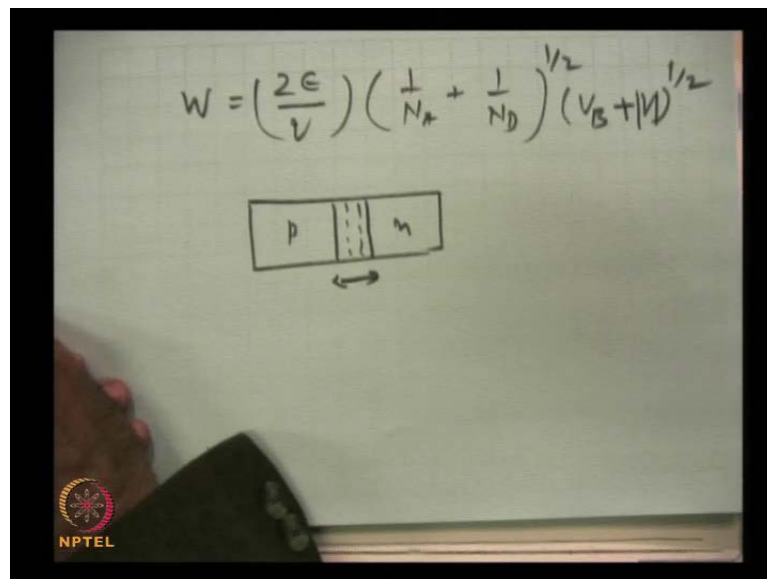


Therefore, this is important consideration, important point to remember that reverse current **reverse current** does not depend almost does not depend on applied reverse voltage **applied reverse voltage** and because these charge carriers, they are the function of temperature. So, reverse saturation current is a function of a temperature. Reverse current depends on temperature. Higher the temperature, higher will be the reverse current in by one estimate roughly for every 10 degrees rise of temperature, the reverse saturation current gets doubled. This is about the reverse saturation current.

And this becomes clear that reverse saturation current is very small and why it is called saturation current reversely saturated saturation current, because the charges which constitute this reverse saturation current they are very much limited in number and

immediately, they are they move under the applied field and there are not many chargers and hence, the current gets saturated very quickly. Here, these look at the polarities that electrons will be this field here the positive field here and negative field here, this will pull our apart more chargers more majority charge electrons will move towards the electrodes. Similarly, holes will move away from the junction. When they move; that means, that the ionized impurities larger in number will be uncovered and the depletion width will increase with the applied voltage

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The image shows a handwritten equation for the depletion width  $W$  of a p-n junction under reverse bias. The equation is:

$$W = \left( \frac{2\epsilon}{V} \right) \left( \frac{1}{N_A} + \frac{1}{N_D} \right)^{1/2} (V_B + |V|)^{1/2}$$

Below the equation is a simple diagram of a p-n junction. It consists of a rectangle divided into two regions: the left region is labeled 'p' and the right region is labeled 'n'. A vertical dashed line in the center represents the depletion region. A double-headed arrow below the rectangle indicates the width of the depletion region.

This is true even mathematically we have seen that this was the expression which we wrote earlier power half and here  $V_B$  minus  $V$  and we said that the sign of  $V$  has to be taken into account when we calculate the depletion width. So now, it was reverse bias, so this sign will be positive and that implies that higher the applied voltage, now we can put in we talk here only of magnitude.

So, higher the magnitude of the applied voltage, higher will be the width. So, if at certain voltage or under low voltage if this was the depletion width  $p$  and  $n$  region, then this depletion width becomes higher becomes larger as we apply the field. And so, this we will remember and we will see the implications of this.

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current-voltage characteristics of diode.

$$I = I_0 (e^{\frac{V}{\eta V_T}} - 1)$$
$$V_T = 26 \text{ mV} = 0.026 \text{ V}$$
$$\eta = 1 \text{ Ge}$$
$$\eta = 2 \text{ (Si)}$$

Forward bias

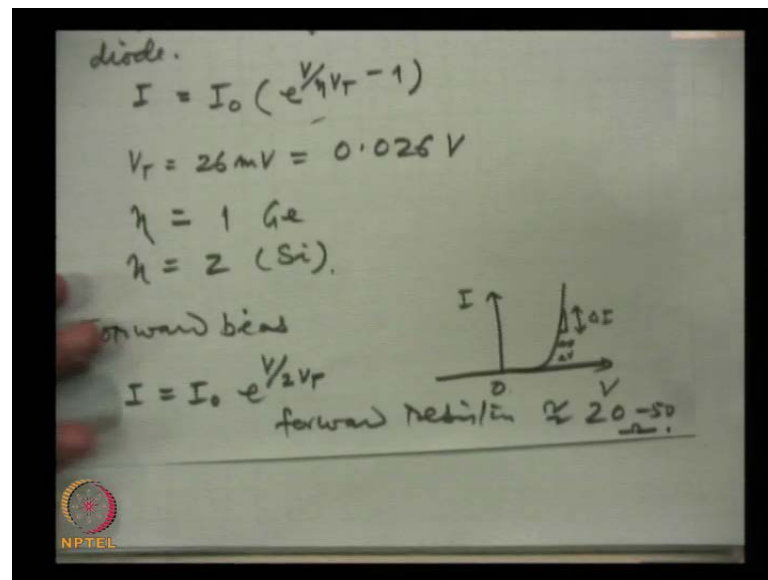
$$I = I_0 e^{\frac{V}{2V_T}}$$

A graph showing current  $I$  on the vertical axis and voltage  $V$  on the horizontal axis. The curve starts at the origin and rises exponentially for positive  $V$ .

Now, we will talk about current voltage characteristics of a diode current  $I$  which flows through the diode is related with the applied voltage by this equation. This is the expression which gives the  $i-v$  characteristics which expresses  $i-v$  characteristics of a diode. Here,  $V_T$  as we said earlier this is the volt equivalent of temperature and this is equal to 26 millivolts or 0.026 volts;  $\eta$  is equal to one for germanium diode and  $\eta$  is equal to two for silicon diode. So, this equation and  $V$  of course, is the applied voltage which we have to consider the appropriate sign. For forward bias it is positive; for reverse bias it is negative. When we plot these first we consider forward bias, then the characteristics we can see from here that when  $V$  the applied voltage is large compared to the thermal equivalent of the volt equivalent of temperature  $V_T$ , then this term the exponential term will become soon very large and one can be dropped.

And in that case, the current will exponentially rise with the applied voltage and the expression of course will become if we consider a silicon diode, then it will be this and this current will increase exponentially with the applied voltage. So, if this is the current and this is the voltage, the current rises exponentially. And to limit the current the current should not exceed, then the prescribed rate of current for the diode by the manufacturer we normally use a resistance in series with the diode.

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And in the reverse bias case, so this is understood that current increases exponentially with the forward bias. And another thing is that we can find out the resistance of the diode in the forward direction by taking this is small triangle. This is change in current which occurs because of change in voltage a small change in voltage when change the current drastically and hence, the resistance is a very small and forward resistance for a diode is around 20 to 50 ohms. We will continue our discussion of p n junction. Next, we have to discuss what happens in the reverse bias.