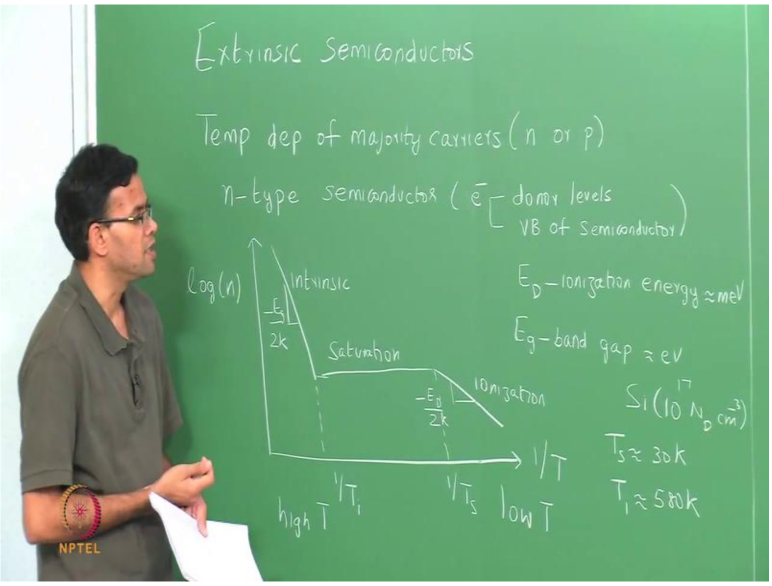
# Fundamentals of electronic materials, devices and fabrication

**Dr. S. Parasuraman**
**Department of Metallurgical and Materials Engineering**
**Indian Institute of Technology, Madras**

## Lecture - 08
## Extrinsic Semiconductors – Conductivity

Let us start with the brief review of last class. In last class, we continued discussing about extrinsic semiconductors.

(Refer Slide Time: 00:24)



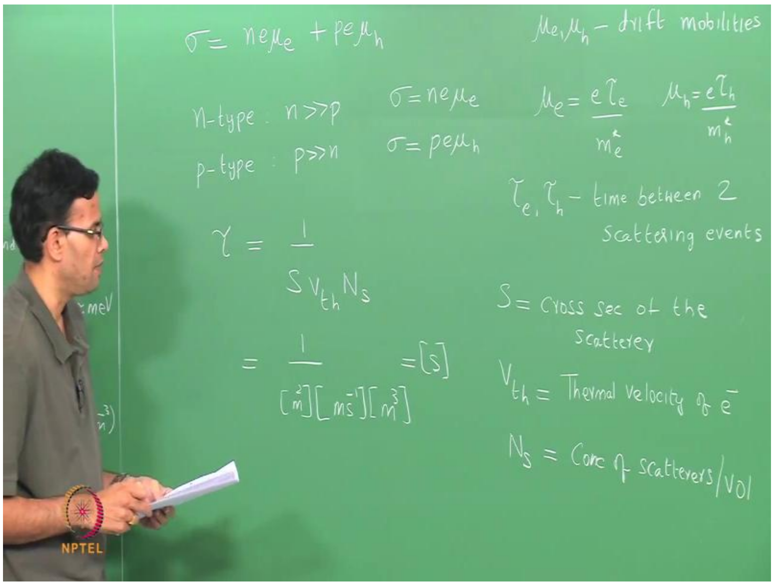
And, if you remember extrinsic semiconductors are those where we add a small amount of a specific impurity in order to selectively increase the concentration of either electrons or holes. Towards the end of last class, we looked at the temperature dependence of the majority carrier concentration. So, these would be electrons in the case of n-type semiconductors; and holes, in the case of p-type semiconductors. We use the example of an n-type semiconductor and whatever discussion that we do using n-type, the same is valid for a p-type.

So, in this case, electrons are the majority charge carriers and they are essentially two sources of electrons. One, your electrons can come from the donor levels, these levels are close to the edge of the conduction band at high temperatures the electrons can also come from the valance band of the semiconductor. Putting these 2 information together, we did a plot of the log of the electron concentration versus 1 over T. So, this is $\log(n)$, this $1/T$. Since this is 1 over the temperature, this represents the high temperature side, this represent the low temperature. In this plot, we said that we could divide an extrinsic semiconductor into essentially three regions. At low temperature, the concentration of electrons is dominated by those electrons that come from the donor level. So, if you plot n versus $1/T$, we are going to get a straight line with the slope that was given by the ionization energy. So, $E_d$ is the ionization energy of the donor. We also saw that this is typically of the order of milli-electron volts.

Once all the donor atoms are ionized we have a regime, where the electron concentration is more or less constant. And then at high temperature, we find that we have electrons that come from the valance band and your extrinsic semiconductor behaves like an intrinsic one. So, this is the high temperature behavior, and the source is $\frac{-E_g}{2k}$, where $E_g$ is the band gap. And, this is usually of the order of electron volts. So, we have 3 regimes in the case of an extrinsic semiconductor. The low temperature one we call the ionization regime, because it is dominated by ionization of the donor atoms. Then you have a saturation regime, where the concentrations of electrons which are the majority charge carriers, it is nearly a constant. And then we have an intrinsic regime where your extrinsic material behaves like an intrinsic one. We also called the temperatures corresponding to these as $T_s$ which is your saturation temperature and $T_i$ which is your intrinsic temperature.

We did some calculation for the value of $T_s$ and $T_i$ in the case of silicon with 10 to the 17 donor atoms, and we got a value of $T_s$ that was approximately 30 Kelvin and a $T_i$ which is approximately 580 Kelvin, which means there is a wide temperature range where the concentration of the majority carriers is nearly a constant, and it is equal to the concentration of your donor or your accepter. So, we have 2 advantages, if we dope semiconductors. The first is that the conductivity increases, because the carrier concentration increases. With secondly, we also have a regime where the carrier concentration is almost a constant and it is independent of temperature. So, today we will go further and talk about conductivity in the case of an extrinsic semiconductor, and how that depends upon temperature.

(Refer Slide Time: 06:24)

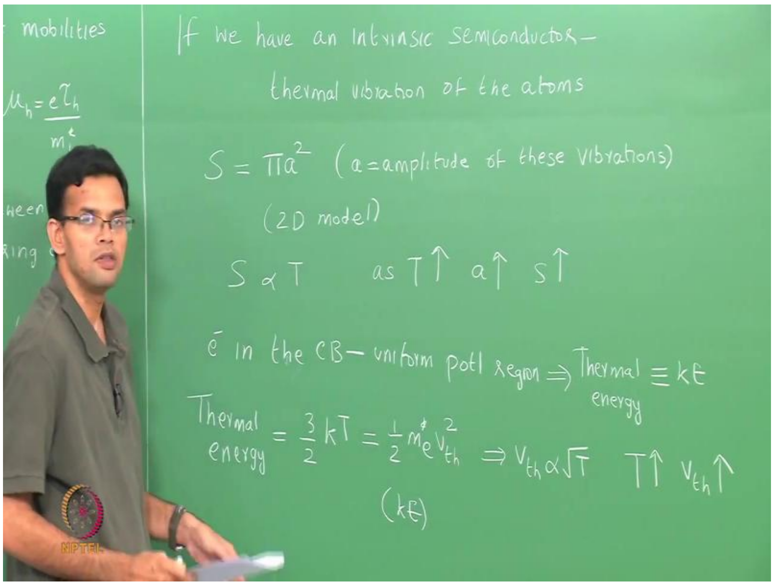


So, we start with the equation for conductivity. We have written this earlier $\sigma = n\ e\ \mu_e + p\ e\ \mu_h$, this is a general equation for the conductivity. If you have an n-type semiconductor, n is typically much larger than p. We saw in the case of silicon that n could be more than 7 or 8 orders of magnitude higher depending upon the dopant concentration, in which case sigma would just be $n\ e\ \mu_e$. In the other hand, if you have p-type semiconductor, p is much larger than n; in which case sigma will just be $p\ e\ \mu_h$. We have seen $\mu_e$ and $\mu_h$ earlier. $\mu_e$ and $\mu_e$ are the drift mobilities. So, $\mu_e$ is the mobility of the electron in the conduction band, $\mu_h$ is the mobility of the hole in the valance band. We also saw earlier that $\mu_e$ symbol $\frac{e\tau_e}{m_e^*}$, $\mu_h$ $\frac{e\tau_e}{m_h^*}$, where $\tau_e$ and $\tau_h$ are the time between 2 scattering events.

Now if we want to look at the temperature dependence of the conductivity, we need to look at the temperature dependence of the carrier concentration and also the temperature dependence of the mobility. You have done looking at the temperature dependence of the carrier concentration which is what we did at the end of the last class, the beginning of today. Now we look at how $\mu_e$ and $\mu_h$ depend on both temperature, and in the case of extrinsic semiconductor how it depends upon the presence of these dopants.

Now there is in another way we can right $\tau$ which is the time between 2 scattering events. $\tau$ can be written as $\frac{1}{S\,V_{th}N_s}$. So, what are these terms? S represents the cross section of the scatterer, $V_{th}$ is the thermal velocity of the electrons and $N_s$ is the concentration of the scatterer. If we plug in the units, S is the cross section area, which is in $m^2$; $V_{th}$ is the velocity so that is $m\ s^{-1}$. $N_s$ is the concentration of scatterer, it is usually given per unit volume, so this is in $m^3$, so that the finally, unit is in seconds. So, to understand this, if you have a larger cross section of the scatterer, then you are going to have a shorter scattering time. If the electrons are in travel faster, then once again they can interact between two scattering events quickly, so time will be short. And if you have more number of scatterers, once again the time will be short. Now, the question is what are these scatterers that we talk about, and how do these values depend on temperature.

(Refer Slide Time: 11:16)



mobilities

$\mu_h = \frac{e\tau_h}{m_h^*}$

ween

ring

If we have an intrinsic semiconductor –

thermal vibration of the atoms

$S = \pi a^2$ ($a$ = amplitude of these vibrations)

(2D model)

$S \propto T$ as $T\uparrow$ $a\uparrow$ $S\uparrow$

$e^-$ in the CB – uniform potl region $\Rightarrow$ Thermal energy $\equiv$ kE

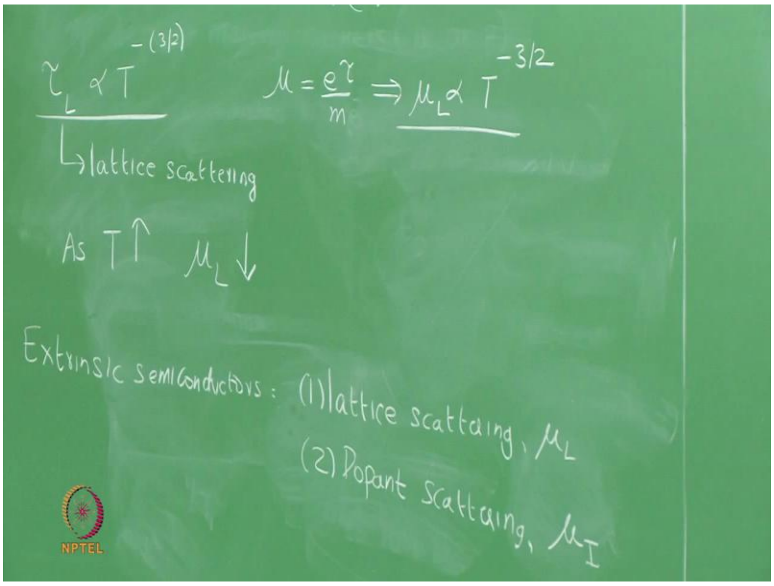
Thermal energy $= \frac{3}{2}kT = \frac{1}{2}m_e^* V_{th}^2 \Rightarrow V_{th} \propto \sqrt{T}$ $T\uparrow$ $V_{th}\uparrow$

(kE)

Let us start first with intrinsic semiconductors. If we have an intrinsic semiconductor then the electrons will scatter because of the thermal vibration of the silicon atoms. So, we have thermal vibration of the atoms. So, if S is the scattering cross section, S can be written as $\pi a^2$, where a is the amplitude of these vibrations. So, this is in the case of a simple 2 D model. We can show that if your scatterers or your thermal vibration of the atoms then S is proportional to the temperature, which means as temperature increases, the amplitude of the vibrations increase. So, a increases and correspondingly S will also increase. The next term in the equation for $\tau$ is $V_{th}$. If you have electrons moving in the conduction band, we can say that they are moving through a uniform potential region, and in this case, we can say that the thermal energy of the electrons is approximately the same as their kinetic energy. Typically thermal energy is given as $3/2\ kT$, and, the kinetic energy is nothing but $\frac{1}{2}m_e^*V_{th}^2$, so this is the kinetic energy. So, if we use this expression,

$V_{th}$ is proportional to square root of temperature, which means once again as the temperature increases the thermal energy increases, so the kinetic energy will also increase, so $V_{th}$ will increase.

(Refer Slide Time: 15:02)



$\tau_L \propto T^{-(3/2)}$

↳ lattice scattering

As T↑ $\mu_L$↓

$\mu = \frac{e\tau}{m} \Rightarrow \mu_L \propto T^{-3/2}$

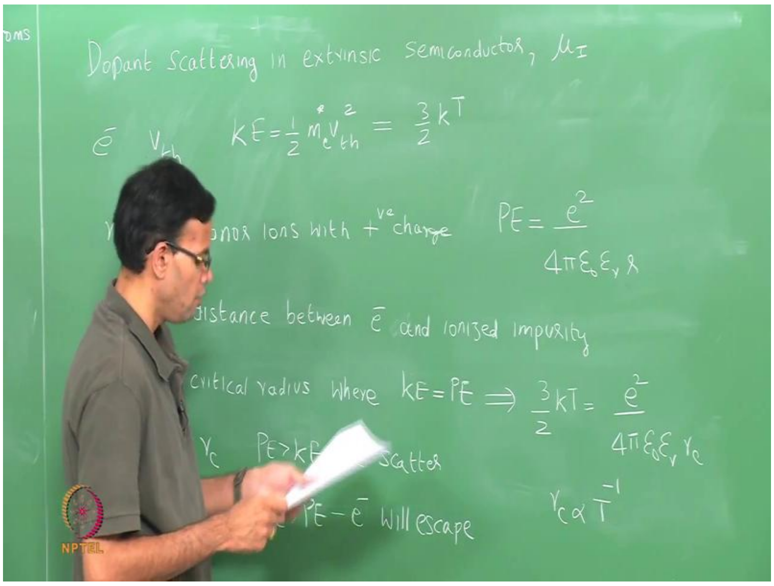
Extrinsic semiconductors : (1) lattice scattering, $\mu_L$

(2) Dopant scattering, $\mu_I$

So, let us put these 2 terms together. So, we have the expression for tau which is nothing but $\frac{1}{S\,V_{th}N_s}$; in the case of an intrinsic silicon atom, we said that the scattering is only due to the lattice vibrations. So, we wrote this as $\frac{1}{\pi a^2 V_{th}N_s}$. We found that $\pi a^2$ is directly proportional to 1/T. $V_{th}$ is proportional to $\sqrt{T}$, which means $\tau$ is proportional to $\sqrt{T}/T$; $N_s$ is a number of atoms and that is usually a constant, it is not going to change with temperature. So, if you take these 2 into account, which is proportional to $T^{-3/2}$. So, $\tau$ due to the scattering of the lattice, I am just going to denoted as $\tau_L$ is proportional to $T^{-3/2}$, may call this. Now $\mu$ is equal to $\frac{e\tau}{m}$, and since $\tau$ is proportional to $T^{-3/2}$, we can say that $\mu \propto T^{-3/2}$.

So, if you have an intrinsic material, where the conductivity is by this scattering is due to the vibration of the lattice atoms as the temperature increases the vibration increases. So, there is more scattering and hence the mobility will go down. So, I will write this as $\mu_L$ to denote that it is due to lattice scattering. So, as temperature increase, $\mu_L$ will decrease. So, this make sense, because the temperature increases you have greater lattice vibrations and also you have electrons there are traveling faster. Now in the case of extrinsic semiconductor, you also have this lattice scattering because we also have the silicon lattice if your material is silicon. So, you also have the lattice scattering, this is given by a term mu L, but you also have this scattering due to your dopants whether they be donors or acceptors, we are going to call that $\mu_i$. So, i is to denotes the fact these are impurities. So, in the case of extrinsic semiconductors, you have scattering due to the lattice; you also have scattering due to the dopants. So, both of them play a role in determining the mobility of the electrons and holes. The lattice scattering term is very similar to what we did for intrinsic semiconductors. So, once again $\mu_L$ will be proportional to $T^{-3/2}$. The one thing we have to see is how the dopants scattering changes with temperature.

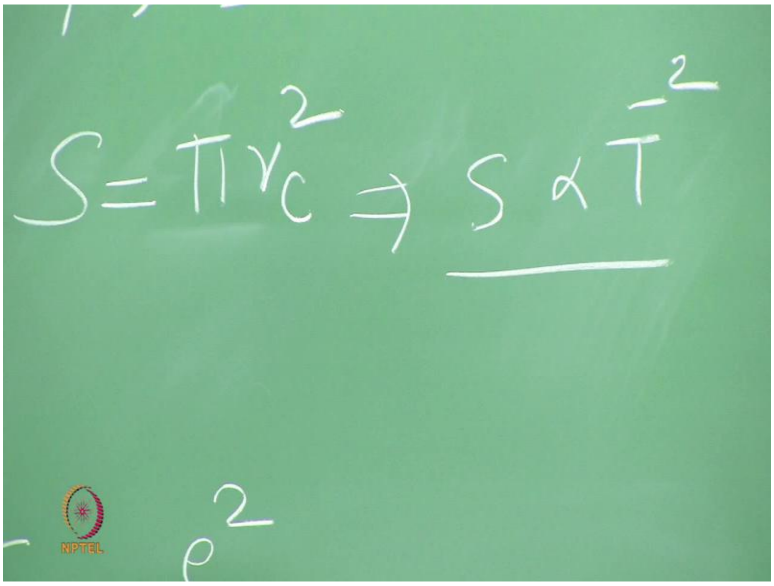
(Refer Slide Time: 19:30)



So, we want to look at the dopants scattering in an extrinsic semiconductor, we call this $\mu_i$. We want to find out the temperature dependence of this term. So, if you look at in extrinsic semiconductor, so whether you have an n-type or p-type, you are going to have donors and acceptors and these are ionized, because, we find that in case of n-type, the donor atom has an extra electron that goes to the conduction band; in the case of a p-type, if you have an acceptor atom that can accept and extra electron and create a hole. So, these are ionized impurities and these can then interact with the electron. So, if you have an electron with velocity being $V_{th}$ then the kinetic energy is $\frac{1}{2} m_e V_{th}^2$ or $\frac{1}{2} m_e^* V_{th}^2$. We said that in the case of an intrinsic semiconductor where an electron is traveling in the conduction band; this kinetic energy is nothing but the thermal energy, so this is 3/2 kT.

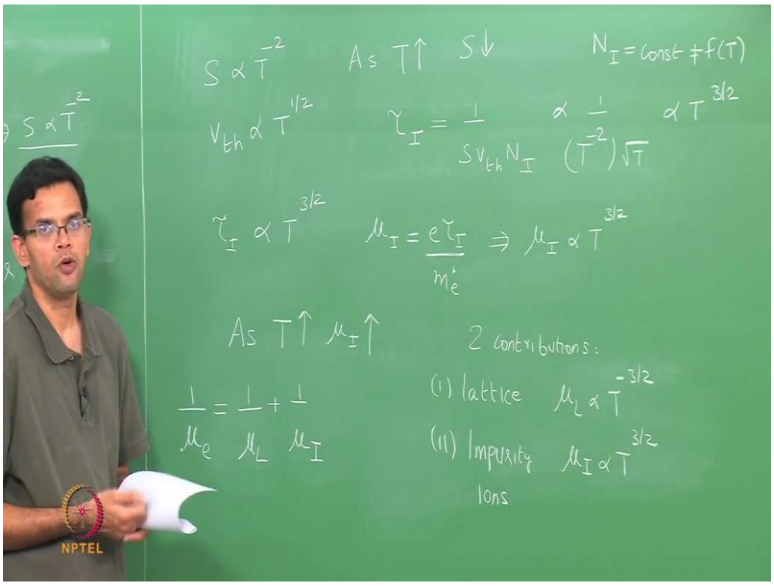
But now you have the electron having an electrostatic force of attraction with the ionize donor. So, if you have an n-type, you have donor atoms or donor ions with the positive charge and these can interact with the electrons. So, this electrostatic force, I will call it a potential energy is nothing but $\frac{e^2}{4\varphi\varepsilon_o\varepsilon_r r}$. So, r here is the distance between the electron and the ionize impurity. Usually in the case of extrinsic semiconductors, we define a critical radius $r_c$, where the kinetic energy and potential energy are equal. If r is less than $r_c$, if r less than $r_c$ here, then the potential energy is greater than the kinetic energy, and your electron will scatter. If r is greater than $r_c$, it is the reverse; the kinetic energy will be greater than the potential energy in the electron will not scatter or the electron will escape. Matching these 2 terms, we define a critical radius when the kinetic and potential energies are equal. If we do that we can say $\frac{3}{2kT} = \frac{e^2}{4\varphi\varepsilon_o\varepsilon_r r_c}$, which means $r_c \alpha T^{-1}$.

(Refer Slide Time: 24:16)



Now, if you want to look at the cross section for scattering S is nothing but $\varphi r_c^2$ and knowing that $r_c \alpha T^{-1}$, $S \alpha T^{-2}$.

(Refer Slide Time: 24:45)

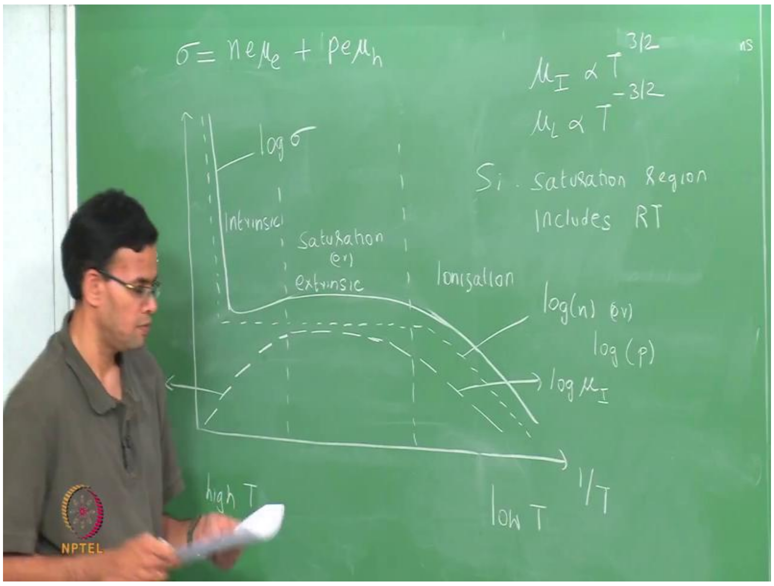


So, in the case of an extrinsic semiconductor, where we are looking at the interaction of the electrons with the ionized impurities, we find that the scattering cross section area $S\ \alpha\ T^{-2}$. This we got by looking at the balance between the kinetic energy of the electron and the potential energy of attraction between the electron and the ionized impurity. As temperature increases, the electron can travel faster which means the kinetic energy becomes higher, so becomes easier for it to escape the influence of the ionized impurity which means the scattering cross section S goes down. Earlier we saw that $V_{th}\ \alpha\ T^{1/2}$ to the half, this is the same argument that we use in the case of an intrinsic semiconductor.

Putting these 2 together tau due to scattering from the impurities, so it is $\tau_I = \frac{1}{S\,V_{th}N_I}$. Once again, $N_i$ is the concentration of impurities which is a constant, it is not a function of temperature. So, this is proportional to $1/T^{-2}$ in the case of S, and then $\sqrt{T} \alpha T^{3/2}$. So, $\tau_I$ which is the time due to scattering because of impurities is proportional to $T^{3/2}$. $\mu_I$ is nothing but $\frac{e\tau_I}{m_e^*}$. So, $\mu_I$ is proportional two half, which means the contribution of the impurities to mobility is such that as the temperature increases $\mu_I$ increases. And this is because as the temperature increases your electrons can move faster and so they can easily escape the electrostatic force.

So, in the case of an extrinsic semiconductor, we have two contributions to the mobility one is from the lattice, and we saw earlier that this is proportional to $T^{-3/2}$; the other is from the impurity for your dopants and these are ionized. So, I will write these as impurity ions when $\mu_I$ α $T^{3/2}$ . So, we have two contributions both of which have an opposite dependence on temperature. If you look at the total mobility, it will be dominated by whichever scattering process has the lower value. So, we can write $\frac{1}{\mu_e} = \frac{1}{\mu_L} + \frac{1}{\mu_I}$ . so, this in the case of an extrinsic semiconductor, where we have contribution due to both the impurity atoms $\mu_I$ and the lattice $\mu_L$. So, let us put this together and then do a plot of the conductivity versus one over temperature.

(Refer Slide Time: 29:12)

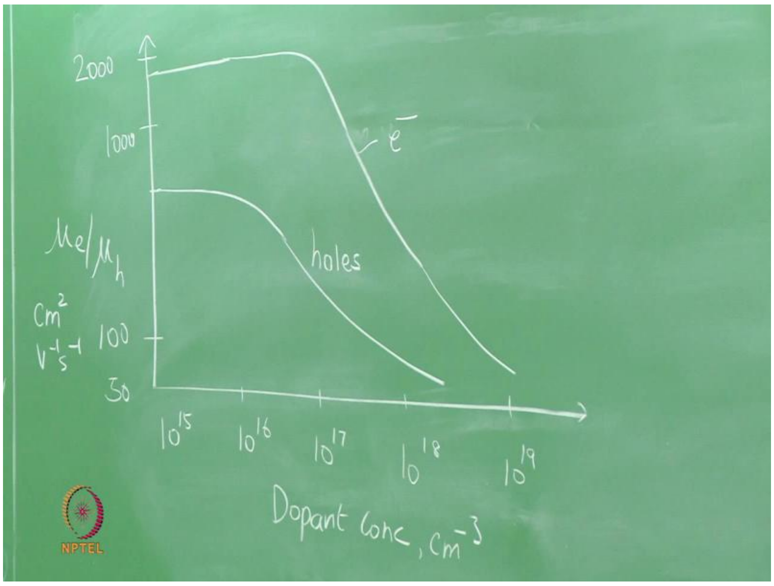


Again let me rewrite the equation for the conductivity; $\sigma = n\ e\ \mu_h + p\ e\ \mu_h$. So, in this equation, the first thing we looked at is the carrier concentration. So, on a log scale, this is 1/T. Since this is 1/T over T, this end is the high temperature end; this is your low temperature end. If you plot log of the carrier concentration, and this is similar to what we had before, so it high temperature, you have an intrinsic contribution, you have a saturation region, where the concentration is nearly a constant, then you have low temperature region where it is due to ionization of your donors or acceptors. So, this is log n or log p. If we then plot the log of the mobility, we find that at low temperature mobilities are dominated by scattering due to the impurities, because at low temperature your lattice vibrations are very small. So, the mobility is dominated by impurity scattering and as temperature increases, your mobility increases. Remember $\mu_I$ α $T^{3/2}$ is proportional T to the 3 over 2. If we do that then this is the contribution due to the scattering of the ionized impurities. So, this is $\log\mu$ at low temperatures. So, it is dominated by impurities.

At high temperatures scattering is dominated by the silicon lattice in which cases $\mu_L \alpha T^{-3/2}$, so that as the temperature increases $\mu_L$ goes down. So, this is $\log \mu_L$. At intermediate temperatures both the scattering from the lattice, and the scattering from the impurities will be more or less equal. So, the first dotted line represents n, the second dotted line or dash line represents $\log(\mu_L)$. If we put both these together, we will get the conductivity. And if we plot the conductivity, which is the solid line, we get a curve like this. So, this is $\log(\sigma)$ versus $1/T$. We just erase this section and plot it slightly better, this is $\log(\sigma)$. So, once again we have three regions; at low temperatures, we have an ionization region; at high temperatures, we have an intrinsic region; and then there is a region in the middle, where $\sigma$ does not change much with temperature and that is your saturation region; another four for the saturation region is your extrinsic region.

So, doping gives us 2 advantages - one is that it increases the conductivity, but at the same time there is also a temperature region where both the carrier concentration and hence the conductivity is almost a constant and is independent of temperature. In the case of silicon, this saturation region or the extrinsic region is around room temperature or I should say includes room temperature, which means if you have doped silicon then your conductivity is almost a constant in an around room temperature, this is very important when we try and form devices later with these extrinsic semiconductors. So, this is the carrier concentration as a function of temperature. So, how does the carrier concentration in the case of extrinsic semiconductors change with dopant concentration? So, let me just plot $\log(\mu)$ versus dopant concentration.

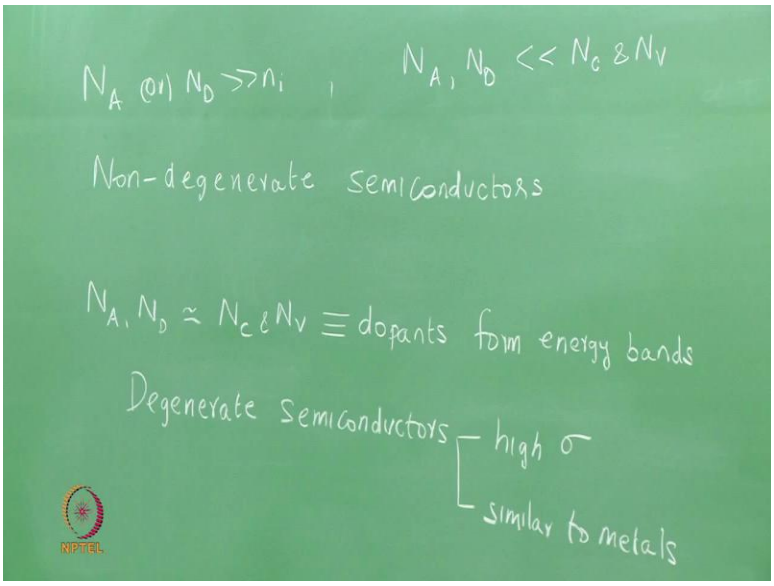
(Refer Slide Time: 34:43)



So, I want to plot how $\mu_e$ or $\mu_h$ changes with concentration of the dopants. This is $\mu_e$, $\mu_h$; we will use the example of silicon, but this is again true for any other semiconductor. This is dopant concentration square. So, we in increase the dopant concentration, the overall mobility decreases, because now you have more scattering from these ionize impurities. So, let me make the plot 100, this is your y-axis; concentration is $10^{15}$. So, if you plot $\mu_e$ starts at high value in the case of silicon at room temperature, $\mu_e$ for intrinsic silicon is around 1315 $cm^2$ $V^{-1}$ $s^{-1}$. So, let me just write down the units here centimeter square per volts per second. So, it starts of high; initially your mobility is more or less constant; and then as your dopant concentration increases, the mobility starts to drop. This is for electrons.

We can do similar plots for the holes. Once again when we have intrinsic silicon the hole mobility is around 450 1315 $cm^2$ $V^{-1}$ $s^{-1}$. So, if you do a similar plot for holes, again it is stay a constant, but then it is start to dropdown. In all the extrinsic semiconductors we have considered so far, you always had the situation $N_A$ or $N_D$ - whether these are acceptors or donors is much greater than $n_i$ which is your intrinsic carrier concentration, this means that we can say that the electron concentration is equal to $N_D$ or the hole concentration is equal to $N_A$.

(Refer Slide Time: 37:09)



$N_A$ (or) $N_D >> n_i$ , $N_A, N_D << N_c$ & $N_v$

Non-degenerate semiconductors

$N_A, N_D \simeq N_c$ & $N_v$ ≡ dopants form energy bands

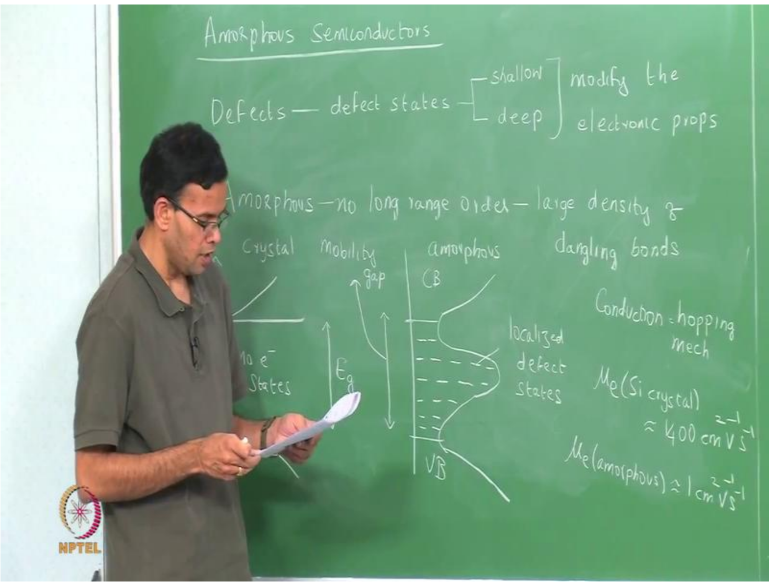
Degenerate semiconductors — high $\sigma$

— similar to metals

We also only consider the situation where $N_A$ and $N_D$ are much smaller than the effective density of states $N_c$ and $N_v$. So, this allows us to think of these impurities as localized states in the band gap. So, your donors from localized states just below the conduction band and the acceptors from localized states just about the valence band. These semiconductors are called non-degenerate semiconductors this is true for almost all carrier concentrations that we normally encounter, but if we have really high doping values, so that $N_A$ and $N_D$ are comparable to $N_c$ and $N_v$, we can no longer think of them as localized states, but we say that the dopants form energy bands. So, these semiconductors are called degenerate semiconductors, because your dopants form energy bands, it is also possible that these bands can overlap with the conduction band or the valence band.

So, degenerate semiconductors have high conductivity, because they have a high concentration of impurities, but they also behave very similar to metals. For most of the devices that we discussed, we will essentially deal with non-degenerate semiconductors, but for some cases will find and we can also have high doping and will also have degenerate semiconductors.

(Refer Slide Time: 40:16)



The last topic, that I want to cover when we are talking about electronic materials are Amorphous Semiconductors. So far, when we have talked about an intrinsic semiconductor or when we talked about an extrinsic semiconductor, we always consider materials that are single crystals which are perfect and have no defects. This is because defects in a material will introduce states in the band gap, and will change the electronic properties. Defects will cause defect states. We saw earlier that these states can either be shallow - shallow states are those there are close to the band edges, they can be close to the conduction band edge or they can be close to the valence band edge or they can be deep states. So, these defect states can essentially modify the electronic properties.

So, defects can be good or bad. For example, if you are trying to look for higher conductivity then defect states can essentially act as traps and trap electron in holes and then reduce the conductivity, in that case defect case are essentially bad. On the other hand, in the case of some direct band gap semiconductors, we can have defect states in them that can modify the optical properties, in such cases defects states are good. So, depending upon the applications, we may or may not one defect states. And, amorphous semiconductor is an extreme example of a semiconductor the large number of defect states. An amorphous material has essentially no long rage order, which means there is a large density of dangling bonds. Dangling bonds are formed when we have one silicon atom which has one electron, but there is no opposite silicon atom to supply another electron to form the bond. So, amorphous materials are characterized by having a large density of dangling bonds; in these dangling bonds, basically act as defect states in the band gap.

So, if you were to draw the band picture in the case of a crystalline material so, this is a crystalline material, let us take crystalline silicon. So, we will have a conduction band, we will have a valence band that is your band gap. So, if we have a perfect crystalline material, there are no electronic states in the band gap then, you have a density of states in the conduction band and the density of states in the valence band. Now if we have an amorphous semiconductor, because you have a large density of dangling bonds, there will be a large density of defect states in the band gap, and these defect states are localized states. So, if I were to draw the band diagram for amorphous material, so once again I will mark $E_c$ and $E_v$. So, I will have a large density of states in the bands; but within the band gap, we will also have localized states. So, these represent the conduction band and the valence band. So, within the conduction band and valence band will have extended states, but we will also have localized states within the band gap.

In the case of an amorphous semiconductor, we no longer talk about a band gap because we have all of these localized states. So, we call the distance between the conduction band and the valence band as a mobility gap. Now all these localized defect states can also take part in conduction, they can essentially trap the electrons and holes. So, in the case of an amorphous semiconductor, conduction takes place through a hopping mechanism where we think of the electrons and holes hopping through all of these localized defect states. So, this drastically brings down the mobility and hence the conductivity. If we have crystalline silicon, $\mu_e$ is usually around 1350 or 1400. On the other hand, $\mu_e$ for amorphous can be as low as 1. So, you can have a nearly 3 orders of difference in magnitude in the mobility in the case of amorphous and crystalline materials.

So, with this we are done with the electronic materials part of the course. So, we have looked at intrinsic and extrinsic semiconductors. Next we will look at the devices. And in devices, we will have to form junctions between these materials.

So, the next thing we will do is to look at junctions and that we will look starting from next class.