Electronic Materials, Devices and Fabrication
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Lecture – 29
Productivity and Process Yield

Last class, we saw about the various techniques that are available for process evaluation. We saw that, we have techniques for electrical measurement, techniques for physical measurement. These are usually the thickness of films, but, also lateral dimensions, especially in the case of lithography and also techniques for measuring the number of defects, and also the type and the distribution of defects. So, process evaluation is important because, we saw that at typical IC manufacturing, can take place in approximately a month's time and has 500 or more processes. So, we need know, where there the wafers which past to each of these processes are good enough, in order to go on to the next step. So, today, we are going to talk about process yield and also productivity of the IC manufacturing process.

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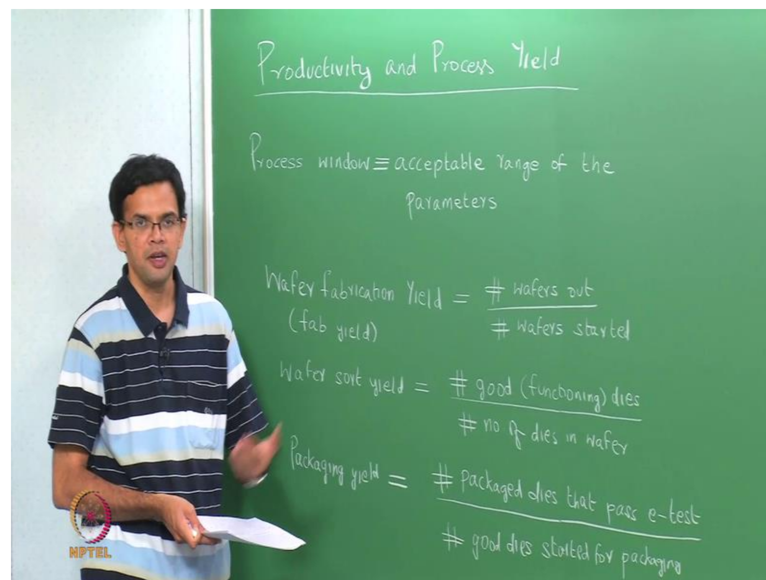

So, when we talked about last about process evaluation in last class, we saw that for each of the individual processes, we define some sort of a process window. So, the process window basically, defines the parameters test that there acceptable to that particular

process. For example, if you are looking at oxide growth, then the process window would essentially have the thickness of the oxide, that is, the range of thickness that are permitted and also the amount of defects.

So, the process window defines; the acceptable range of the parameters. So, semiconductor IC manufacturing is essentially a complex process. It is a series of processes, which are sequentially arrange one after the other, as a sort of assembly line. So, we start with a blank wafer and ultimately at the end of the process, we get a finished die or the finish chip. So, for this manufacturing, we usually define something called a process yield. And there are three main measurements of process yield.

So, the first one is called the wafer fabrication yield or fab yield. This is usually abbreviated as fab yield. So, this is the ratio of the number of wafers that come out of the fab after processing, to the number of blank wafers that start at the beginning of the fab process. So, this is the number of wafers out divided by the number of wafers there are started. We can also define something called a sort yield or a wafer sort yield, which is the number of good dies in a given wafer. When I say good die, it is essentially a functioning die. So, it passes the electrical testing. So, the number of good dies in the number of functioning dies divided by the total number of dies in the wafer. And then finally, we have something called a packaging yield, which is the number of package dies that past the electrical test. So, I will just abbreviate as e-test, but, e-test is nothing, but, electrical testing divided by the total number of good dies.

So, the overall yield in a fab, is the product of all three of this; the fabrication yield, the sort yield and the packaging yield. And this is closely related to the cost of the manufacturing. So, typically you want as high a yield as possible because, this again will lower the cost per individual die. So, today we are going to look into three of this in detail and some of the parameters that affect, the various yield values.

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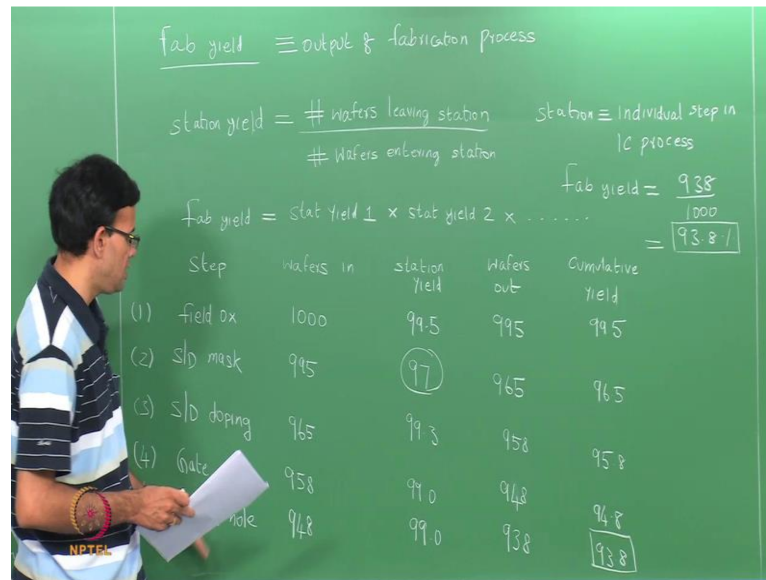

So, we will first start with looking at the wafer fabrication yield. So, I am going to abbreviate this as the fab yield and this gives the output of the overall fabrication process. If, you look at a fab, we saw that a fab is essentially like and assembly line. So, the blank wafers start and then go through each and every process and subsequently after all the process is done, they come out of the fab. So, we can call each and every step of the IC manufacturing process, as a station. And for each station or each step of the process, we can define a station yield.

So, the station yield again is nothing, but, the number of wafers leaving the station divided by the number of wafers that are entering the station. And when I talk about station, each and every step in the manufacturing process is called station. So, station just refers to the individual step in the manufacturing process. So, if he can define an yield for each and every step in the process and the fab yield is the overall yield of the overall output of the fabrication process, then the fab yield is nothing, but, the cumulative yield of all the individual stations.

So, the fab yield can be return as station yield 1, time station yield 2 and then this just goes on. So, to the overall yield, is the cumulative yield of the individual stations, which is why when we look at IC manufacturing, we want as higher station yield as possible

close to a 100 percent because, of the fact that the overall fab yield is a cumulative of all the individual station yields. So, we can consider this by taking a simple example. So, I have difference steps, I am going to start with 1000 wafers. For each step, we can define a station yield, which will tell you how many wafers come out. And finally, you have a cumulative yield.

So, right now will only consider a five step process, just to see how the cumulative yield depends upon the individuals' station yields. But, remember I typical IC fabrication, can have more than 500 processes so that, what we have in five steps, has been multiply by 100. So, may first step have will called to be the field ox, so formation of an oxide layer. So, initially I will start which say 1000 wafers, this station yield is 99.5 percent, which is nothing, but, the number of wafers leaving the station, by the number of wafers entering so that, the number of wafers at come out is 995.

The next step is forming this source and the drain mask. So, we start with 995 wafers because; remember this is an assembly line process. So, after the first step, the wafers that come out of the first step go to the next step, those at come out go to the next step and so on. So, we start with 995 wafers, your station evil is 97 percent to the wafers out is 965. So, already with just two steps we started with a 1000 wafers and we have essentially lost essentially 35 wafers, even though your individual station yields are much higher than 95 percent. Your third step is your source and the drain doping. So, you form the individual source and the drain reagents. So, we start with 965, 99.3 is your station yield, your output is 958.

The fourth step is gate ox. So, 958, 99 is your percent is your station and you have 938. And I will dried 1 more step and then stop there. So, this should be 948. And then contact hole, so start with 948. Again I will say 99 percent, overall yield is 938. So, we have just 5 steps in a fabrication process, is started off with 1000 wafers. And at the end of 5 steps, we have a essentially 938 wafers or you have lost proximately 62 wafers. We can define a cumulative yield, which is the product of the yield of each and individual step.

So, the cumulative yield; the first step is 99.5, then it is the product of these 2, which is

96.5, then the product of this 99.3. So, let me just right the numbers; 95.8, 94.8 and then 93.8. So, the overall cumulative yield after 5 steps is; 93.8, the fab yield is nothing, but, the number of wafers that come out, by the number of wafers that go end. So, if you look at the fab yield, again just 938, which is the wafers that come out, by the number of wafers at went in, which is again 93.8 percent.

So, what we see here are a couple of important points. The first is just your individual station yields are still pretty high. So, these are 99.5, 99.3, 99 99. The lowest 1 is for the formation of the mask, in that this still pretty high 97. So, even though the individual station yields are high, the overall yield because it is it cumulative process, is lower. Also if you increase the number of steps, the overall yield reduces because, once again it is a cumulative process.

So, with just 5 steps, he only get a yield of 93.8. So, if you half 500 steps, then the overall yield will be even lower, which is why in the case of IC manufacturing, which Involves so many processes. It is very essential that, each of the individual processes have a high yield, close to a 100 percent so that, the overall process has a high yield. We will next look at some of the processes or some of the issues that affect this station.

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So, factors affecting the fab. So, the fab yield is related to the yield of the individual stations so that, some of the factors which also affect the individual station yield. The first factor is the number of process steps. Again, as we saw earlier, more than number of process steps, lower is the overall yield. So, as the number of steps increases, the yield will reduce. For example, let a say you have a 50 step process and each step, so which is your station yield as a value of 99.5. So, each step has a yield of 99.5 percent, which means if 100 wafers come in or 1000 wafers come in, 995 wafers will come out. So, only 5 wafers are lost per individual step.

But, if you have 50 such steps, the overall fab yield individuals station is 0.995 times 50, which you just 0.755 or 75 percent fab yield. If instead of 50, we had 100 of process; the yield will be even lower. So, more the number of process steps, lower will be the yield. Unfortunately with reduce with reduction in the size of the individual circuits because, of devise miniaturization, a number of process steps actually increases as we go from 1 generation to the next.

So, having a high individual's station yield is important to get a overall good fab yield. Another factor that affects fab yield relates to wafer breakage and also warping. So, this is the related to the wafer handling inside the fab. So, these days, 12 inch wafers are used in a typical IC manufacturing process. The next extraction will go from 12 inch to 18 inch or you going from 300 millimeters to 450 millimeters.

So, the handling of these wafers which have pretty huge; is essentially entirely and automated process. Later even look at how the wafers move in a fab and will also look a look briefly, at the automation process in the fab. But, the overall handling is automated in order to prevent wafer breakage because, we have wafer breakage, 1 again you will lose these wafers. The number of wafers that come out will be lower and this again will affect the fab yield. Wafer warping is related to the change in dimension of the wafers, as it goes through 2 different heat treatment processes, especially processes like rapid thermal aniline, will as take the wafer to high temperature, in a short duration of time and also cool it faster. So, this can in use thermal stresses in the wafer and also cost a change in the dimension of the wafers. This is called the wafer warping.

So, once again this can affect the yield of the fab. So, wafer war page is very important, especially even dealing with heat treatment processes. The third factor is the process variation. So, in last class, when we looked at process evaluation, we define a process window for each process, which tells you the acceptable parameters that have possible for a particular process. So, if a process has a value that is beyond the range of these acceptable values, then once again in the process is set to have failed and then, the wafer a set to have failed at that particular process step, which will again affect the yield.

So, it is very important to set the proper limits for any process or the proper parameters for any process. This is called a spec limit. Spec is nothing, but, shorts for specification. So, this spec limit is set for each process, which tells you the acceptable range. For example, if you growing and oxide layer or a nitride layer or any other layer, thickness range would be an acceptable spec limit. Similarly, the maximum amount of defects at the permissible; would be another spec limit. So, the spec limits are too loose, so they are too wide. Once again they can cross cause a process to fail because; there will be a lot of variation. On the other hand, if the spec limit is too tight, the lot experiments would not they able to meet the spec limit and once again the wafer will.

So, setting the appropriate spec limit or the specification limit is important, when where looking at trying to get a higher yield. The next 1 relates to the process defects. These are essentially isolated defects there are cost during the process. So, this could be a related to the process steps or it could be a related to any contamination that arises from the process chamber and so on. So, these are isolated defects, either related to the process or to the equipment. Again to give an example, we can go back to the idea of oxide growth on a wafer. If there are some issues with the farness, so there is some sought contamination, then just contamination in again affect the wafers.

So, if you produces spec limit for the defect concentration, any contamination in the chamber can affect the defect limits and once again lead to the wafers being rejected. So, having a good maintenance or a good preventive maintenance of the equipment is essential, in order to reduce the number of process defects. It can also have defects there are related to the mask. This is especially related to lithography. So, these mask defects. So, these are essentially defects in the hard mask.

The hard mask contains the pattern; that is then transferred to each and every wafer. So, it typically defects could be something like a dust. Usually this is made of glass, so that could be cracks in the glass. You could have and damaged mask layer due to handling. All of this will again cost defects in the pattern, which will again to a lowering of the yield. So, it typically a mask is clean just before using at for transferring pattern on to the wave. So, cleaning the marks important because, remove some of the dust. And regular mask inspection is also carried out, in order to mask show no damages to the mask or no damages or cracks in the mask, which again affect the wafer.

So, these are some of varies factures it affect the fab yield. All of these have to be minimized, in order to get high fab yield. The next thing you going to look at is wave for shortly and some of the factors that affect short.

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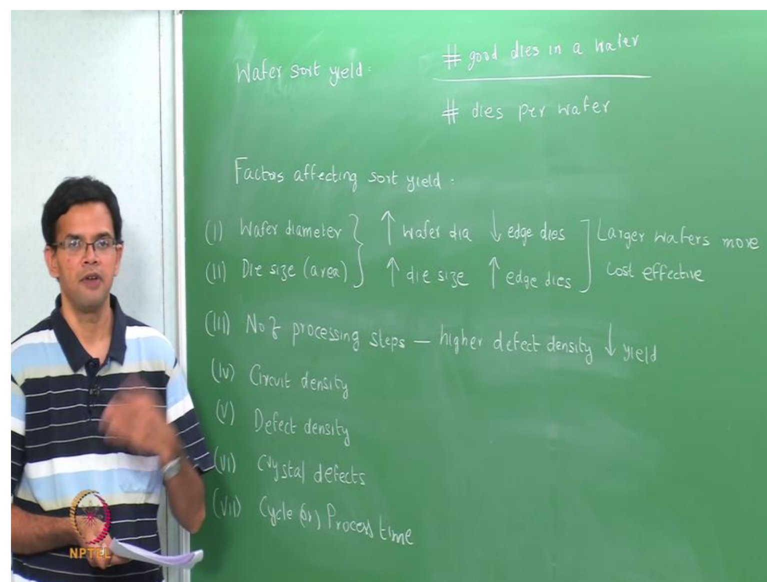

So, will look at the wave for sort yield next, we define wafer for short as the total number of good dies, in a wafer divided by the total number of dies per wafer. So, as a mentioned earlier, when a talk about good dies, these are dies that have electrical functionality so that, there pass some sort yield test or electrical test. So, factors that affecting the sort yield. The first 1 is a diameter of the wafer good and link to that is also the size of the die or area of the die. So, these 2 are sort of link. So, if think about it, as

we increase, the number also increases the size of the wafer. So, if we increase diameter of the wafer, the number of dies we need to also increase.

So, if you have more number of dies, then you overall wafer sort yield will be because, you have higher percentage of good dies and you also have less number of edge dies, partially complete and the ... So, increase wave for diameter to basically reduce the number of edge dies and again increase overall sort yield. So, the happen if increase the dies size. So, the increase size of individual die, which means number of edge dies will increase, which will need to lowering of the yield. So, these 2 sort works; 1 against the other so that, overall idea is to have larger wafers, which are more cost effective, which is why initially in the industries is started with 1 inch wafers, which finally, group and now you have 12 inch wafers, shall a being used. And the next generation will essentially have 18 inch wafers.

So, driving force behind using larger and larger wafers is, to reduce the number of edge dies and to increase overall sort yield. Again the next parameter is the number of processing steps. So, we seeing this earlier, in contacts of fab yield. So, same things; more the number of processing steps, you will have higher back ground density or higher defect density, which will again reduce the yield. Then, you have other parameters like the circuit density, defect density. So, any defects that present within the silicon, which can again affect process.

So, these are defect present even before, the wafer for enter the fact. So, this is during the manufacturing of the silicon wafer and also the cycle time or the process time. So, all of these are varies factors, affect the sort yield. So, again if you have larger cycle time, you can more contamination, which again affects the wafers. Circuit density you have higher circuit density, the individual component are closely, which means even smaller defects can essentially damage. And other things defect density crystal defects is; obviously, related to the sort yield. So, there are different models, which basically look and how all of these defects affect the fab yield.

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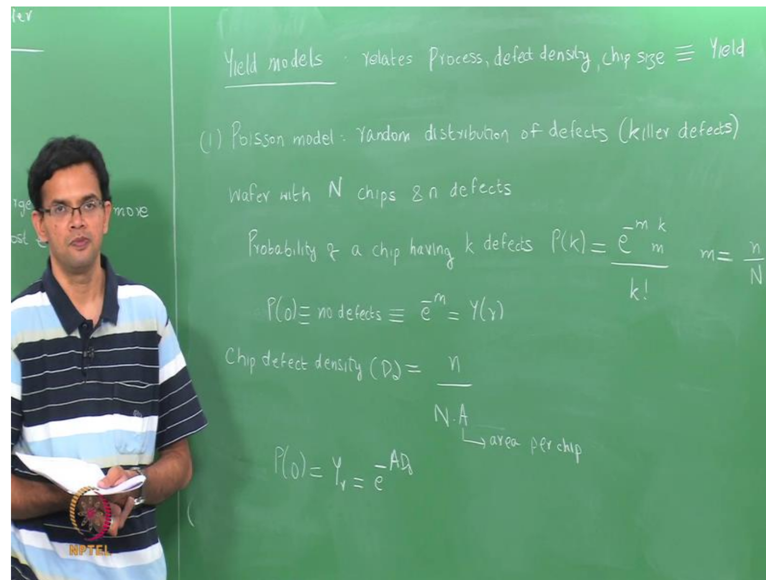

So, let as look some yield models there are currently. So, we will look at some of the yield models. Yield model basically relates the process. So, the number of processing, steps the defect density and chip size to the yield of process. So, varies parameters that essentially come from each steps to the overall yield of the process. The simplest yield model is a poison model. So, this assumes, you have random distribution of defects in the wafer. The defects we are talking here are essentially the killer defects. So, defects that can essentially damage the chip and make the chip not function. You can all have defects that non critical, there density will be typically higher than the killer defects, but, you will not focus on them because, they do not affect the yield of wafers.

So, we have random distribution of defects. Let us say you have wafer with N chips and n defects. Given these are randomly distributed, the probability of a chip having k defects. That is call this p of k is nothing, but, poison distribution even by e to the minus m mover k by k factorial, m is nothing, but, n. So, the probability of a chip with no defect; so p of 0 which is no defects, this is nothing, but, the yield because, we define yield as number of chips which are good and functioning to the total number of dies or total number of chips is nothing, but, e to the minus n. This is yield of the process.

So, instead of defining the total number of defects, you can define a chip defect density

D not is nothing, but, the number of defects divided by the total number of chips times A with A is the area perched. So, if e define a chip defect density D not, then p of 0 by the poison model which nothing, but, you yield is e to the minus A over D. So, yield again defines upon the area perched.

So, if you have larger chip area, it means we have larger die area; the yield is lower for the same density of defect on the surface. This is once again in the reason y you go for the larger wafers so that, the overall number of chips are higher. So, the poison model assumes random distribution of defects, but, that is something that is not always true.

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So, poison model assumes random defect distribution, but, in most cases defects are clusters, which means there are different models to accounts for this clustering. Another term used is called decoration. You say that defect decorate the surface. So, in that case, you define the yield as integral F of D e to the minus d and F of D refers to how the defect distributed in the wave, so distribution of defect density.

So, there are different models take in to account, different values of F of D, these give much more closer to reality. For example, you have Murphy's model, which assume triangular distribution so that, yield has the exponential function. You also have an

exponential yield model, where once again you have different distribution. So, according to this model, have some areas in the wafer, which have high density of defects, in some area that are not.

So, if you have high defect densities that are essentially restricted small areas sample. In that case, you yield essentially given square route of AD not. In this model called seeds model. There are some other models. For example, there again model which once again assume some other distribution of defects, it gives different value of yield. So, all of these assume non random distribution. But the overall common theme behind all of those is that, as a die area increases, that is, A increases; yield essentially drops.

So, if see 3 processes or 3 type of yield. 1 is the fab yield, than we have the sort yield finally, we have the packing yield. All 3 of them come together to overall yield. So, the overall yield is nothing, but, the fab yield times, the sort yield times, the packaging yield. So, we have look at parameter that effect yield. Yield is the 1 of the factors that those in to the overall cost of producing wafer. This tells you why the wafer fabrication is such capital. So, we look at the sum of cost associated wafer manufacture.

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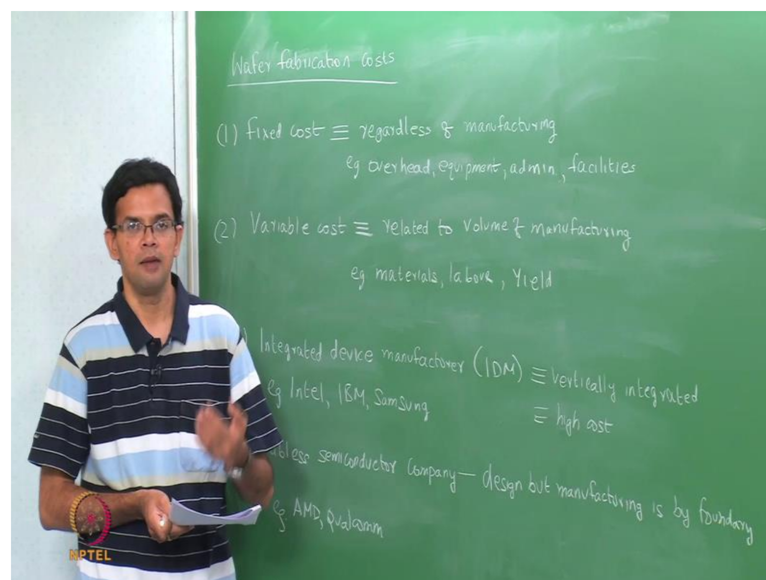

So, if you look at wave for fabrication cost, there overly mainly 2 main kinds of cost

factors. The first is called fixed cost. So, this is related to the presence of the over head; so administration facilities, any development and also equipment. Fixed costs are there, whether the wafers are manufactured or not. So, there regardless of manufacturing; so there not link to the volume of the manufacturing. Example of fixed cost overhead, any equipment that is purchased. So, whether the equipment is use or not, the purchasing cost is still be there, administration, then facility, building facility other things. All of these come in to the fixed cost.

The variable cost; these related to amount of materials, is related to volume of manufacture. So, more the number of wafer that produced, greater is the variable cost. Some example this are materials labor because, more the manufacturing is done, more the number of labor is required, which leads to greater cost. But, more importantly yield which show earlier, is related to the variable cost because, the lower the yield, which means we still have less number of wafers at come out and that will need to higher variable cost. Because of these different expenses, semiconductor manufacturing companies are essentially divided in 2 main models.

The first model is called integrated device manufacturer or IDM. So, these are vertically integrated companies that own all the steps, starting from the wafer fabrication to wafer sort to packaging to circuit design so on. Vertically integrated; so these companies are essentially high overall cost because, own all the equipment and also all the facilities for doing the research and also the manufacturing. So, an example of the IDM; most famous example off curse INTEL, but, you also have companies like IBM and Samsung. So, for these companies at high volume of a production, with high yield is essential, in order to offset the high cost.

The second kind of company is Fables; semiconductor company. So, these companies that make the circuit design, but, then the chip manufacturing is done by in other company. So, the outsource chip manufacturing to foundry. So, do the design, but, manufacturing is done by foundry. Examples of Fables Company include AMD, QUALCOMM. So, the advantage of these companies is that, the cost is lower, but, then the disadvantages that process is basically define by the foundry or the technology of the foundry to which essentially outsource the job.

So, of the foundry is based on a 32 nanometer technology. The final products we also be based on 32 nanometer technology. So, the technology is limited by the capabilities of the foundry company. So, the yield that we show before essentially enters in to the overall cost of the final wafer. So, we want high yield, in order to ensure lower cost for the individual wafers.

So, today we are look at an example process yield and also how the yield affects productivity. In the next class, we will look at the cline room designs and also how to minimize contamination inside a cline room, or why we need cline room, in order to do semiconductor manufacture.