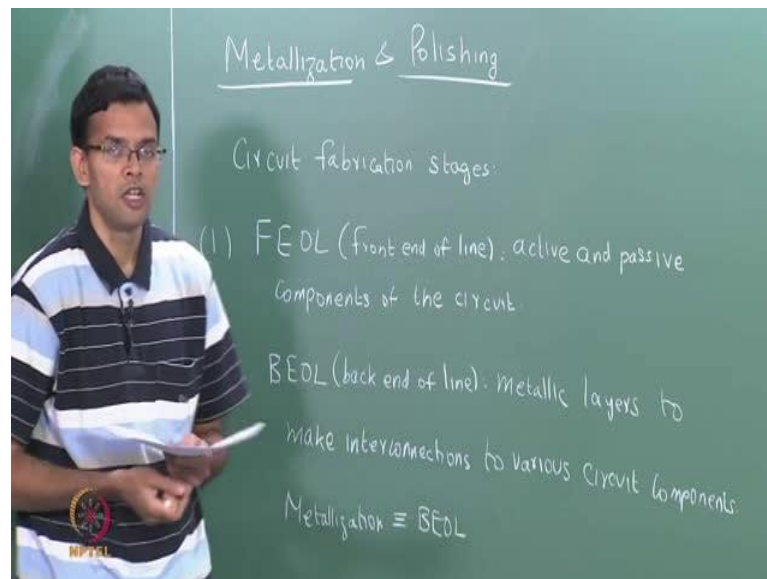


Electronics Materials, Devices and Fabrication
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Lecture - 27
Metallization and Polishing

Last class, we looked 2 of the process in the IC fabrication. We first looked at etching; which is a technique for removal of material; we found that we could combine etching with the lithography or patterning, to selectively remove material from certain places in the wafer. So, etching we found, could be done either by a wet process which is your wet etching or by a dry etching. We also looked at the opposite of the etching process, which is the growth process, where we add material to the wafer. So, we mainly focused on growth, by a chemical vapor deposition process. Today, we are going to continue to look at growth process. We are going to look at formation of metal layers.

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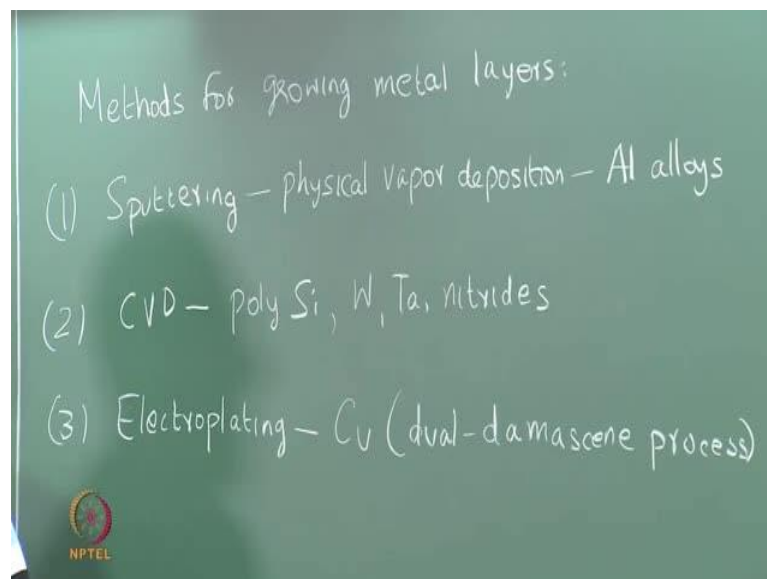
This process is called a metallization. Along with metallization, we will also look at polishing, where we remove excess material in order to give a smooth finish and remove surface roughness. So, today we are going to focus on two techniques; one is metallization, the other is polishing. So, before we do that, we said that IC fabrication essentially acts like an assembly line. You start with a blank wafer; the wafer goes through a series of processes and steps. So, and then gives you the final IC product. So, this circuit fabrication is normally divided into two big stages.

The first one is called the front end of the line or FEOL. So, this usually refers to the processes that are used, to generate the active and the passive components of the circuit; so, the transistors, the resistors, the diodes and so on. So active and passive components of the circuit. The next one is called the back end of the line or BEOL. So, while the front end of the line; all the device components are manufactured, these components have to be connected to each other and also to the outside circuit. So, this interconnection is done in the back end.

So, metallic layers to make the interconnections to the various circuit components. So, later, we will see that, there is also a contamination reason, by processes are divided into front end and the back end. Now metallization process is mostly related to the back end processing. It is defined as the wiring of the different circuit components, to get a functioning circuit. Now if, you remember, the original IC device that was manufactured by Jack Kelby; essentially had external wiring. So, the wiring was not part of the IC circuit. But, in the first modification that was done the wiring, was made part of the IC circuit and aluminum was the material that was used for doing the wiring.

Now, common methods for growing these metal layers and to your IC circuit; there are normally physical vapor deposition techniques.

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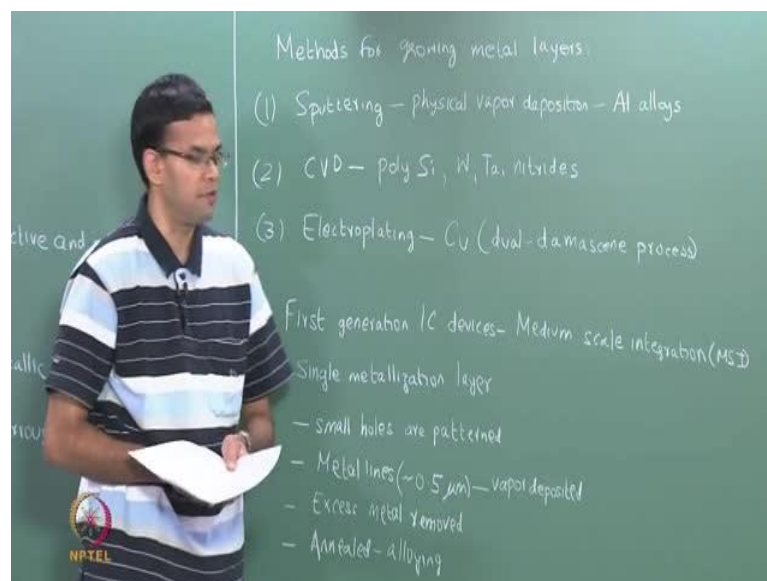


So, the methods for growing metal layers; 1 technique is called sputtering and we will see what this means later. So, sputtering is an example of a physical vapor deposition

process, mainly used for aluminum alloys and it is also used for growing the copper seed layers, which are used for electroplating. Another technique is chemical vapor deposition. We already saw CVD last time, we again used it for growing layers like silicon dioxide or nitrides or dielectrics, but, CVD is also used in metallization. It is usually used for example, say you want to grow poly silicon for a gate for materials like; tungsten, tantalum, nitrides and so on. And then finally, electroplating; it is mainly used for copper. So, for doing copper metallization, for growing the copper layers, electroplating process is used.

The whole idea of copper electroplating and copper metallization is called a dual damascene process. And again we will see what this process means. So, if you looked at the first generation of IC circuits, usually there was 1 layer of metals that was added or 1 layer of metallization that was carried out.

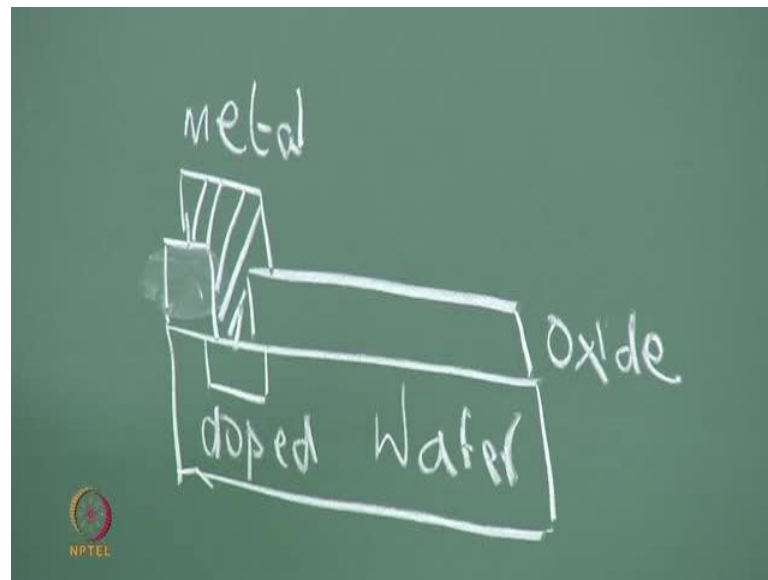
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So, the first generation devices; there was usually a few 100 components per device. So, it is an example of a medium scale integration; MSI. So, you essentially had a single layer of metallization. So, in this process, small holes, these are called contact holes are first patterned on to the wafers, usually using a mask and there will be in oxide pacification layer. So, small holes are patterned, metal lines approximately 0.5 microns thick or 500 nano meters, where vapor deposited.

So, aluminum was the material that was used for the first generation of IC devices. So, it is possible to vapor deposit aluminum, usually you can use thermal evaporation or sputtering. After this the excess metal was removed along with the photo resist. And then finally, the system was annealed, for alloying to generate good interfaces.

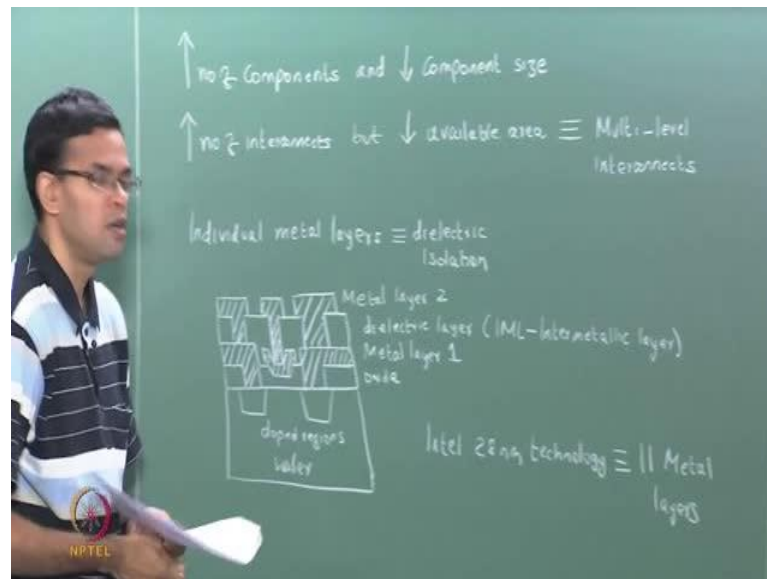
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So, if you want to depict this; say we have a wafer, with a certain doped region. So, we want to make contacts to this doped region. So, in this case, you had an oxide layer, just erase this, you had an oxide layer and then a metal layer. So, you start off with a wafer which has a doped region, there is a uniform oxide layer that acts as passivation. So, the oxide layer is patterned, in order to open a small hole. Metal is then deposited, so you have excess metal everywhere. Remaining excess metal is then removed along with the photo resist, to leave behind the metal plug. And then usually some sort of annealing is carried out, to better develop the metal wafer interface.

So, in the first layer of IC device, in the first generation of IC devices, metallization was essentially a single layer. So, you can think of this as being replicated, throughout the entire wafer. Now what happens as we have an increase in component size is that, the different higher generations of IC devices, we essentially had greater integration. So, you went from medium scale to large scale, to very large scale integration and so on.

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So, the individual component sizes reduced. At the same time the number of components increased. So, the number of components increased and at the same time the component sizes reduced. So, these meant, that because you have more number of components, you needed to make more number of connections. So, the number of interconnects increased, but, the available area to make these interconnects reduce, which means; we have to make more number of wiring, but, the area of amount available is smaller. So, 1 way to this is to of course, reduce the size of the wires. So, you make the interconnects smaller and smaller, but, even that will not be enough because, of the large increase in the number of components.

So, a typical component device now has anywhere around 10 to the 7, so on 10 billion components. So, to overcome this, interconnects essentially became layer. So, instead of having a single layer of interconnects, it lead to the formation of multi level or multi layer of interconnects. Again in the case of multi level interconnects, you had individual layers of metals that were connected to 1 another and there were then isolated, by using dielectric materials. Individual metal layers with a dielectric isolation.

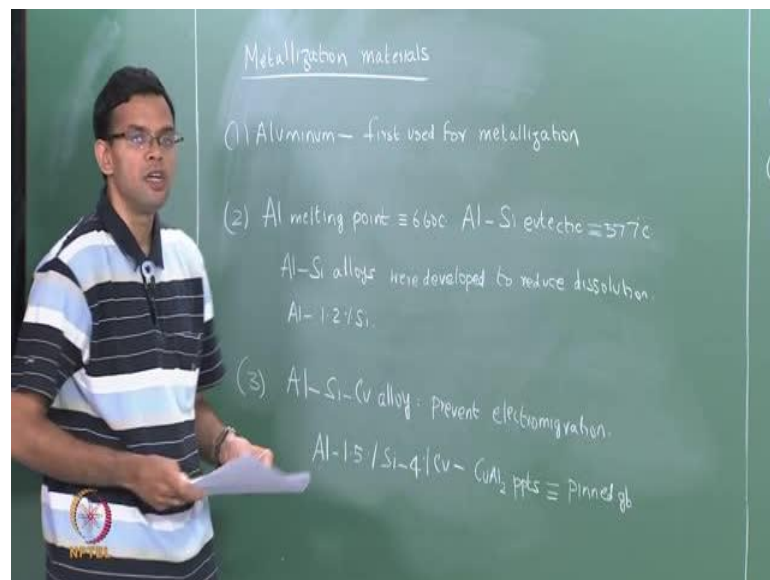
So, let me just draw a brief example of a 2 layer interconnection scheme. So, I will just draw this bigger. So, now, we have the wafer, with 2 doped regions. So, this could be an example of a simple transistor. So, again we can use an oxide layer for pacification. So, now we have the first layer of metals. So, the shaded region represents the first metal layer; metal layer 1. So, if you think of this as your simple MOSFET. You have a source

and a drain and then you have a oxide layer and then you have a gate and you make connections to the source the drain and the gate.

So, we can build upon this by having another layer of metal. So, we again have dielectric layer. So, this is the dielectric layer. This dielectric layer is usually called the inter metallic dielectric layer. Inter metallic layer because, it separates 2 metal layers. And then, you have another layer of metal on top, this becomes metal layer 2. Again it is possible to make electrical connections between these metal layers. So, in this particular example, I have just shown 1 MOSFET. You have a large numbers of these MOSFET's. Again interconnections can be made between these different layers.

So, as device complexity increase, you can basically end up building more number of these metal layers. So, if you look at it, the current 28 nano meter technology has essentially 11 layers of metals or 11 metallization layers. So, we are seeing that, with increasing in device complexity, we essentially end up building a large number of these metal layers. There is also been an evolution, in the kinds of materials that have been used, to make these interconnections.

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So, what are some of the metallization materials that have been used? So, the original material that was used for forming the metal layers was aluminum. So, in the IC circuit that was developed by Robert Royce; aluminum was vapor deposited on to the circuit, in order to make the metal connections. So, some of the advantages of aluminum is that, it

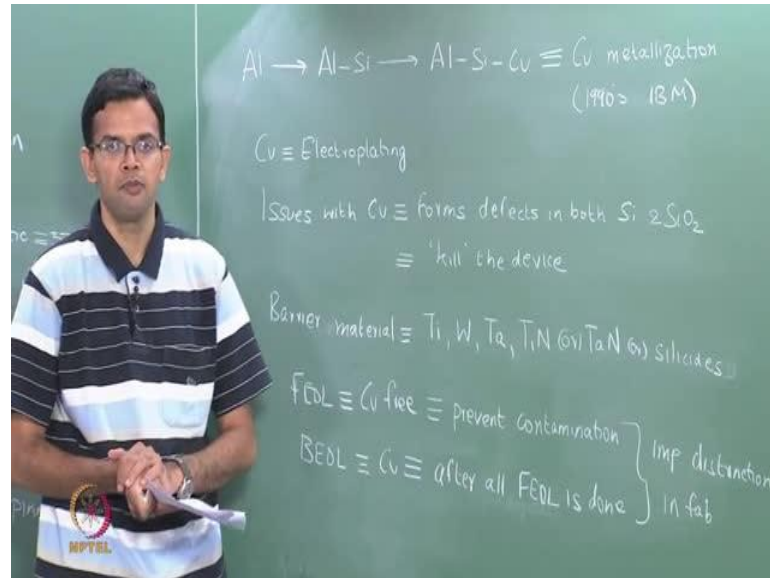
is easy to vapor deposit. It forms a good bond with the silicon dioxide first. Silicon dioxide is used, in order to pattern the sub straight in open contact holes.

Aluminum also has low contact resistance. So, by annealing the circuit it can form a good contact with silicon and it is also easy to pattern. 1 of the drawbacks of aluminum though is that, aluminum has low melting point. So, aluminum melting point is typically 660 degrees. But along with silicon, if you look at the aluminum silicon phase diagram, it forms a eutectic and the eutectic has a even lower melting point, so around 570 degrees. So, aluminum silicon eutectic is around 577 degrees. So, pure aluminum, when it was used as a metallization layer, essentially tended to dissolve into the silicon and this will lead to loss of contact resistance. So, aluminum silicon alloys were developed to reduce this dissolution. So, typically aluminum with 1.2 percent silicon was used.

Now as the device dimensions reduced and you have more number of components, the dimensions of the individual metallic layers also reduced. So, this means the thickness and also the width and the height of these metal layers, also became smaller. So, this led to the problem of electro migration. So, what happens in electro migration is that, you have atoms which start to move under the application of an electric field. Also because you had thinner wires, you also had higher resistance, which means there was greater heating. So, $I^2 R$ heating is higher, which again lead to movement of material. So, this is especially problematic in the case of aluminum, which has a low melting point.

So, these electro migrations again lead to cases where, the wiring failed leading to open circuits. In order to prevent this, the next layer of material was developed was based on an aluminum, silicon and copper alloy. So, this was developed to prevent electro migration as used. So, a typical alloy composition was aluminum with 1.5 percent silicon, and 4 percent copper. So, in this particular case, the aluminum and the copper formed Cu_2Al_3 precipitates which essentially; thinned the grained boundaries, and reduced electro migration.

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Finally now, aluminum is totally dispensed and we have pure copper is used as a metallization layer. So, if you look at the development of materials that were used for metallization, we first started with aluminum. Aluminum gave rise to aluminum silicon and this is to prevent the dissolution of aluminum within the silicon. This in turn went to aluminum silicon and copper. Copper was added to prevent electro migration of the aluminum which caused open circuits. And now finally, we have copper metallization. This was a process that was started in the 1990s, typically by IBM, but, now it is essentially the industry standard. And copper is the material that is used for forming all the metal layers; pure copper.

So, copper is usually grown by electroplating process. We will see the electroplating process later on. But, one of the biggest problem with copper is that, copper can diffuse into both silicon and silicon dioxide and essentially from deep leveled effects. So, 1 of the issues with copper is that, it forms defects in both silicon and silicon dioxide. This can essentially kill the device. What we mean of course, is that, the device loses this functionality so that, copper will essentially kill or poison the device.

So, even though we use copper for metallization, usually some sort of a barrier layer is added to separate the copper from the wafer. So, some barrier material is used. Typically materials based on titanium, tungsten, tantalum. So, these could also be nitrides like titanium nitride or tantalum nitride or even silicides are all used. So, these are essentially used to form the initial electrical contact. And then copper is first vapor deposited and

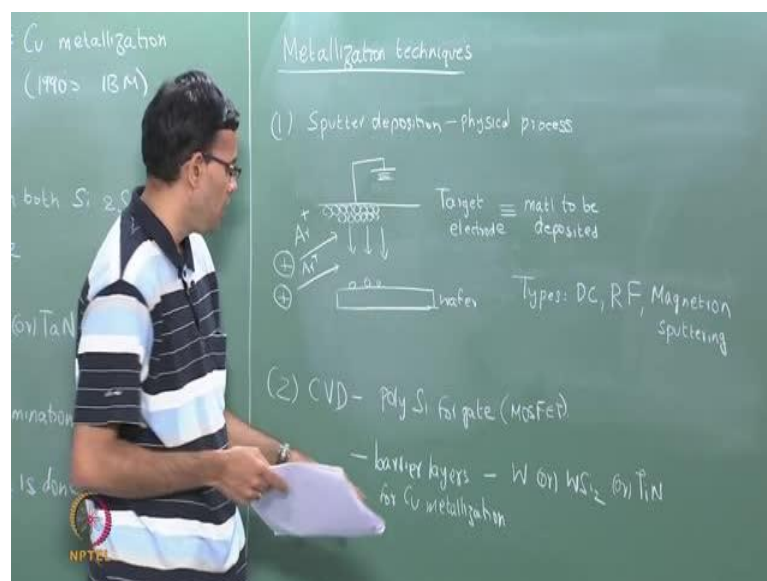
then electro plated on top of it. So, this is another reason where all the IC fabrication processes are divided into front end and back end.

So, we saw that the front end processes are essentially copper free so that, no copper is introduced into the device at any of this stage. This is to prevent copper contamination. The back end of the line is where the metallization is carried out. So, here you have copper. And whatever happens at the back end, the vapors never go to the front end processes. So, all the front end processes are carried out first, before going to the back end where copper is introduced. So, this distinction is maintained very carefully in the fab, to prevent contamination with copper.

So, for example if, there is any down time, in any of the equipment that is used in the back end, tools that are used for repairing the equipment; will not be used for repairing any of the tools that are used in the front end. This is because, those tools could be contaminated with copper and that again can introduce copper contamination in the front end. So, this is a very important distinction between these 2 types of tools, in any operating fab.

Similarly, any tools that are used for back end processes will not be used for growing wafers for the front end. So, we have looked at some of the different materials, which are used for metallization. So, let us now look at some of the metallization techniques.

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So, the first technique we are going to look at is sputtering or sputter deposition. So, this is a physical vapor deposition process. It is mainly used for growing both metals and alloys. But, generally sputtering can also be used for growing dielectrics, oxides compounds and so on. So, in this particular case, we just draw a brief schematic. The material that we want to sputter or to want to be deposited is made as the target electrode. So, this essentially consists of atoms. So, I will just show some of these atoms on the electrode. This is taken in a evacuated chamber and then argon ions are bombarded on to the target.

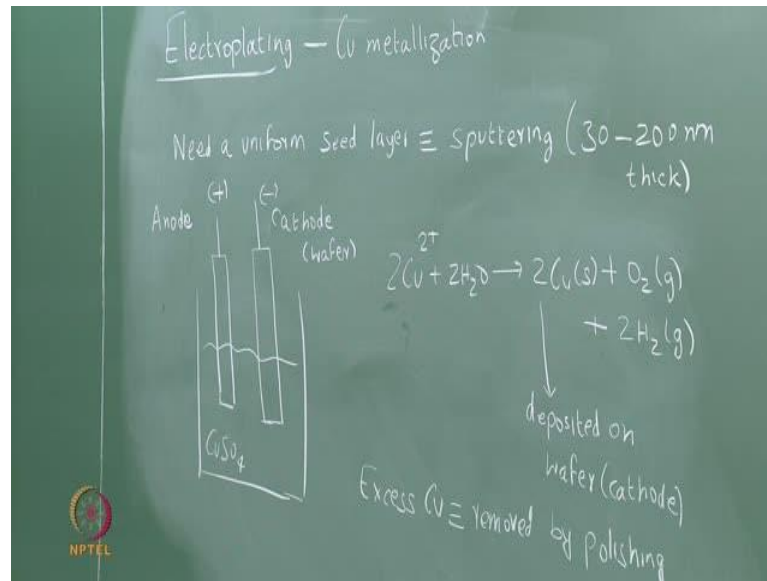
So, in this process, the argon ions physically remove the atoms from the target material, these are then accelerated on to the wafer and then in pinch on the wafer. So, this is essentially a line of side process so that, the wafer sees the atoms that are not out from the target, using the argon ions. So, there are different techniques in the case of sputtering. So, sputtering techniques or types. 1 crosses your DC sputtering. You also have something called RF or radio frequency sputtering. Last 1 is called magnetron sputtering.

Sputtering is usually done in a vacuum chamber at low pressure, where argon ions are used to sputter. Sometimes you can also have reactive sputtering, where a reactive gas is used so that, not only material removal takes place, but, the material that is removed reacts with the gas to form compounds. For example, oxygen can be used in order to form oxide layers, boron can be used to form borides, nitrogen to form nitrides and so on.

The next process is CVD; chemical vapor deposition. You have again seen CVD in last class. So, for example, you can use CVD to grow the poly silicon for the gate, this is in the case of a MOSFET. CVD is also used especially for growing the barrier layers that separate the copper from the metal. So, this could be your tungsten or you could have tungsten reacting with silicon to form tungsten silicide, titanium nitride or so on. CVD is especially used when you have to fill regions with high aspect ratios.

So, for example, if you had a trench, we will see an example of a trench later. And a very thin barrier layer has to be grown in the trench, with the correct aspect ratio, CVD process is used. The third process for metallization is electroplating and it is mainly used for growing the copper layers.

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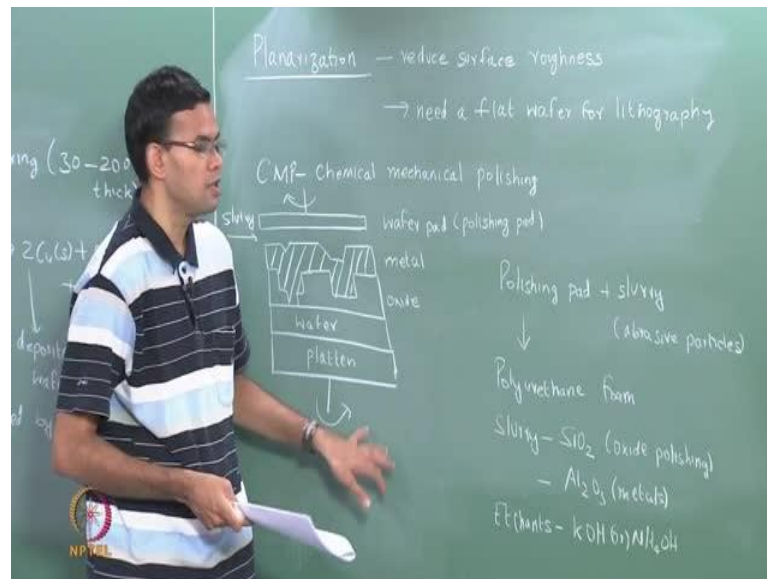


So, in the case of electroplating, it is used for copper metallization. So, initially a seed layer of copper is first grown. So, this seed layer is usually grown by sputtering, initially grown by sputtering. This is typically around 30 to maybe 200 nano meters thick. So, in the case of electroplating, the wafer is taken in a bath. So, bath of copper sulfate. The wafer forms the anode, the wafer forms the cathode. And there is also an anode, which is your counter electrode. During the electroplating process, the copper 2 plus that is present in the solution, gets reduced and forms metallic copper. So, the copper in the copper sulfate gets reduced to form metallic copper. And this gets deposited and the anode, which is the wafer gets deposited on the wafer, it is the cathode. So, once again it is a process where copper deposition takes place.

The advantage of electroplating is that, it is a low temperature process. Can be carried out at room temperature, so that, once the barrier is grown, the copper layer can be electro plated directly onto the wafer. The excess copper is usually removed by a process called polishing. So, this polishing process is usually called planarization. It is not only restricted to copper, it is usually used in the IC fabrication to remove excess material and to minimize the surface roughness.

So, let us look briefly at the planarization process next.

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So, planarization is an important process in IC fabrication, especially when we come to patterning because, planarization is used to reduce the surface roughness and this is especially important, when we are trying to pattern multiple layers. This is because; we need a flat surface for photolithography so that, we can align the different mask, we have multi layer lithography. Need a flat wafer for lithography.

So, in the case of planarization, another name for this technique is called CMP, just chemical mechanical polishing. So, in this particular case, the wafer is mounted on a platen. In this particular example, the wafer has some oxide layers. This is the oxide layer. And exaggerating the thicknesses here, the oxide layer is usually much thinner than the thickness of the wafer. This is just to show the process, maybe with some metal layer on top. So, here I have a wafer with oxide layer and some metal layer on top. So, this metal layer could have been grown by sputtering or CVD or even by electroplating, but, this metal layer is not flat. So, if you want to do another patterning and another metal layer on top, we first need to make this flat. And this is done by a polishing technique.

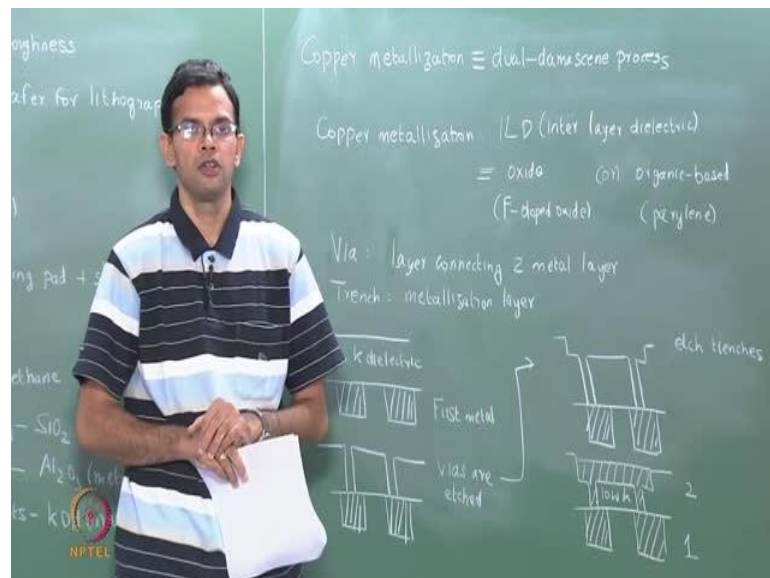
So, a wafer pad is used. The wafer pad rotates in 1 direction and the platen rotates in the opposite direction. Another name for this pad is called the polishing pad. Usually some sort of slurry is also fed into the system. So, the slurry consists of abrasive particles that can essentially remove the metal. At the same time, it will also help in giving you a smooth finish.

So, we have a mixture of polishing pad plus the slurry. And the slurry contains some abrasive particles. So, the type of slurry depends upon the layer you want to remove. So, the polishing pad is made of poly urethane, slurry for removing oxides usually SiO_2 is used for oxide polishing, alumina is used for metals and then you can also use etchants like KOH or NH_4OH .

So, this process is called chemical mechanical polishing because, you have mechanical removal of material by the slurry. At the same time, the slurry material is chosen in such a way that, it chemically reacts with the layer that needs to be removed and helps in increasing the removal rate. So, you have both mechanical polishing and chemical reaction. So, it is called CMP. So, planarization is combined along with copper metallization, to create the metallic layers. This process is called dual damascene process.

So, let us look at that briefly. So, as I mentioned earlier, copper metallization was introduced in the 1990, was originally introduced in the IBM and then became an industry white standard. Copper essentially replaced the aluminum silicon and copper alloy that was used for metallization earlier.

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So, the copper metallization process is called a dual damascene process. So, this has an interesting historical connotation because, the damascene process was originally introduced in the middle ages, as a process for growing, for generating very good metal

inlays; mainly for decorative purpose. So, this process was originally supposed to have evolved, in the Middle East somewhere near Syria, maybe in Damascus. This could be the reason for the name of the damascene process.

So, in the case of the dual damascene process, the first layer of metallization is formed. So, this could be a copper, separated by some barrier layer and inter layer dielectric is then grown on top and then the next metallization layer is formed and so on. So, in the case of copper metallization, this inter layer dielectric called ILD, is usually some sort of oxide. Originally silicon dioxide was used as the dielectric material, but, it has a high K. So, low K dielectric materials were essentially used.

So, usually some sort of a fluorine doped oxide is used. Organic based dielectrics can also be used as a dielectric. Example is parylene. So, the dielectric layer is usually chemical vapor deposited or it can even be spun on directly onto the metal layer. So, when we look at patterning, using the copper metal layer, we have 2 terms that we need to keep in mind. 1 is called a via; a via refers to the layer that connects 2 metallization layers. Then the other is a trench. The trench refers to the metallization layer, which are trying to pattern.

So, in the dual damascene process, both the via and the trench are grown simultaneously. So, to start with, the first layer of metallization is grown. So, we are going to say that, we already have the first metal layer. So, a low K dielectric material is then deposited on top of it. So, this could be grown by CVD process or by spin on. So, then the via's are first etched. So, this is called a via first process. So, the via's are etched. You can also have a process, where you first etch the trench, but, here it is a via first process. This in turn leads to a process, where you etch the trenches. So, you have etched the via, then you etch the trenches. Then the second layer of metallization is carried out. So, both the via and the trench are filled at the same time. The excess metal is removed by chemical mechanical polishing, to give the final 2 layer metallization.

So, this is layer 1. That is layer 2. That is the low K dielectric. So, this process can be repeated to build a subsequent layer. So, this is an example of a dual damascene process, where the via's are first etched. You could have a similar process, where the trench is first etched and then the via's are etched. So, so far we have looked at, all the various

steps that are involved in the fabrication of your IC device. You start with a blank wafer; then you go through these series of steps, to give you the final product.

The next class, we are going to look at how we actually evaluate the process. So, what are the various ways and we can measure the process at various stages, in order to make sure that, everything is proceeding correctly.