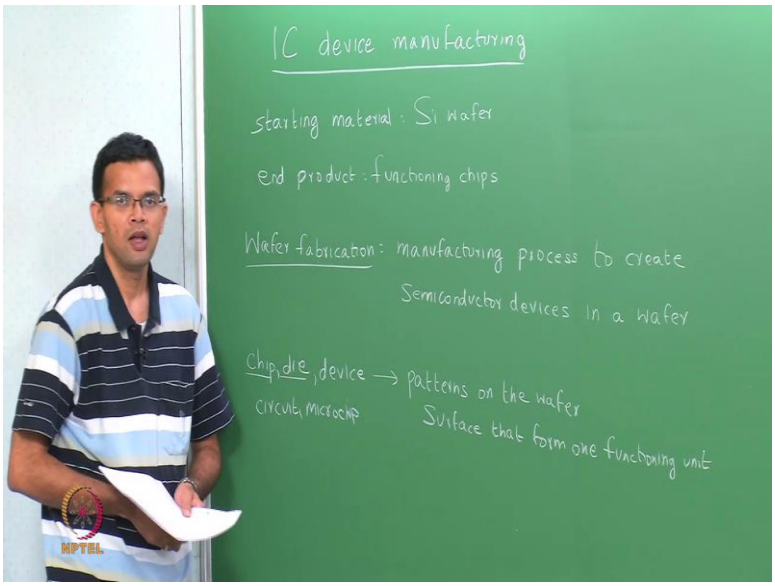
Electronic Materials, Devices And Fabrication
Prof. Dr. S. Parasuraman
Department Of Metallurgical And Materials Engineering
Indian Institute Of Technology, Madras

Lecture - 22
Ic Device Manufacturing: Overview

Last class, we looked at how to get a black or a bare silicon wafer starting from the ore which is quartzite. We first saw that we produce the quartzite to get something called metallurgical great silicon, which is around 98 percent pure. We further, purify the metallurgical great silicon to get electronic great silicon, which is has the purity of required silicon wafer, but is polycrystalline. We also saw that, they are two techniques; 1 is Charles k growl technique and the other is the float zone technique which is used in order to get single crystal silicon wafers.

(Refer Slide Time: 01:02)

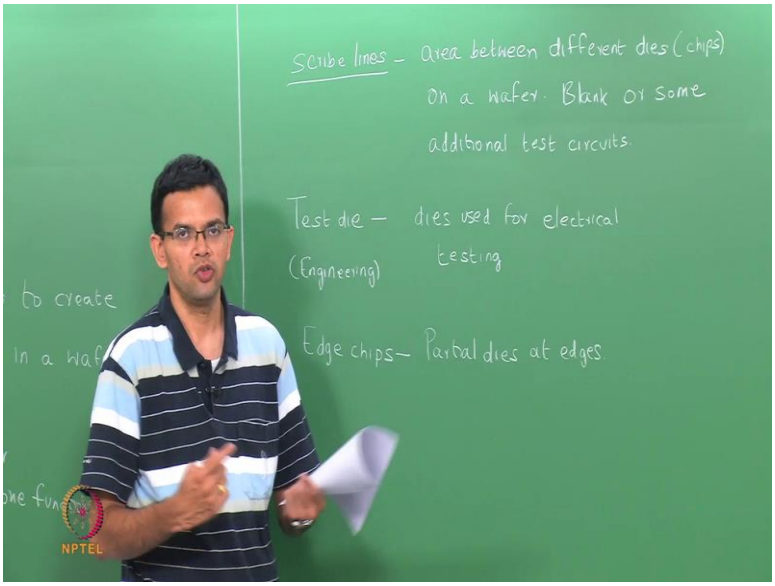


Today, we are going to look at an overview on IC device manufacturing or IC device patterning. So, the starting material for the IC device manufacturing is the silicon wafer which is what we ended up in last class, this is just the bare silicon wafer in the final configuration that we want, the end product is a silicon wafer containing the functioning chips, which are then separated out and package into the final product. So, this series of steps which start from your bare wafer and give you a functioning chip is the wafer

fabrication process.

So, we can define wafer fabrication as a manufacturing process to create semi conductor devices in a wafer search. So, today we are going to look at a overview of the wafer fabrication process and then in the next few classes, we looked in detail at some of the individual steps, but we before to go to the overview like to look at some definitions. The first definition is that of a chip or a die other common words there are used is a device a circuit or a micro chip.

(Refer Slide Time: 04:32)

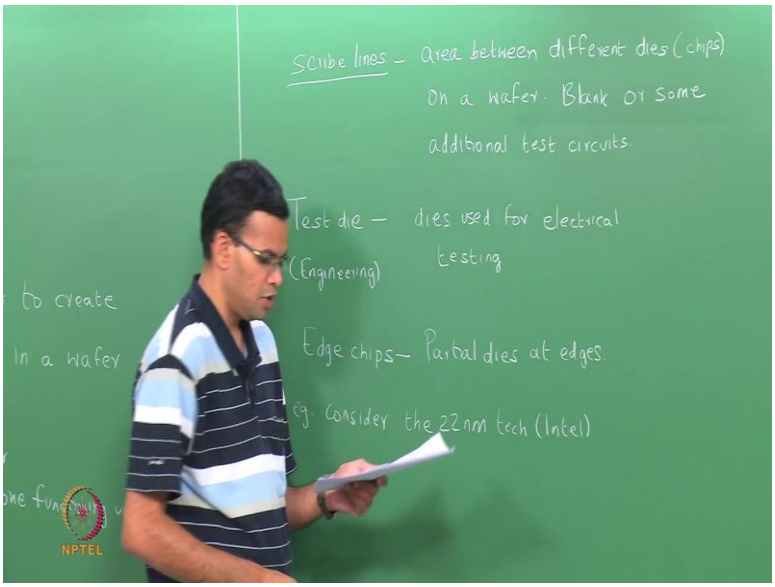


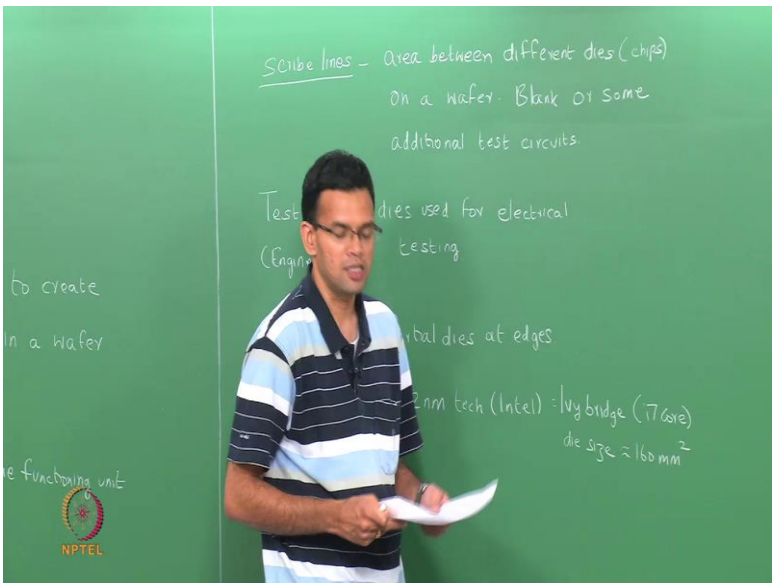
So, all of these refers to patterns on the wafer surface that form 1 functioning unit out of these chip and die are the words which are most commonly used at die is especially used. In the context of a fab scribe lines another term. So, this refers to the areas between the different chips or dies on a given wafer. So, a wafer is made up of a large number of dies. So, they are of the space between them is called the scribe line no the scribe line can be blank or may also have some additional circuits to the especially used for testing. So, thin be blank, but more often and not, but have some additional circuits for testing; apart from the die, you also have things that are called the test die.

So, the die originally refers to the product which is which finished and which has to be

marketed, but after along with those dies which are a product dies you may also have things there are called test dies or engineering dies. These are again incorporated in the wafer and these are dies used for electrical testing. So, this is especially useful when you are looking at a product control or process control. You also have something called edge chips, the idea being that any wafer sub proximately circular except for the plats, the dies are usually square or rectangle. So, that you will always have some amount of partial dies or partial chips at the edges, these partial dies are essentially called your edge chips.

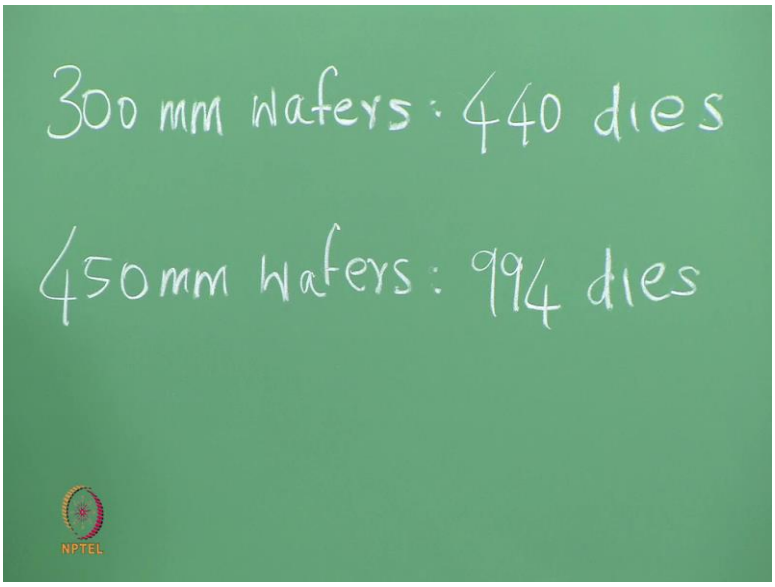
(Refer Slide Time: 07:27)





So, with increase in die size will be greater number of this edge chips and 1 way to minimize that is to increase the size of the wafer, give you an example consider the 22 nanometer technology for inlet. So, this is called Iv Bridge which is the code name which forms your i7 processors. So, i7 core there are a bunch of dies here with different sizes, but a typical die size is approximately 160 millimeter square.

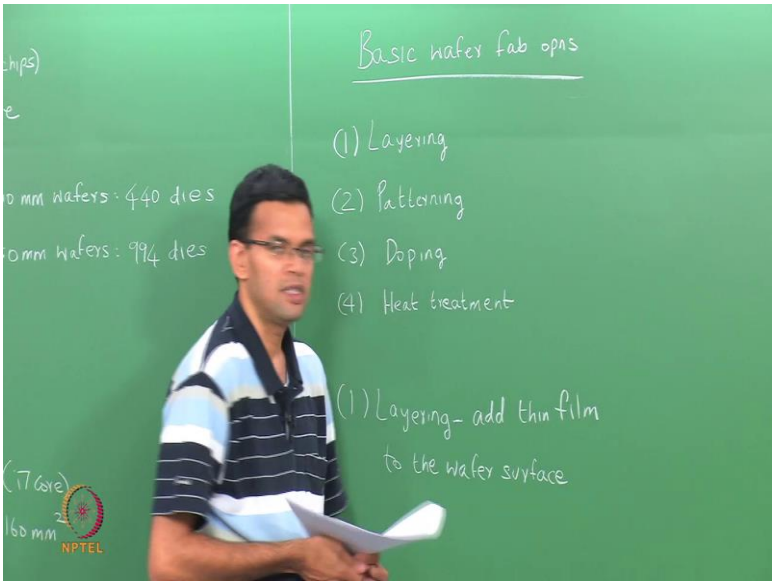
(Refer Slide Time: 08:19)



So, if you manufacturing these chips on a wafer then each die has an area of around 160 millimeters. So, here going to use 300 millimeter, wafer 300 refers to the diameter of the wafer; you can calculate the area and dividing by the die size. You find that, you can approximately make 440 dies. So, this just assumes that, you have dies that are spread through the wafer in you dividing the area of the wafer by the area of the die on the other hand, if you make these same dies on a 450 millimeter wafer.

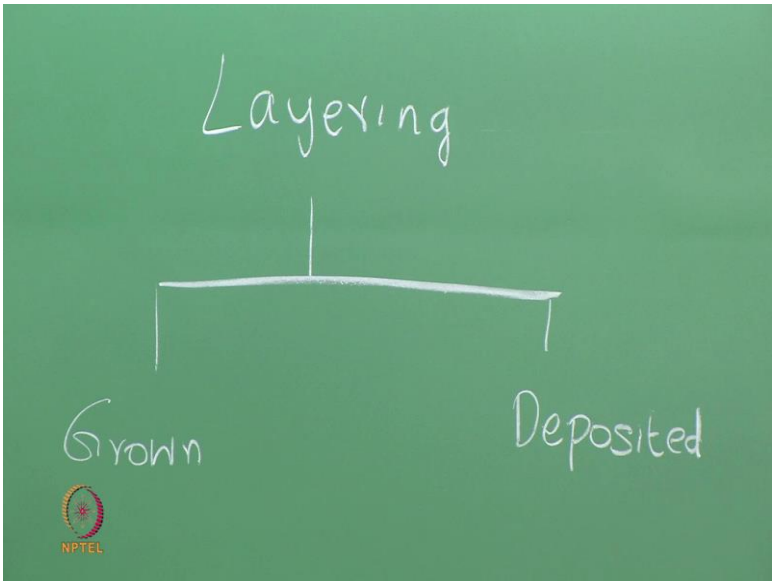
So, this 1 is the 12 inch 300 is a 12 inch, 450 is the 18 inch, then you have possibility of making 994 dies because some of these dies will be edge dies or edge chips and may not be fully formed or only partial, but you can increase the number of dies of a given size by increasing the overall size of the wafer. So, let us look at some of the basic fab operations there are in use, these can be separated into different categories. So, I will just looked at 1 particular classification for divide the fab operations into 4 major categories

(Refer Slide Time: 09:44)

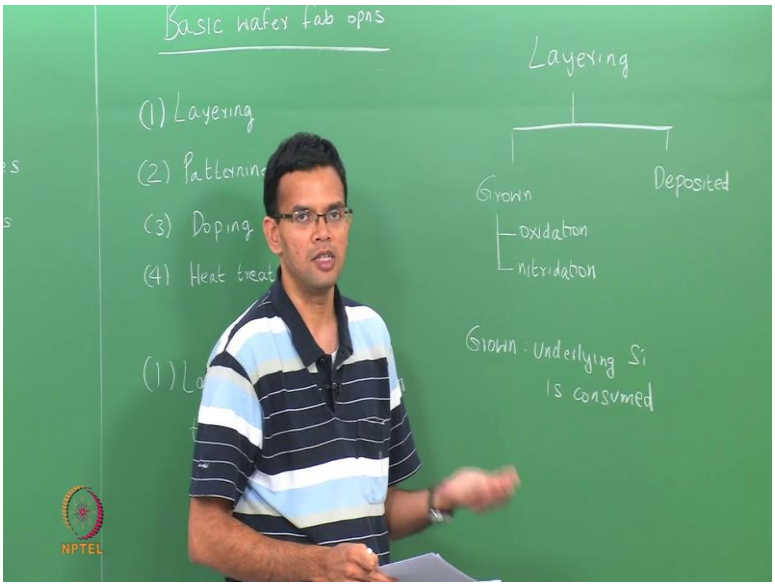


So, the basic wafer fab operations they can be divided into 4 categories. The first 1 is called layering and we look at each of them today, then we have patterning doping and heat treatment. So, these are 4 broad categories into which, you can divide your fab operations. If you think of your fab as an assembly line, then your wafer go through each and every step in sort of an assembly line process and you can have different combinations of this you could have a layering step, followed by a patterning step, followed by a say heat treatment and then doping and then layering and so on. So, today will look briefly at each of these techniques and the subsequent classes we will also look at them in detail.

(Refer Slide Time: 11:48)



(Refer Slide Time: 12:23)

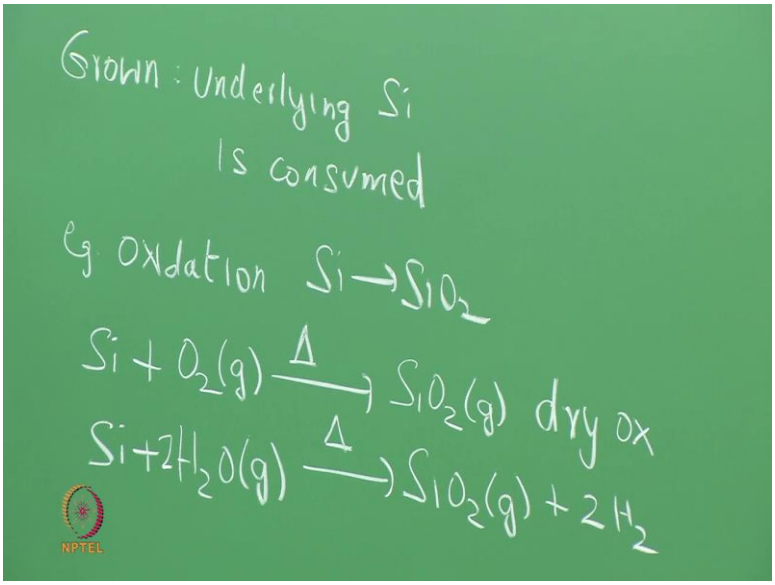


The first one you are going to look at is the layering step. So, just from the term layering means; you are trying to add a layer or a thin film to the wafer surface. So, you're adding a thin film the wafer surface there are essentially 2 ways of doing this. So, if we look at layering you can have films, there are grown on to your wafer surface or you can have films that have depositing. So, in the case of grown films, we are consuming the silicon

that is already present in the wafer in order to grow your new layer. So, here in the grown films the underlined silicon is consumed.

So, example of grown film can include oxidation in which, case you are forming in an oxide layer by consuming the silicon your also have nitridation were instead of forming an oxide layer, you forming a nitride layer, but either case the silicon in your wafer consumed in order to form the oxide or the nitride layer to give an example, of oxidation in oxidation your silicon forms Sio2, the simplest way to form this is by reacting silicon with oxygen.

(Refer Slide Time: 13:08)

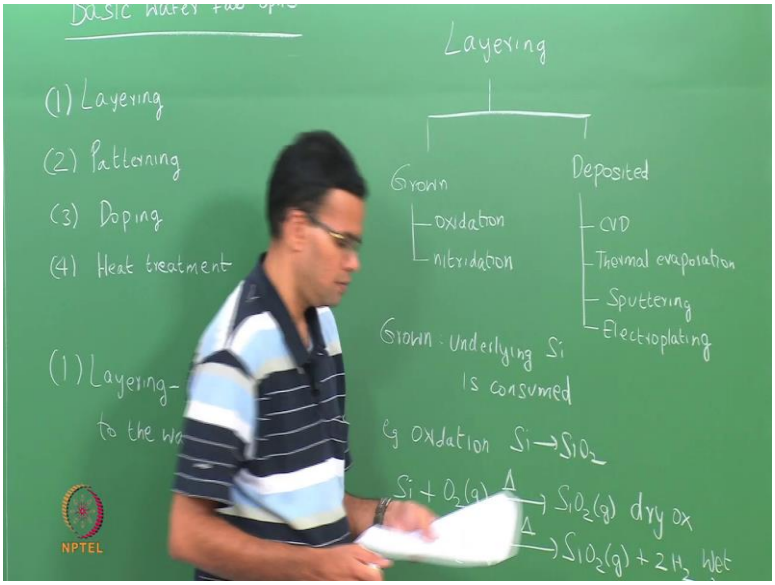


So, oxygen is a gas typically this is done at high temperature to form Sio2, this is called dry ox instead of oxygen you can also use water or steam. So, silicon plus H2o gas in just for balance it could to, again a high temperature gives you Sio2 gas plus 2 H2. So, here were you are using water is called wet ox. So, in both cases the gas you are supplying is oxygen or steam and the silicon comes from the wafer. Compare to grown layers, deposited layers are those were you deposit the layer on to a wafer surface and do not consume the underline silicon. There are a variety of deposited layers.

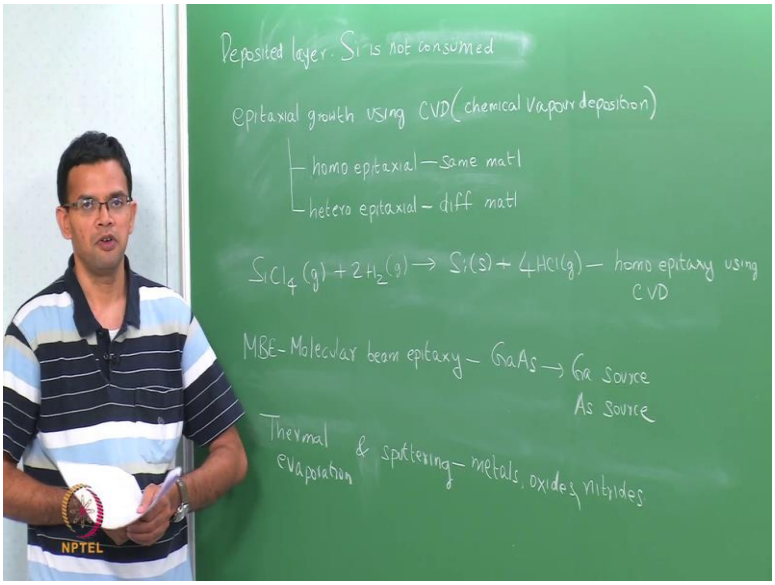
So, they can be grown by chemical wafer deposition, thermal evaporation spattering both

thermal evaporation and spattering are called physical wafer deposition processes; well this 1 is chemical wafer deposition you can also have electro plating. So, these are some examples or some techniques, of growing deposited layers onto the wafer. So, let us look some of them briefly.

(Refer Slide Time: 15:21)



(Refer Slide Time: 15:28)



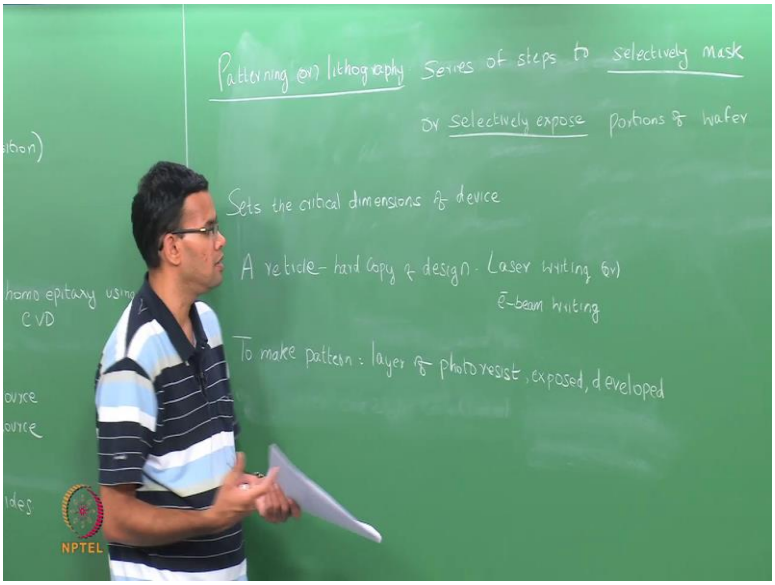
So, in the case of a deposited film, the underline silicon is not consuming deposited layer. So, we saw some examples of processes 1 common example is, an epitaxial growth process using chemical wafer definition. So, CVD; let me write the full form here CVD stands it chemical wafer definition; in the case, of an epitaxial process you growing a new layer, having the same orientation as that of the substrate, epitaxial growth can be homo epitaxial. In which case, the material is just same you can also have hatero epitaxial growth, which case you are growing a different material for example, in the case of a silicon wafer we will possible to grow an epitaxial layer of silicon on top of the wafer.

So, this can be done by reducing declorocilane glass or tetra clorocilane glass along with hydrogen. So, SiCl4 with hydrogen it gives you silicon solid plus 4 Hcl gas. So, this reaction can take place in the gas face and the silicon solid that is formed gets deposited onto the substrate and has the same orientation as that of the substitute. So, this could be an example, of homo epitaxial using chemical wafer definition another way of growing epitaxial layers is called molecular beam epitaxial or MBE. So, in this particular case molecular beams of the constituency of a layer are directed on to the surface.

So, for example, if a trying to grow gallium arsenide you have a gallium source and an arsenic source. So, both of these sources are used to produce molecular beams, of gallium and arsenic which are deposited on to the surface and form gallium arsenide. The advantage of MBE is a very precise composition can be obtained. It is also possible to dope for example, if you want to dope gallium arsenide which something like say sulfur or phosphorus or any other group 2 element that, can be also added as a source and we controlling the amount of material in that a précised amount of doping.

So, this is an example of a deposited layer both CVD and MBE, you can also that deposited layer by physical wafer processes. So, in that case we have thermal evaporation or spattering rather you should say thermal evaporation and spattering because both are physical wafer deposition processes. So, they can be use for growing metals, oxides, nitrides and a variety of other materials. So, first we have looked at layering which is a way of adding a layer of thin film onto a substrate the substrate here being the wafer.

(Refer Slide Time: 20:40)

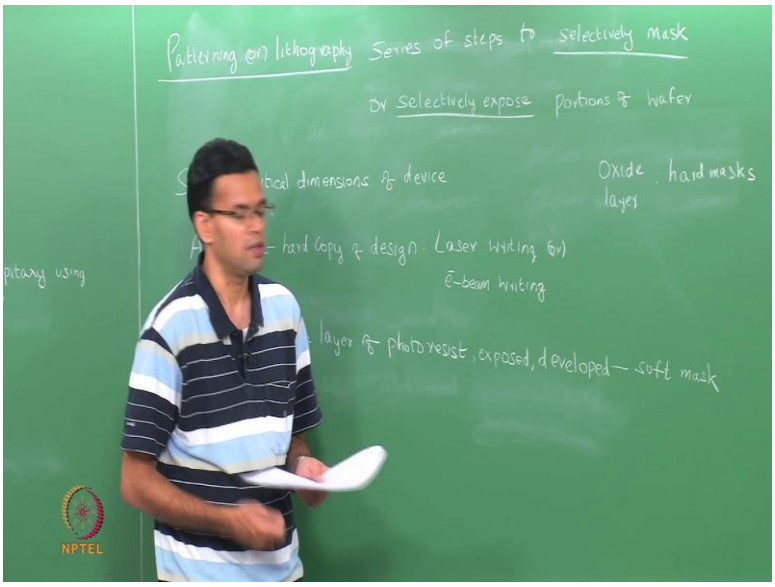


The next most important part, in the case of wafer fab operation is the lithography step. So, the next step is called patterning, another name for it is lithography, this is 1 of the most important steps, in wafer fabrication because this is used in order to define the size or dimensions of the various components of the device. So, patterning is defined as a series of steps that is used to selectively mask or selectively expose parts of the wafer. So, it is not 1 step, but it is a series of steps to selectively mask which means, the selectively cover or selectively expose, which is sort of the compliment the mask portions of the wafer surface.

So, this we do because of the exposed regions you can do other things. You can do doping, you can do layering, you could do hatching or you could do other processes on these portions that are exposed. So, that you can build a pattern on to your wafer. So, lithography is important because which sets, critical dimensions of the device. So, remember, with the increase in technology we have a situation where are trying to pack more and more transistors in a smaller area. So, that the individual device dimensions are all going smaller. So, the latest technology right now is called 28 nanometer technologies the next 1 is 22 and then, it is 14 nanometers, 11 nanometers and so on. So, this size here

refers to a critical dimension of the device and this is d dawn the ability to pattern the smaller and smaller areas on to the wafer.

(Refer Slide Time: 25:48)

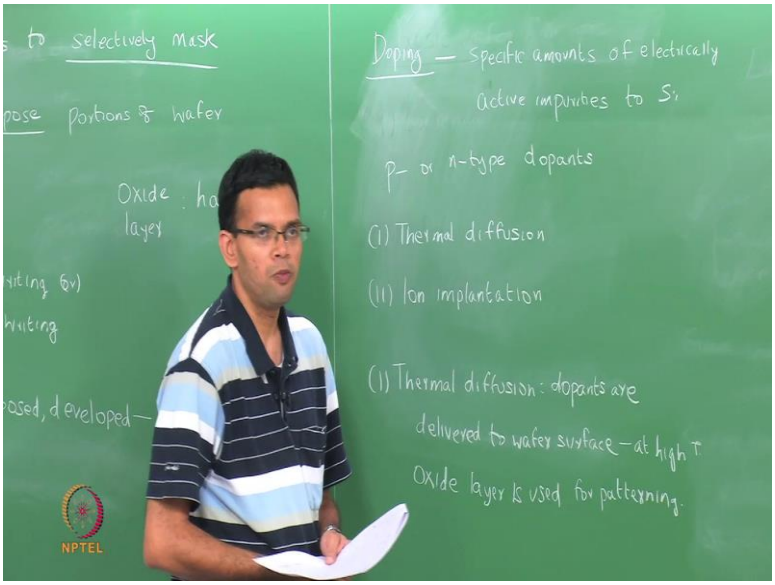


So, the patterning process is also highly defective processes, highly defect sensitive. So, if you want to grow things on a smaller and smaller area then, defect control is something there is very important. For lithography or patterning a reticule or usually madder a retile is nothing but, the hard copy of the design that we want to pattern on to the wafer. So, reticule is usually generated by using a laser beam or electron beam. So, it is by a process called laser writing or for smaller dimensions, you go for electron beam writing and usually this is done, on a layer of chromium in the case of laser writing a layer of chromium on a quartz glass or a borosilicate glass. So, this forms the hardcopy of the design, which is then copied onto each and everywhere.

So, this is done by coating a layer of photo resist. So, to make the pattern a layer of photo resist is added to the substrate or to the wafer, which is then expose to UV light through the pattern. So, that some portions of the photo resist is exposed. Well, other portions are blocked this is then developed. So, this language very similar to a film camera and after developing and removing the photo resist, the pattern is formed on to the wafer. Sometimes an oxide mask can also be used for patterning instead of a photo resist, those

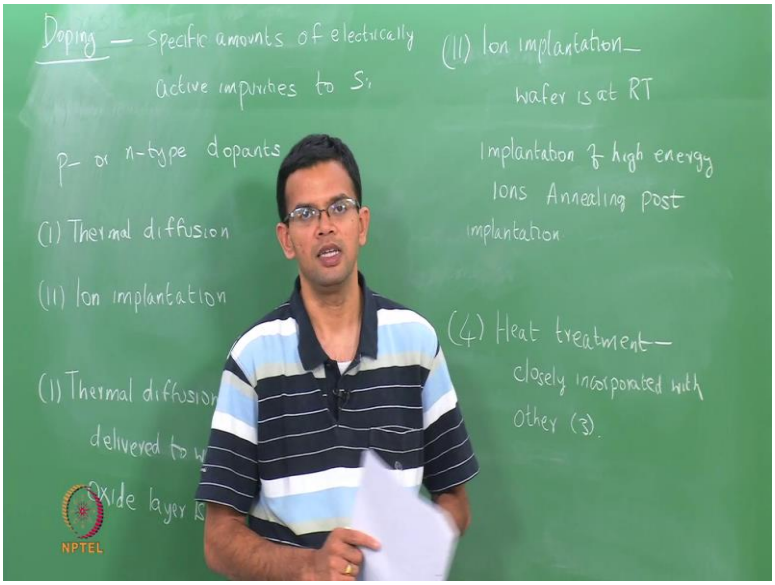
types of mask, I called hard mask.

(Refer Slide Time: 26:28)



So, you could use an oxide layer for patterning those are called hard mask because they can typically which stand high temperature. A pattern that is formed using a photo resist is called as soft mask, which can typically which stand of few 100 degrees, were definitely not much more than 200 or said 250 degrees. So, we have looked at layering, you have looked at lithography the next thing we will going to look at is doping. So, doping is something which you have seen before, right to the beginning of the course it is a process of adding electrically active impurities. We want to add specific amounts of electrically active impurities to your wafer.

(Refer Slide Time: 29:51)



In order to get desired electrical properties for example, if you want to form a P-n junction and your starting wafer is n-type in a typically add P-type impurities or P-type dopings to form the junction. So, you dopings can either by P or n type dopings and we have already seen examples of them. In the case of silicon, there are 2 main techniques for doping, you can either dope by thermal diffusion or you can dope, by ion implantation. So, thermal diffusion as a name implies is a diffusion process the dopings are delivered to the surface of the wafer which is a high temperature.

So, the wafer surface is maintained a high temperature and then the doping just defused into a material. So, this is a high temperature and you have a classic diffusion. So, the dopings can be delivered, either in a solid form or in the form of a wafer or in the form of liquid. So, you have different sources depending upon what type, in which you are delivering the dopings this will also affect the concentration profiles of the doping within the material. So, whether a solid or a wafer is will affect how the dopings are then distributed in a material.

So, because thermal diffusion is a high temperature process, you cannot use lithography. In order to pattern it, usually an oxide layer is used for patterning. So, the other way of doping is called ion implantation. In the case of ion implantation, the sample is

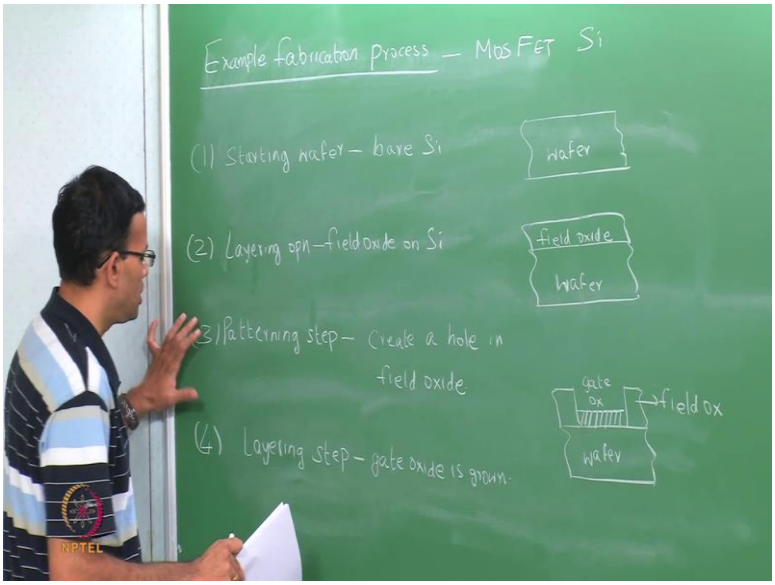
maintained close to room temperature, wafer is a room temperature. The doping atoms are ionized, these ions are accelerated and in pinch on the wafer surface and then, get embedded. So, you a doping not by diffusion, but by implantation of high energy ions. So, here because the wafer is at room temperature, we can also do conventional lithography.

So, you can dope really regions; in the case of, ion implantation dope the fact that you a hitting that a wafer surface with high energy ions can lead to wafer surface damage. So, usually some sort of unhealing is used post ion implantation. So, you do un healing post implantation to repair the surface. So, we have looked at layering, patterning and doping; the last classification is heat treatment. So, heat treatment operations are usually a part of the other 3. So, sometimes there is not always essential to treated as a separate step, it is closely incorporated with the other 3 operating other three categories.

For example; in the case of layering, were we deposit a layer of metal and heat treatment operation of or unhealing operation can follow it. In order to react the metal with the silicon to form silicides. So, this is especially useful for forming good electrical contacts. In the case of doping with ion implantation once again you can have a heat treatment post implantation, to repair the damage in the wafer. Similarly, in the case of lithography when you first put the photo resist layer onto the wafer, you do a soft bake which is a soft unhealing step. In order to remove the solvent and then after exposure and development we do a hard bake in order to harden the photo resist layer.

So, in these of these cases these are all heat treatment operations, which is fully incorporated with the other thing. So, you looked at an overview of the various fab operations. So, you can always think of the operations in the fab as sort of an assembly line, by your wafer grows from 1 step to the next and undergoes some process. So, let us look at an example, of a fabrication of a device starting from a blank silicon wafer, in order to understand how these various steps play a role.

(Refer Slide Time: 33:39)



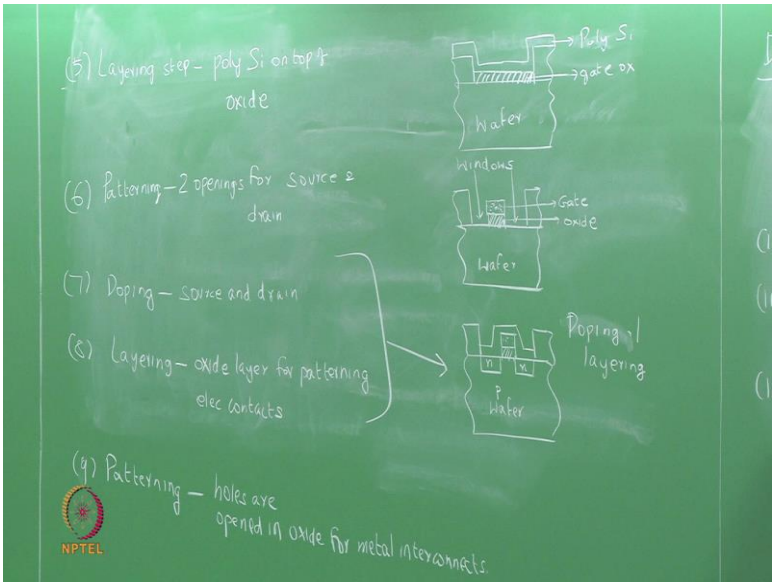
So, we are going to look at an example fabrication process and the process, we are going to look at is the formation of a MOSFET device on silicon. So, MOSFET is nothing but, your metal oxide semi conductor field affect transistor. So, you have seen a mosfet device before we also seen how the device actually looks you seen, the schematic of the device. So, now, you are going to look at the various steps to actually form of fabricate this device. So, the first thing is off course, your starting wafer this is the bare silicon that enters the fab. So, this is just a wafer. So, on this bare wafer that growing to grow an oxide layer, which you will use for patterning this oxide layer is called a field oxide.

So, the first step is your layering step or a layering operation. So, this is to grow the field oxide. So, this is an oxide layer that is, grown on to the silicon layer. So, this could be by dry ox or wet ox, but either way or the lined wafer that is, once we are done growing field oxide, you are going to go to a patterning step. The case of patterning step we want to open a window in the field oxide. So, that we can deposit the gate oxide in also the gate. So, if you remember a MOSFET device, a MOSFET has a gate and a source and a drained region. So, the first thing we going to do is to make the gate. So, far making the gate we use patterning and the use the appropriate mass. So, mass you look at later, but we use the appropriate mass to create a window.

So, create a hole in the field oxide; now, you are going to grow an oxide layer. So, this oxide layer is the gate oxide. So, this is again a layering step, in earlier technologies usually s a o2 will act as the gate; later silicon ox nitrites and now even some high k bioelectric materials are used as gate oxide, but whatever be the oxide is basically a layer. So, a now you a created a wafer or a started which your wafer, you created a whole in the field oxide and then you grown the gate oxide this is my wafer, this is the gate ox, this is still, the field oxide.

So, this diagram actually combines both these steps both the patterning and the layering step. So, after growing the gate oxide you grow a layer of poly silicon on top of that, this is to form the gate. So, the gate is usually a highly conduct to material, can either be a metal or in this particular case we can use heavily doped poly silicon.

(Refer Slide Time: 38:25)



So, in this step you know another half a layering step very grows a layer of poly silicon is typically grown by chemical wafer deposition. So, if we look at the diagram it is again a wafer have my field oxide layer. I have my gate oxide in then, I growing a layer of poly silicon on top wafer, this is poly silicon this is gate oxide. So, we then need to define both the source and the drain. So, if you remember in the case of a MOSFET led say you have p- types of silicon, the source and drains are n-type silicon. So, we need to do some

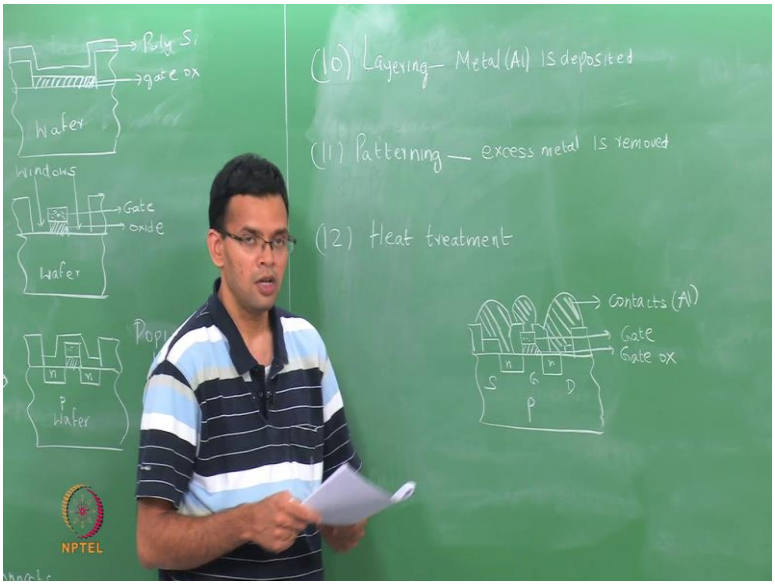
sort of doping.

So, the next step is to do the patterning in order to create 2 openings first source and drain when you do the patterning you will also remove the x s poly silicon. So, that only have poly silicon in the gate region now if you look at it wafer field ox, I only have my gate oxide, in the center and then I have the poly silicon gate on top this is the gate and this the oxide and you have 2 windows that are open for forming the source and the drain. So, after patterning the next operation is doping.

So, of the underline wafer is P-type your doping will be n-type and the underline wafer is n the doping will be P. You can either use a solid dopant or a liquid or a gas; either way, you can defuse some material in order to create the source and the drain. So, after doping you again have to pattern in order to make the electrical contacts. So, the first step to do that patterning is layering. So, you grow an oxide layer on top. So, this is for patterning electrical contacts. Your let me draw that, in a wafer I have my field oxide from the start I have my gate oxide on gate ,I have 2 regions which, I have doped to form my channels I am going to assume my wafer is P-type.

So, that the 2 source are drain are end type than I have in oxide layer on top. So, this is patterning and layering combine. So, after layering you again do, you do the patterning step. So, you this is doping and layering combine this refers, these 2. So, after layering you do patterning in order to create holes in the oxide. So, we can deposit the metal and form interconnects.

(Refer Slide Time: 44:23)



So, we do patterning in order to create holes for depositing the metal. So, the metal layer could be something likes a aluminum, is the metal layer is deposited. So, this could be done by a physical wafer deposition process likes as spattering. After we deposit the metal we go for another layer of patterning in order to remove any excess metal. First this is a uniform def au deposition. So, it will go all over the place. So, we want to remove the excess metal. And finally, some sort of a heat treatment is done. So, that the metal layer will react with silicon to form a silicide with gives a good electrical contact. So, if we look at the final structure of the device. So, you have your wafer, which is a P-type wafer, is still have the oxide layer at the both edges.

So, this oxide layer basically acts the separate 1 MOSFET from the next, you have 2 regions, which are doped. So, they form your source and the drain, then you have a gate oxide and then a gate region; you also have electrical contacts. So, these refers. So, in this case, I am first drawing the oxide isolation which you also have electrical contacts to the source, to the gate and the drain. So, this is source that is the drain that is the gate these are the contacts. So, typically aluminum, this is the poly silicon gate that is the gate oxide.

So, in order to form this mosfet starting from bare silicon we will go through a series of

steps this particular example. There are approximately 12 steps; in order to get the final device, in this series you are not looked at inspection or looked at various steps. So, usually also have inspection steps, there were also included along with this. So, this is just an overview of the various processes that, take place during IC device manufacture. In the next few classes, you will look at each of these in detail. So, we understand how the processes actually.