# Electronic Materials, Devices and Fabrication

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## Lecture No.-21
## Si wafer manufacturing

So, let us start with brief recap of last class. So, last class we looked that a very short history of IC device a manufacture. So, we saw that the integrated circuit is 1, in which the various circuit elements. So, it could be a diode, a transistor, resistor, capacitor or all manufactured or fabricated on a single wafer. So, this type is called monolithic integrated circuit because, you have the same chip. We saw that, the first IC’s where built somewhere in the early 1960s. They had a few 10s or 100s of the devices, which a fabricated on a single wafer.

With time, the number of devices on a wafer increased exponentially. This is given by a Moore’s law which says that, the number of components doubles in nearly 2 years. So, right now, we have wafers with more than 10 to the 7 or 10 to the 8 components. So, these could be the transistors on a single wafer. Correspondingly with increase in devices density, there is also shrinkage in the dimension of the individual components. So, starting with in the 1960s, we had components that were of few micrometers long, now we have components that we order of 10s of nanometers. In all of this, the first thing you need is your blank silicon wafer. So, today we are going to focus on silicon wafer fabrication and production.

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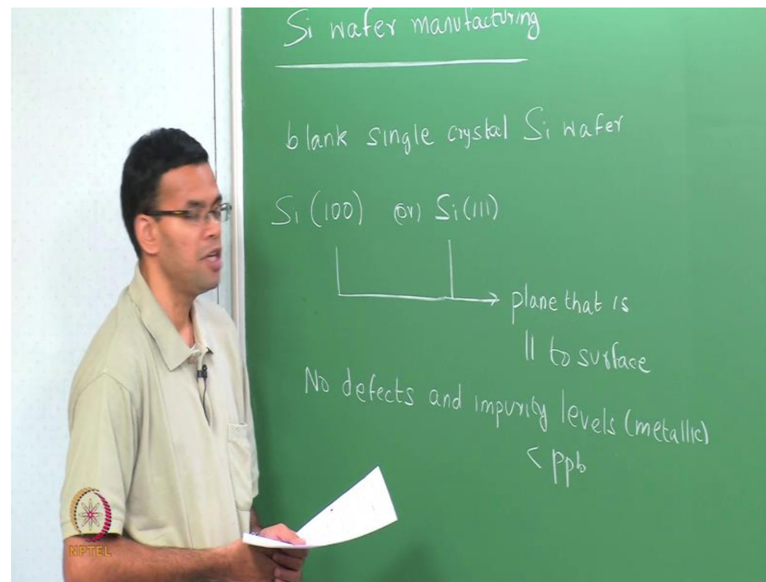


Or we look and the manufacturing of silicon wafer. So, in the case of the fable, the first thing you need is a blank single crystal silicon wafer. So, this blank wafer goes through all the operations in the fable, in order to produce the various components of the integrated circuit. Silicon wafer usually has a specific orientation. So, we either talk about silicone 1 0 0 or silicone 1 1 1. These are the most commonly used wafers. 1 0 0 and 1 1 1 refers to the plane that is parallel to the surface.

We also need to manufacture these wafers with very low defects. For example, things like these locations because, these interned can affect the electronic properties. More importantly, defects can also cause the devices to fail because, later we will see that these wafers go through whole bunch of processing operation; thermal grandniece, stress grandniece so that, defects in the crystal can cause the wafers to break. They must also have very low impurity concentration especially metallic impurities should have concentration less than a few parts per billion.

So, we ideally want materials with no defects an impurity levels. So, this should not be confused we dopens. So, dopens are impurities that are added intestinally, but, impurity levels especially metallic should be less than a few part for believe. So, we want a material that is extremely pure.

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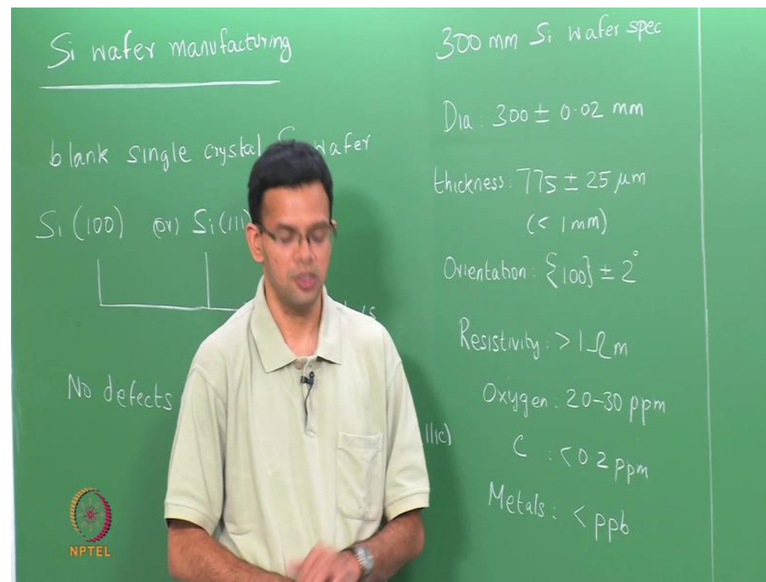


So, let me give some specs the case of a current 300 millimeter silicon wafer. So, a 300 millimeter or 12 inch wafer is what is currently being used in the IC industry. So, it would have a diameter; the very small deviation from 300 millimeter. The thickness of this wafer is very small 5 plus 25 micrometers which is less than 1 millimeter, so approximately 0.75 millimeter.

So, we are looking to make a wafer that has a thickness, that is, less than 1 3 hundredth of the diameters. So, these are really thin wafers. The orientation, it can be 1 0 0 or 1 1 1 but, the deviation from that should be very small; less than 2 degrees. Typically you may you mention the resistivity of the wafer. So, this determines the doping concentration in the blank wafer. So, this resistivity values can be modified locally, on order to introduced things like a p n junction all things like transistors. So, they will be done during the process of IC manufacture, but, the blank wafers should have a certain resistivity value that is specified by the user.

If, you also look at countermines, oxygen levels should be around 20 to 30 parts per million. And carbon, metals usually aluminum and iron are in impurities, there should be of the order of parts per billion. So, this is a typical specification for a 300 millimeter wafer that is used in the fable. So, we need to make this, starting from the silicon worse, we now look at the various processes that go through it.

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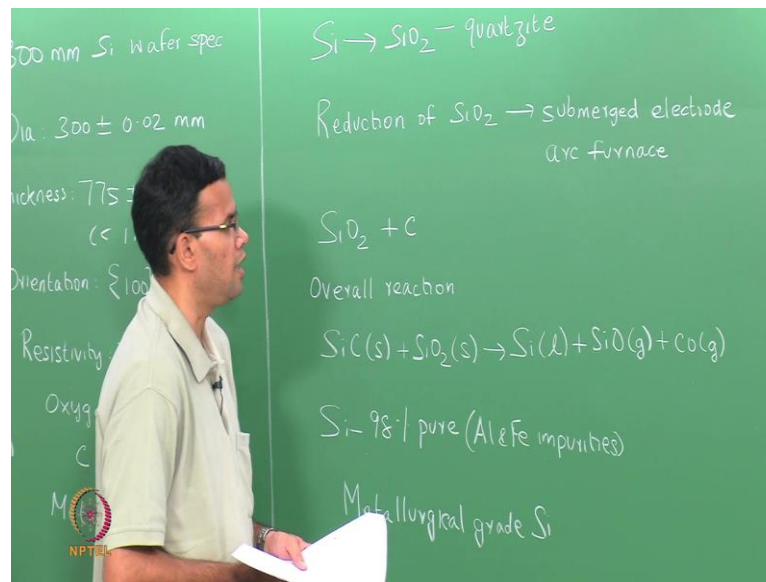


So, the starting worse for silicon is off course sand or S i O 2. S i O 2 is just quart and the over is called quartzite. Quartzite is relatively pure form of silicon, we does have as metallic impurity in it. So, this over S i O 2 has to be reduced in order to get silicon. So, the first thing is reduction of S i O 2. So, in this case quartzite is mixed along with carbon. Carbon is usually in the form of coke and it is taken in a submerged electrode arc furnace. So, in this case S i O 2 is mixed with carbon. So, carbon reacts with the silica in order to forms silicon carbide. And then, the silicon carbide and the silica react to finally, give you silicon.

So, the overall reaction here; the silicon carbide plus S i O 2 giving you silicon and the temperature is high enough so that, the silicon is in a molten form, plus S i O in the gas face plus CO gas. So, silicon that is obtained the liquid form is separated, this silicon is proximately 98 percent pure, aluminum and iron are the impurities and this is called metallurgical grade silicon. So, we can draw small schematic of the submerged electrode arc furnace.

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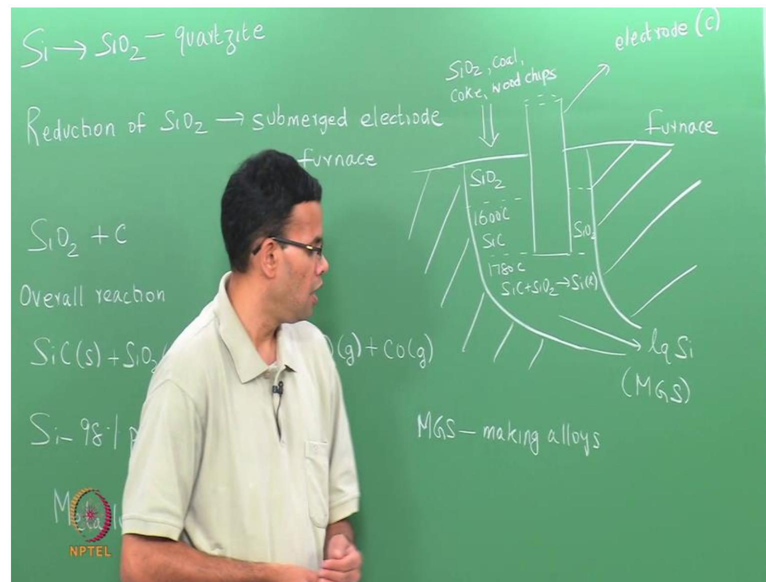


So this is the electrode. Electrode is made of carbon. SO, the shaded region represents the furnace walls. So, the input to a furnace is quartzite along with carbon. So, S i O 2, carbon is the taken in the form of coal coke, wood chips. So, initially the S i O 2 reacts in order to found silicon carbide, so you can divide the furnace into different regions. And then the silicon carbide and silicon oxide or S i O 2 react in order to give you silicon. And then this liquid silicon is just discharged from you reactor. So, this is your metallurgical grade silicon. So, let me just call at MGS. So, let me just marked MGS. So, this is the first step in manufacture of a silicon wafers, getting the metallurgical grade silicon.

So, MGS is also used for making a aliased. So, for example, lot of silly sides is made by combining silicon with metals. For example, you can a have silicon along with platinum, silicon along with aluminum. So, there is lot of aliased made using silicon and for this metallurgical grade silicon is good, has around 98 percent purity. But, in the case of IC manufacturing, we want you impurity levels to be of the order of parts per believe. So, this metallurgical grade silicon must be further purified.

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Next step is the purification of MGS. So, this purification is done by using a fractional distillation process. So, here silicon is reacted with hydrochloric acid gas, in the gas form in order to form S i H C l 3. So S i H C l 3 is in the wafer form and this fractionally distilled, so it is purified. This is an reduced in order to give silicon. So, the starting reaction is silicon solid, this is your metallurgical grade silicon, reacts with H C l gas in order to give you S i H C l 3plus left over hydrogen. This process is exothermic.

The reaction is done in fluidize bed reactor, typically at 300 degree centigrade or above so that, your trichlorosilane S i H C l 3 is in the gas form. This gas is then separated be fractional distillation and then reduce using hydrogen plus hydrogen gas 2 silicon soiled plus H C l gas. So, this process can be repeated in order to increase the purity of the silicon that is up tent. So, we can say this is a looped process. The silicon soiled that is up tent, can further react to the H C l to give S i H C l 3 which are further distilled and so on in order to reduce the amount of impurities, give your final silicon. This silicon that up tent, is called electronic grade silicon EGS.

So, we start with MGS which is the metallurgical grade silicon and by fractional distillation, you remove all the impurities to give you electronic grade silicon. So, this silicon has the amount of impurities of the order of paths per billion. So, it is suitable for use as an IC in as a wafer for IC device manufacture. The only drawback is this is polycrystalline, is usually in the form of ingots, by it is a polycrystalline material.

So, the next step is to convert this polycrystalline EGS in to ingots of single crystal wafer.

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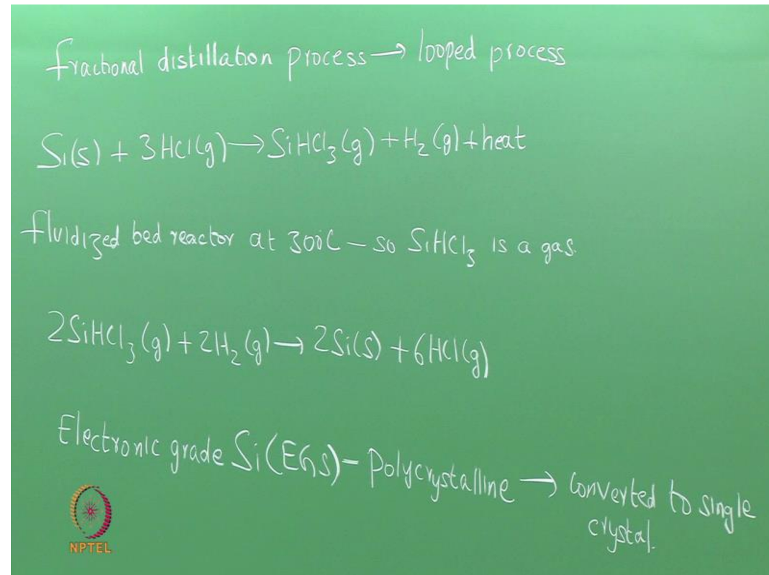


So, this has to be converted. And we also want the single crystal of write orientation. So, remember at the beginning of the class, we said either have silicon 1 0 0 or 1 1 1. So, these is the once most commonly used. So, we need to convert this polycrystalline silicon in order to single crystal. So, we next look at how we do that. So, we need to produce single crystal silicon in that, starting from the polycrystalline electronic grade silicon. There are typically 2 methods for doing it.

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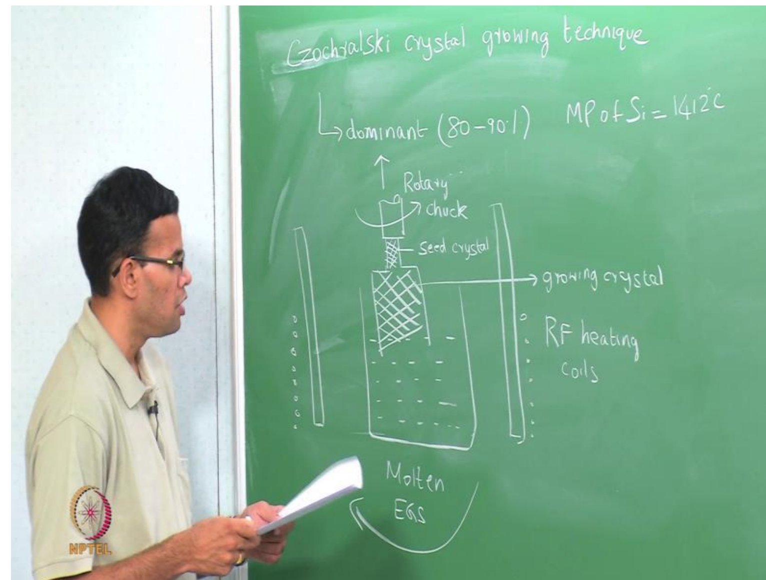


The dominant method is called czochralski crystal growing technique. So, this is the dominant technique for producing the silicon wafers, nearly 80 to 90 percent a wafers a grown by this technique. It is especially shouted for making single crystals of large wafers. So, typically we now use 12 inch or 300 millimeters wafers in the industry. The transition is going to go from 12 inch to even larger to 18 inch wafers or 450 millimeters. So, czochralski growth method is most preferential method for this.

So, in this particular case, you start with the electronic grade silicon. And it is taken in a furnace and melted. So, we have molten silicon in the furnace, the furnace is heated by using order heating calls. So, it typical melting point of silicon is 1412 degrees centigrade so that, the temperature is higher than that. Then a seed crystal is taken, the c crystal has right orientation of what we want. So, if you want silicon 1 0 0 is take a seed crystal with the 1 0 0 orientation, then the other way round, smidge seed crystal.

The seed crystal is depute in to the molten silicon. So, silicon then sticks to the seed and it solely withdrawn. So, as the seed crystal is withdrawn, the silicon that is attached to with start to cool and to takes the same orientation as that of the seed. So, we have a growing crystal here in. As the seed crystal is pulled away, the growing crystal also grows and would has the same orientation as the seed. This is also rotated in order to get a uniform wafer. So, usually it is says nothing, but, rotary check. And it is rotated and at the same time pulled out of the furnace.

So, the trusible also rotated, but, it is rotated in the opposite direction, in order to maintain a uniformity of temperature and uniform growth rate across the entire length of the furnace.

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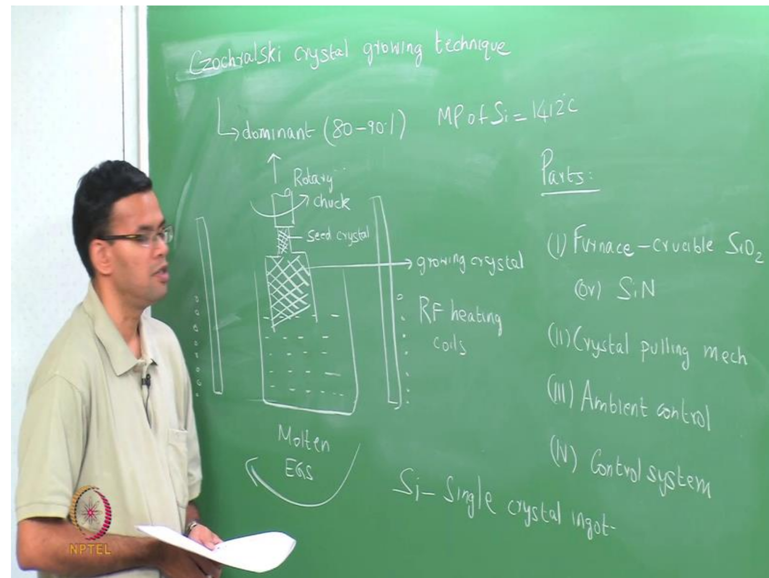


So, the various parts czochralski crystal grower is you furnace. The crushable material that is usually use the silicon dioxide or silicon nitride. The reason being puce any other material because of the high temperature, there is always a chance of contamination. So, usually S i O 2 or S i N is used. The drawback is S i O 2 can also dissolved in the molten silicon so that, the crushable slowly eaten away, as you crystal is being grown. There is a crystal pulling mechanism.

So, crystal pulling mechanism is the rotary check, which pulls the crystal at a rate the dispread determine by the process and the also rotates. There is also an ambient control. So, they ambient control controls a temperature of the furnace, controls the flow of gases within the system. So, it maintains the system properties. And finally, there is a complicated feed back in control system, in order to grow you wafers. So, this is interracial, the czochralski growing grow technique.

So, as mentioned earlier the seed crystal has the same orientation of the final wafer that we want. The final silicon that is sold defined is your single crystal ingot. So, for you doing this, in the case of a 450 millimeter wafer, the ingot can get pretty heavy can be a few 100 kilograms proximately 800 kilograms. So, this process is usually automated. So,

the then entire think in be done, without human intervention. So, 1 way of growing is czochralski grow technique. The other way of producing single crystal silicon wafers is called the float zone technique. So, let us look at that next.

So, the other technique for producing single crystal silicon wafer from the electronic grade silicon is called the float zone technique.

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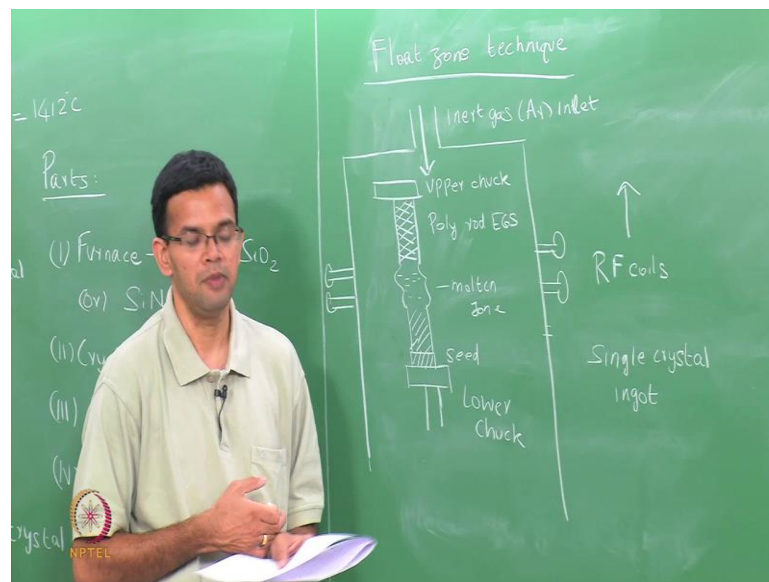


1 of the drawbacks czochralski growth is that, it is done under ambient conditions so that; there is always the possibility of oxygen inclusion in the wafer. For some applications, were oxygen levels have to be really low, we go for the float zone technique. The drawbacks of the float zone technique is that, cannot be used for making large wafers, is usually used for 3inch or 4 inch wafers. So, typically use in share in research lab.

So, in the float zone technique the ingot is taken again in the furnace, there is a seed crystal, so the seed crystal has a right orientation achieve you need, it is maundered on a check me just called it a cower chuck. And the polycrystalline in the wafer in wafer is pushed on to the seed crystal. The whole thing is taken in a furnace. And in order to reduce the oxygen inclusions usually an inert gas is frowned. For example, argon, so you have in argon inlet. So, in this particular case, instead of having a furnace satisfies, you use RF coils to heat the sample, we just draw the coils likelier.

So, these RF coils are used for localize heating and melting. And they travel along the length of the furnace. So, they basically draft around the silicon ingot, there is from a electronic grade silicon and acid goes, it melts the silicon in order to create a molten zone a molten zone. Then there is a rest the endured that is on top. So, the seed crystal is a single crystal and as the ingot is melted, it recrystallizes and takes the same orientation as that of the seed crystal. So, this region has a same orientation; is that of the seed. There is a molten zone and the region above is still the polycrystalline rod.

So, let me just say poly rod to be not that the polycrystalline. So, as the r f coils travels. So, initially the entire rod is polycrystalline, as a travels up, it melts a small region, which recrystallizes with the same orientation is that of the seed. And as the molten zone goes up more and more of the rod becomes single crystal so that, finally, you get you single crystal ingot. And because this entire process is done in an inert gas atmosphere, you can reduce the number or can reduce the concentration of oxygen within a silicon wafer.

So, this both the czochralski growth process and the float zone process, produces a single crystal ingot for the dimension of the ingot depend upon the dimension of the furnace in the process. So, from this ingot, we need to get silicon wafers that are thin. We need wafers whose thickness is less than 1 millimeter.

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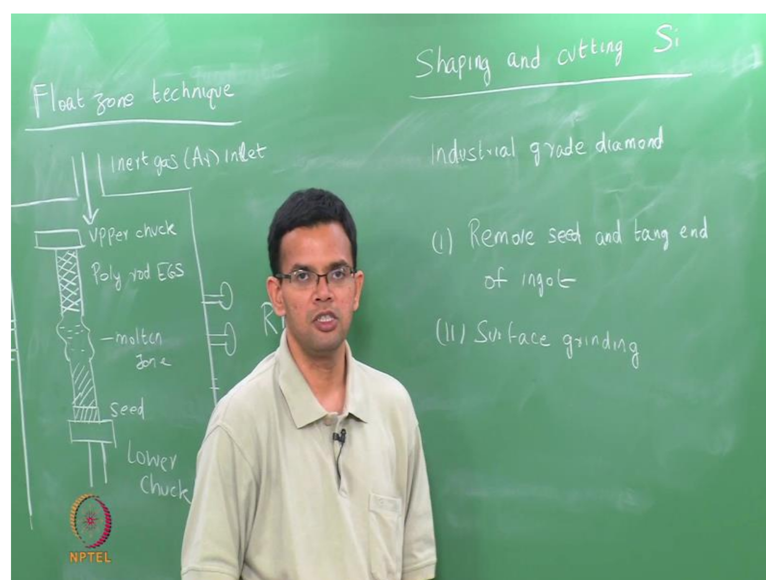

So, we typically need to go for some shaping and cutting operations. So, usually industrial great diamond is used for this process. So, the first step in the shaping operation is to remove the seed and also the tang end from the ingot. So, you remove both ends of the ingot. And then, you do a surface grinding operation in order to increase the smoothness of surface.

So, the size of the ingot is determined by the size or the diameter of the final wafers that we want. So, if you want 300 millimeter wafers, you start with an ingot that is slightly larger in 300 millimeters because, during some of these operations, you lose some amount of a surface. Once you remove the seed and you do the surface grinding, then we also grind something known as flats, along the entire length of the wafer.

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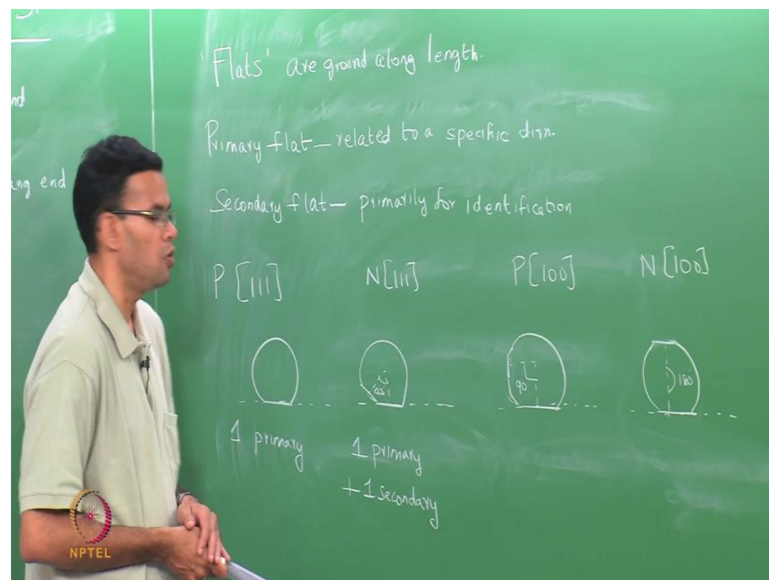


So, after the surface grinding operation, flats are ground along the length of the wafer. So, is something called a primary flat, which is related to a specific crystal direction, this is usually located by using the acres. You also grind a secondary flat primarily for identification purpose. So, for example, we have a p type silicon, it has a 1 1 1 orientation. So, here the 1 1 1 direction, is perpendicular to the surface or in other words the 1 1 1 plans a parlor to the surface. There is just 1 primary flat. So, flat is just that it is a flat region in a wafer. So, this flat region represent your primary flat, is 1 primary.

If instead of p type, you have n type 1 1 1, there is 1 primary flat, but, then there is also a secondary flat that is ground at 45 degrees. So, in this case, you have 1 primary plus 1

secondary. If you have a p type 1 0 0, you have 2 flats; 1 primary flat and a secondary flat that is at 90 degrees, you just draw note clearly. So, once again you have 1 primary in once secondary at 90 degrees. And if you have an n type 1 0 0 have 1 primary and 1 secondary flat, that is, at 180 degrees.

So, the function of the flat is to marked the mager crystallography direction and also as a way of sorting out different wafers. So, rather than having to measure resistivity, just by looking at the orientation of the flats, is possible to say whether you have a p type or an n type or whether you have 1 0 0 or 1 1 1 kind of wafers.

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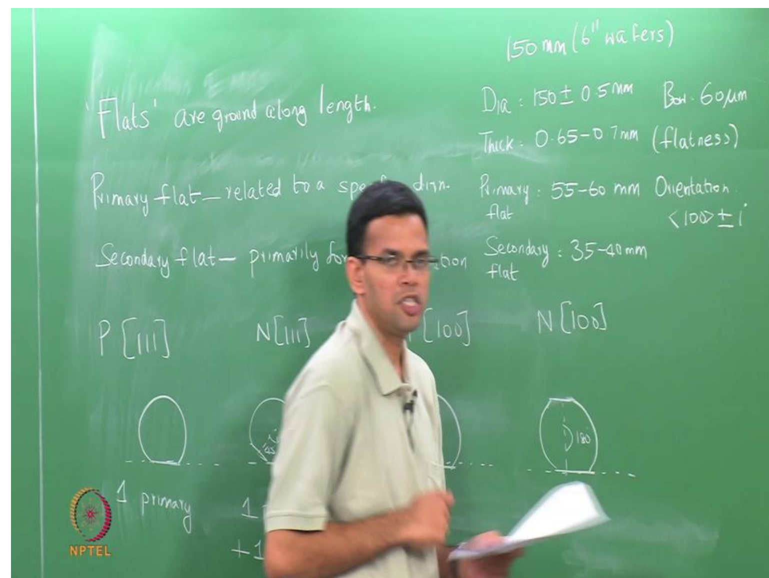


So, we can look at some typical specs. So, you have seen a 300 millimeter wafers before. So, let us just look at 150 millimeter wafer, these are 6 inch wafers. So, once again your diameter has be pretty close; 150 plus or minus 0.5 millimeters, thickness is 0.65 to 0.7 millimeters or 600 to 700 micrometers. You have a primary flat, there is somewhere around 55 to 60 millimeters and then a secondary flat, if it is not p type 1 1 1, which is slightly smaller; 35 to 40 millimeters. And the orientation of the secondary flat depends upon the tight and the orientation of the base crystal.

So, we also defined a wafer above. So, 60 micrometers; this defines the flatness of the wafers. So, if you think about it, you have a wafer at a 6 inch in diameter, but, whose thickness is very small, it is less than 1 millimeter. So, this wafer will not be completely flat, during the processing operations is always some stress. So, that there is always be a

curvature to the wafer to the wafer to the wafer. So, this curvature is defined by the wafer bound. We want this number to as small as possible.

So, let we have a flat wafer. So, later we see that, when this wafer is used for various processing operations for example, of you deposit films on this, in that can call stresses in the wafer, it is can also lead to additional above. So, we want to start the blank wafer as flat as possible. And the orientation, so whether which 1 0 0 or 0 1 or 1 1 1, we want the orientation to be within plus or minus 1 degree or 2 degree. So, we started with the ingot, we cut out the seed and the tang ends, did a surface grinding and then also ground all the flats, whether we have 1 primary flat the primary and secondary flat, the respective orientation.

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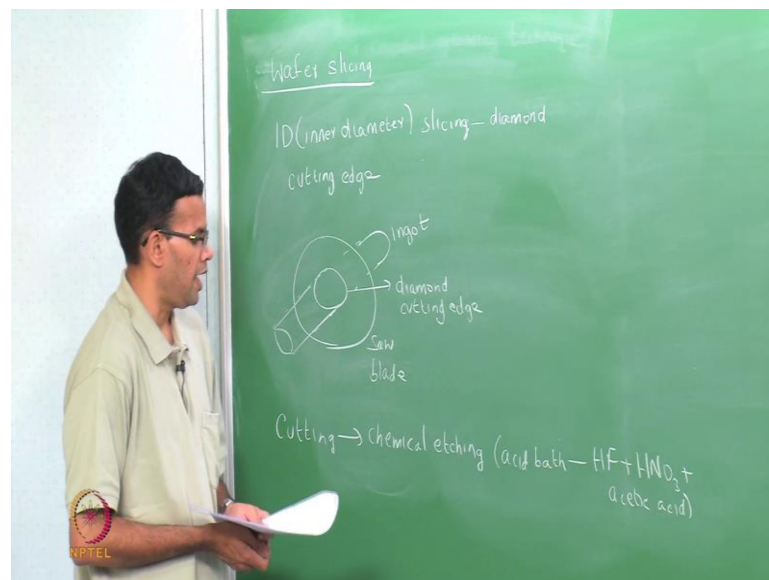


Then, we need to do wafers slicing so that, we slice the individual wafers off of the ingot. So, usually an inner diameters slicer is most common and the cutting edge is usually a diamond cutting edge. So, in this particular example, so here is the slow in the saw blade with a diamond cutting edge on the inside. The wafer is just fed through it. So, this is the ingot. So, the ingot is just fed through, it in the diamond saw, cuts out the portions of the wafers at the right thickness. So, thickness usually increases with increasing diameter, we look at 3inch or 4 inch wafers, there usually around 0.5 millimeters or 500 micrometers thick, with increase in a diameter to basically have better mechanical integrity, the thickness is also increased. So, a 12 inch wafer is usually

around 0.75 millimeters or 750 micrometers thick. So, after cutting, then we do a chemical etching process. So, after cutting so the etching removes any damage or any contaminated regions; usually an acid bath is used with a mixer of H F hydrofluoric and nitric and acetic acid. After etching, the surface of the wafer is polished.

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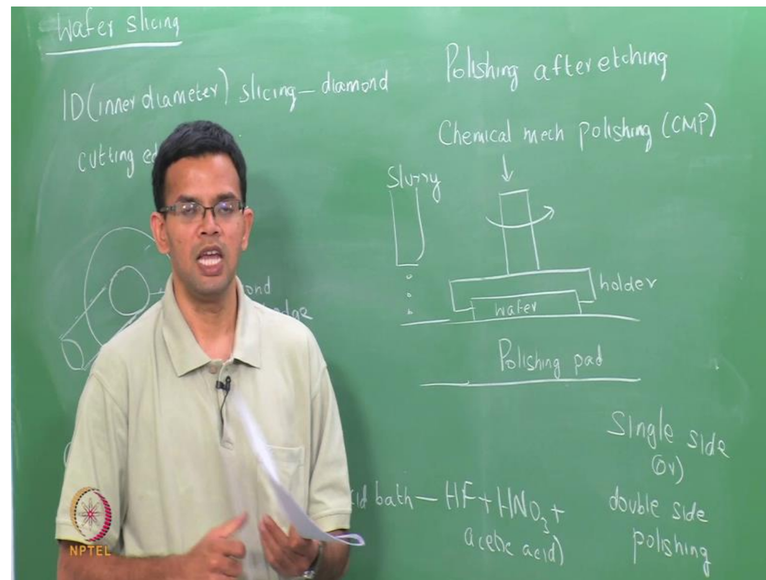


So, we go through of polishing step. So, this kind of polishing is called chemical mechanical polishing or CMP. So, later when we look at wafer fabrication, we see that CMP as 1 of the important steps forms a part of an operation call planarization. So, in this case, a polishing pad is taken and the wafer is placed on to the pad, which some short of holder. So, some amount of fresher is applied, while at the same time the holder is rotated. There is a slurry, so the slurry is some liquid with dissolved particles. So, in this particular case, this slurry used is S i O 2 usually dissolved in N a O H. So, the sodium hydroxide works in the form of chemical reaction, in order to dissolved any of the impurities and particles. And the S i O 2 acts as an abrasive material i order to polish the surface. So, that is way it is called chemical mechanical polishing because, you both have a chemical component and a mechanical component.

So, the surface of the wafer is polished. So, usually polishing is done on 1 side, scaling single side polishing, the other side of the wafer is dull. So, the polished side is then, is what is used for the IC fabrication. We can also have double side polishing, in which case both sides of the wafer or polished. So, we can have single side, single side

polishing is most common, but, we also have double side polish wafers. So, after polishing, the wafers are usually taken to an inspection step. So, in the case of inspection, they are checked for any surface contamination or defects. So, we can also measure the resistivity of the wafers. So, this is usually done for 4 point prop technique. This is especially used if you training to make doped wafers.

So, we saw in the case of the operation, we did not considered the effects of the doping, we did could also dope during the silicon manufacturing process, in order to get dope wafers. So, some sort of electrical measurement, usually a resistivity measurement is used in order to check the measure, in order to check the resistivity of these wafers. So, after inspection, these blank wafers are ready to be transfer to the fable, so there will be used for the manufacture of the IC devices.

So, in next class, we will look at a over view of this manufacturing process. Then we will look at each of this process in detail, in order to consider the various steps. But, the starting step for all of these processes is the blank silicon wafer.