**Electronic Materials, Devices and Fabrication**
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Lecture - 20

In this course, we first started by looking at semi conducted materials and the properties; we started with intrinsic semiconductors and then moved on to extrinsic semiconductors. We then looked at devices looked at the verity of devices.

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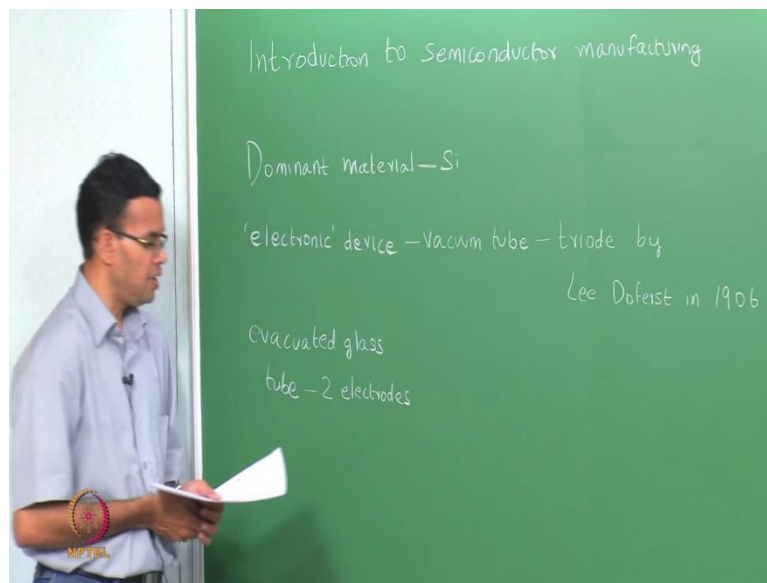
The last part of this course of the last section of this course, we are going to focus on semi conducted manufacturing. So, when we looked at devices, we started with simple p n junctions, we then went on to transistors and we also looked at a verity of optoelectronic devices like LED's, lazars solar cells, then so on. So there are wide variety of material that are used, especially in the case of optoelectronic devices where you have heterostructures; a wide verity of materials based on gallium arsenide is used. But, the dominant material in the semiconductor industry is silicon. One reason for that is a natural abundance of silicon; is 1 of the most widely available materials on earth, it is usually found in the form of SiO_2 a quads and other reason is that the electronic properties of silicon can be precisely controlled by addition of dopants.

So when we talk about electronic properties, mostly the resistant's can be controlled by adding a small amount of do mars or impurity or donors or accepters, as we seen before.

So most of what we do will be with focus with respect to silicon. I will also talk briefly about other materials, especially gallium arsenide but, the dominant material being silicon; there will be the focus when we talk about semi conducted manufacturing.
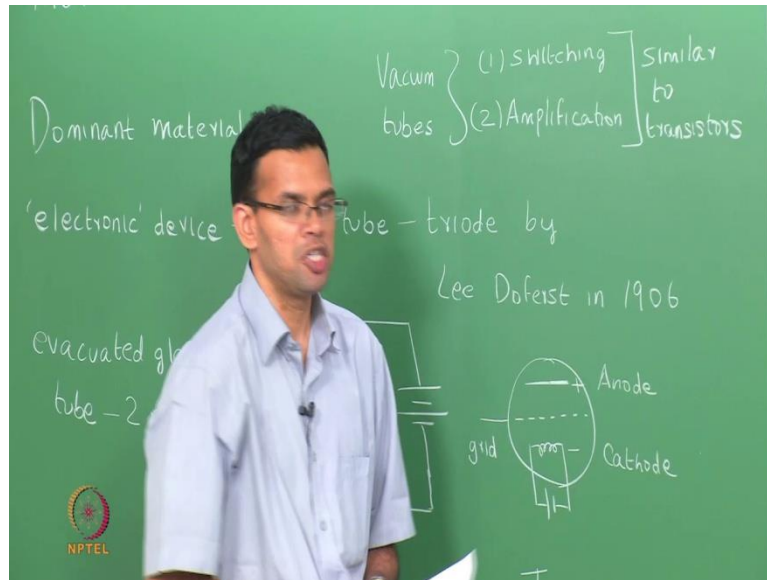
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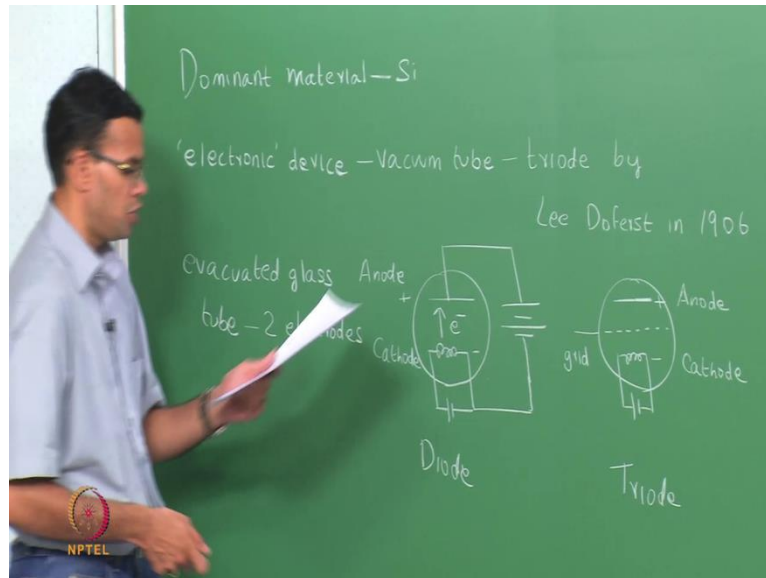
Let us look briefly at the history of device manufacturing. The first electronic device and I write electronic with in quotes was the vacuum tube. This was invented towards the end of the nineteenth century in the beginning of the twentieth century. So, the triode chose 1 form of vacuum tube was invented by Lee Doferst in 1906. So, the vacuum tube consists of an evacuated glass tube. There are usually 2 electrodes; 1 access the anode and the other access the cathode.

So, let me just schematic of the device. So the evacuated glass tube, 1 of the electrode acts as the cathode which is your source of electrons, then you have an anode. The cathode has a negative potential, the anode has a positive potential. This is connected to your outside circuit. So this type of device configuration, where you have 2 electrodes the cathode, let me mark the anode as well is called a diode.

So by applying a current to the cathode, typically the cathode material is heated, so it is thermionic; a machine, electrons are generated and these electrons are accelerated towards the anode and that gives you the current. We can add another electrode to this system to form the triode. So once again have the evacuated glass tube, there is a cathode, and this is negative. There is an anode that is positive and there is a third

electrode that is grid. So grid, anode and cathode. So in this particular configuration, the current between the anode and cathode can be modified by application of a potential to the grid. So the grid can be either positive or negative, with respect to the cathode and that would modify the current within this triode system.

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So vacuum tubes perform essentially 2 functions. They can be used for switching or they can be used for amplification. So in some sense the performance is very similar, to what we expect from your transistors.

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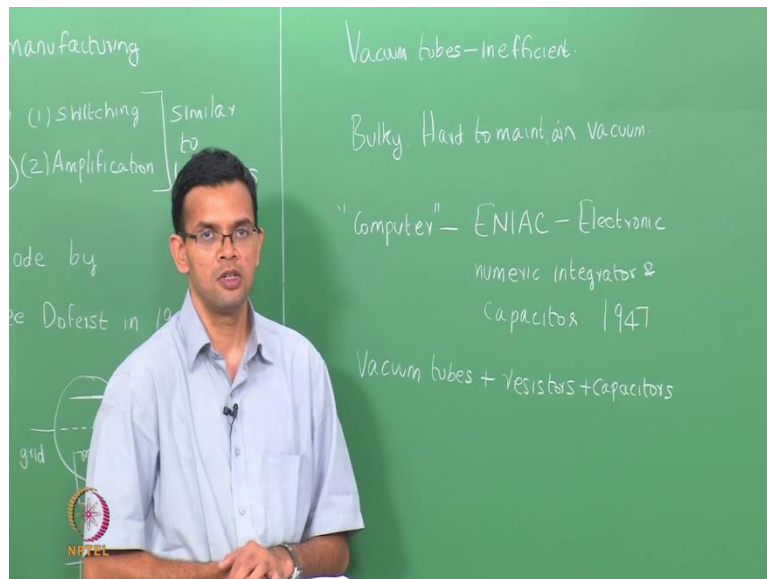
So the vacuum tube itself is the highly inefficient process. They are bulky because, they all have evacuated glass tubes. Also it is very hard to maintain the vacuum in these tubes, so they highly inefficient. But, the vacuum tubes are the forerunners of the modern transistors, so they were used to build the first computer which is call they a ENIAC. So, the ENIAC stands for electronic numeric integrator and capacitor. So this was built in 1947. It was mainly made up of vacuum tubes plus some resistors and capacitors.

So, the ENIAC was capable of numerical calculations but, because it was built out of vacuum tubes, it was huge and bulky, the computer would occupy a large room and we also require a tremendous amount of power in order to run it. To reduce the size of these devices, we need to replace these vacuum tubes with solid state devices

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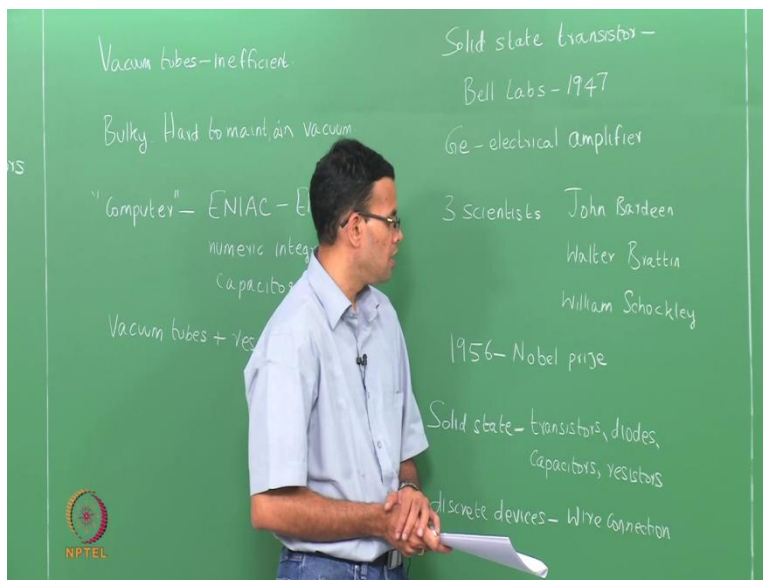
So, the first solid state device or the solid state transistor was built in bell labs in 1947. So, this was an electrical amplifier that was actually made using germanium. So, germanium was the material that was used and if you remember germanium has a smaller ban gap then silicon, so that the intrinsic carrier concentration is higher. So was the first electric electrical amplifier; based out of germanium. So here the germanium actually replaces the vacuum tube the amplifier acts as a transistor and replaces the vacuum tube which is bulky and inefficient.

There were 3 scientist involved in this; John Bardeen, Walter Brattain and William Shockley. They won the Nobel Prize in 1956 for the invention of the transistor. So, using the solid state technology, a verity of devices was built. So you can think about the

transistors which act as your triodes, you can also build diodes which are nothing but, your p n junctions, you can build capacitors or you can build resistors. So, initially these devices were all built as discrete devices. So they built as discrete devices which were then connected by wires.

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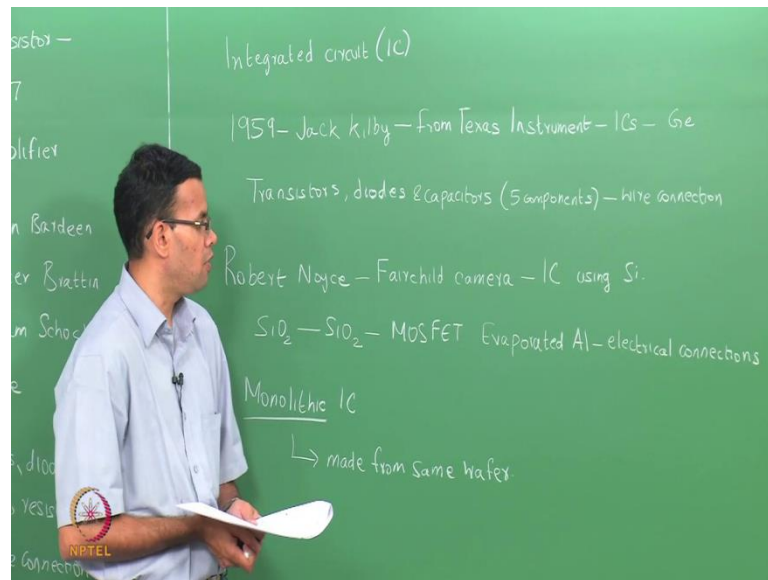
So, they were all built as discrete devices and electrical connections were made in order to build the final device. So first integrated circuit happened, in these different components were made on the same wafer. So in the case of integrated circuits, short form is just IC. So in 1959 Jack kilby from Texas instruments, build the first integrated circuit. So, he build the first integrated circuit and again germanium was the material that was used. In the case of the kilby circuit, he combines transistors, diodes and capacitors, and for resistors he use the natural resistivity of the germanium substrate. So, there were total of 5 components to this but, these were still connected by wires. But, the modern integrate as circuit as we know it, based upon silicon was developed by Robert Noyce who was 1 of the founders of Intel. At that time he was working at Fairchild camera. So he had a different design, where he built the first integrated circuit using silicon.

So the advantage of using silicon, apart from the abundance in this particular case, was its silicon forms a naturally occurring oxide S i O 2. And this S i O 2 on the way for surface can be used as an insulating layer performing MOSFET's. You have seen that before, when you look at MOSFETS's that there was a dielectric layer that separates the

gate from the channel. So this dielectric layer can be easily formed on silicon using S i O 2. Robert Noyce also used evaporated aluminum, performing the electrical connections as approach to using a wire connection so that, your circuit can be thought of as truly integrated. All the components are made out of a single wafer.

So this kind of integrated circuits is called a monolithic IC. And the term monolithic is because, they are all made from the same wafer. So the initial integrated circuits that we formed had only a few components, for the first 1 had only 5 components and later the number of components was usually of 10s or 100s. But, over time the number of components in a given wafer or in a given chip, has increased and at the same time, the size of the devices have also decreased.

So, 2 kinds of improvements have taken place in terms of IC design.

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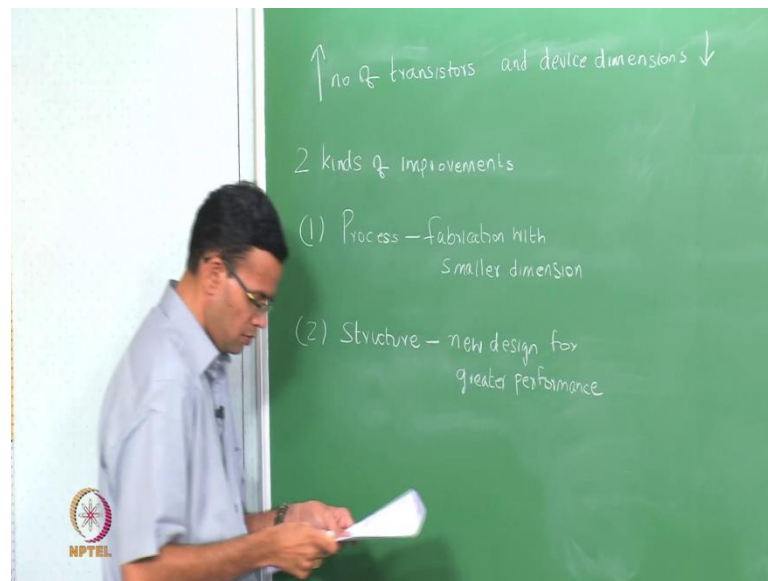
So over time and we look at IC's. The number of transistors has increased, well at the same time the size of the transistors has decreased, I would call it a device dimension, it is nothing but, the size of the transistors. So the improvements in an IC design can be broadly classified into 2 types. So the first 1 was the process improvement, in which case we fabricating the same device and the same structure but, with smaller dimensions. So, this is analogous to sort of taking a chip and then shrinking all the dimensions so that, the overall size is smaller.

The other kind of improvement is your structure improvement, where you have new device designs. So this could be a design in terms of the structure or this could be design in terms of a new material that is being used, in order to give greater performance. We have a new design. So, whenever we talk about integrated circuits, we usually characterize them by the size of the components and also the number of the components.

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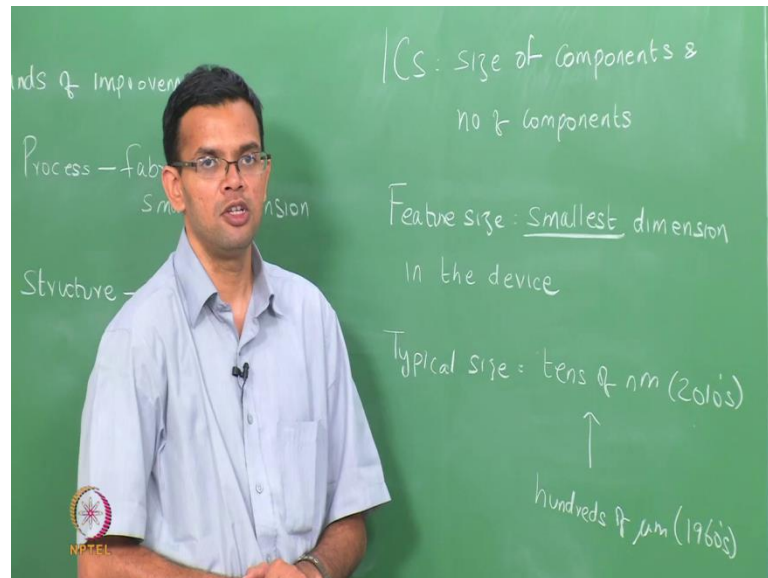
So, always talk about the size of the components. This is usually called a feature size and the number of the components, so this intern as related to your device density. So earlier, the feature size was usually of the order of micrometers, now the size is the around the order of nanometers. So feature size in an IC circuit; usually refers to the smallest dimension in the device. So usually, this is taken as the distance between 2 gates, when you are thinking about transistors that fabricated in wafers.

So it typical feature size now, is around 10s of nanometers. So this started from around 10s of micrometers or 100s of micrometers in 1960s. So along with the reduction in the feature size, the number of components within your chip has also increased. So when we talk about integrated circuits, a famous law that always comes to mind is Moore's law. So this was proposed by Gordon Moore, who is 1 of the co-founders of Intel in 1965.
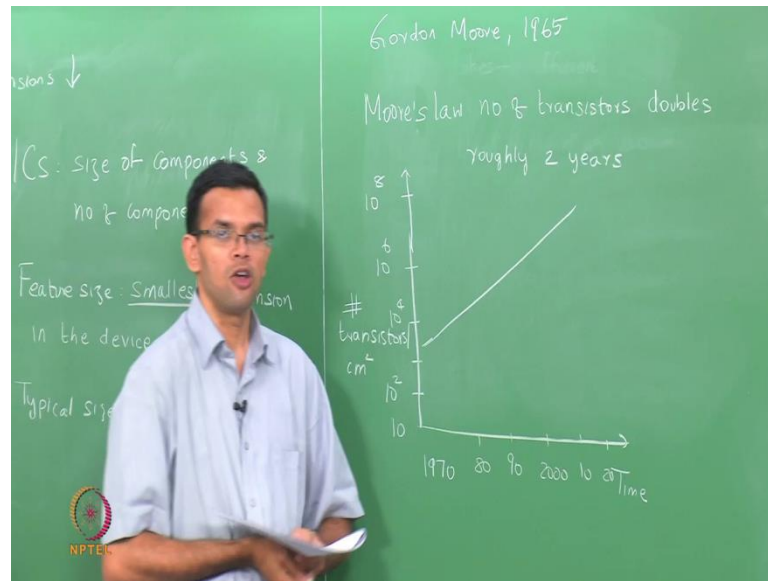
So Moore's law states that, the number of transistors says that, the number transistors on a chip will roughly double every 2 years. The original law had 18 months but, the doubling time is roughly 2 years, the number of transistors doubles in roughly 2 years. So, this was proposed by Gordon Moore in 1965 when the IC industry was just starting up. And remarkably, Moore's law is held for the past 50 years. If, you look at the number of transistors for centimeter square, so let me plot the number of transistors per unit area so per centimeter square, was at time. So this on the y axis it is a lock scale with the 3 4 10 to the 6. Let me just expand the scale a bit; 10 to the 8, starting from 1970 80.
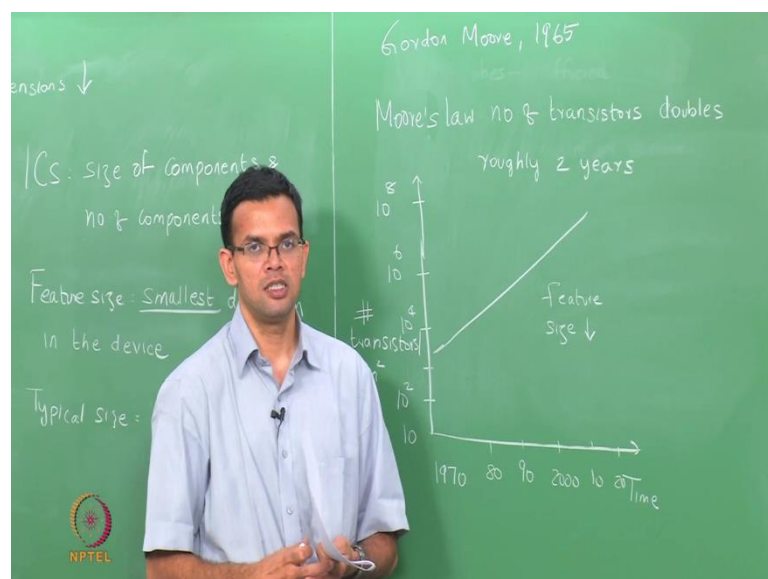
So if you plot the number of transistors was it is time, it is a pretty much a straight line, so it is start somewhere around 10 to the 3 a 1000 transistors per wafer or per chip and it is almost being linear. So corresponding to the increase in the number of transistors, the size of the device have also decreased, feature size has also come down. So we usually refer to the number of transistors on a chip as integration. So they have been levels of integration starting from the 1970's on to today.

So the first one it is called small scale integration, it is called SSI. So the number of components is usually around 2 to 50, so just 10s of components per chip.

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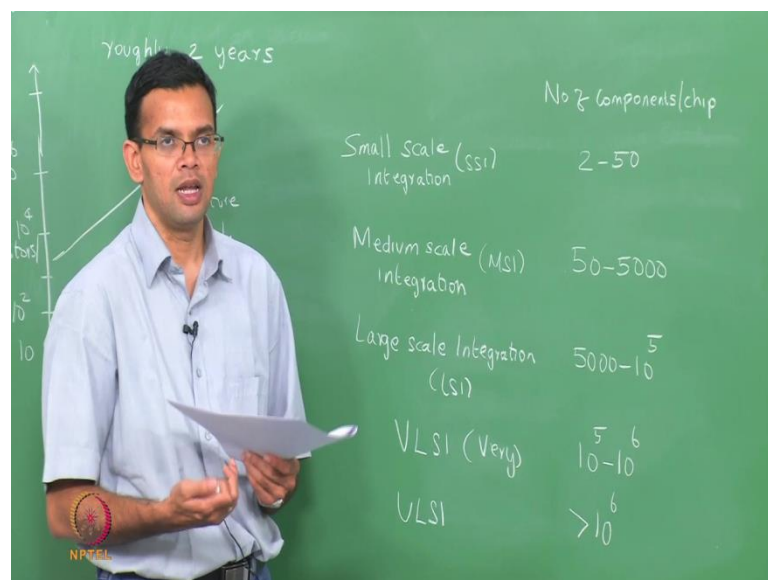
So these components could be transistors, could be diodes, resistors, capacitors and so on. Then we had medium scale integration, let us call it MSI. Now you have a few 1000 components. And note that, as a number components increase, the feature size will also reduce. Then you have large scale integration which is LSI. So from LSI you can go to very large scale integration; so VLSI. It is 10 to the 5 to 10 to the 6. And after that you have ultra large scale integration, where the number of transistors is greater than the 10 to the 6.

So, currently if you look at any of the chips made by Intel, the number of transistors would be above 10 to the 6, it will be close to the 10 to the 7 or 10 to the 8, so you already way beyond the ultra large scale integration limit.

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So let us look at some examples of chips made by Intel and also the component size and the number of transistors. Some using Intel as an example, just to show the evolution of the industry but, whatever is true is for Intel is also true for other semi conducted manufacturers. So we look at the first chip which is 4004. The year of the manufacture is 1971. We usually define called a clock speed, which tells you the frequency of operation of the device. Clock speed is around 100 kilohertz. The number of transistors is 2300 and the technology is called 10 micrometer technology. So 10 micrometers refers to the feature size that may not be the exact feature size but, it gives you an order of magnitude of the size of the component.

So let us jump close to 10 years, will look at 8086. This is from 1978.The clock speed is 5 megahertz, so already by shrinking your component size, you increase the clock speed. The number of transistors is increased; it is now close to 30000, so 10 orders of magnitude increased. And the technology is 3 micrometers, so you have reduced the size of the components. Let us jump on the other 10 years. So you at 486, so is 1989, clock speed is 25 megahertz. The number of transistors is 10 to the 6.

So if you started with medium scale integration, then you went to large scale integration and already you are at your ultra large scale integration. And then technology is 1 micrometer. Then in 2000 you have the Pentium 4. I have not listing all the chips but, only few of them to give you a representative idea. Clock speed is 1.5 gigahertz. The

number of transistors is around 10 to the 7 and your feature size is around 180 nanometers. Xeon which came 7 years later in 2007, it is greater than 3 gigahertz, the number of transistors is doubled and your feature size is 45 nanometers.

So if you look at 45 nanometers and beyond, from there your feature size is shrunk to 32 nanometers and then 22 nanometers. In this case, you no longer have a plainer transistor that is something called finfets or tri gate transistors. And the future plans are 14 nanometer and 11 nanometers. So, the feature size they start at somewhere of the order of micrometers, has shrunk nearly 3 orders of magnitude, then the last 40 years or last 50 years to give you features, there are few 10s of nanometers. So corresponding to this reduction in size, you also have a large increase in the density of the transistors.

So, along with reduction of the feature size, the underlying size of the wafers has also increased. So chips are manufactured on wafers, each wafer can have many 100s or 1000s; now even millions of these transistors. By increasing the size of the wafers, you can make more and more transistors on a single wafer so that, the overall cost comes down.

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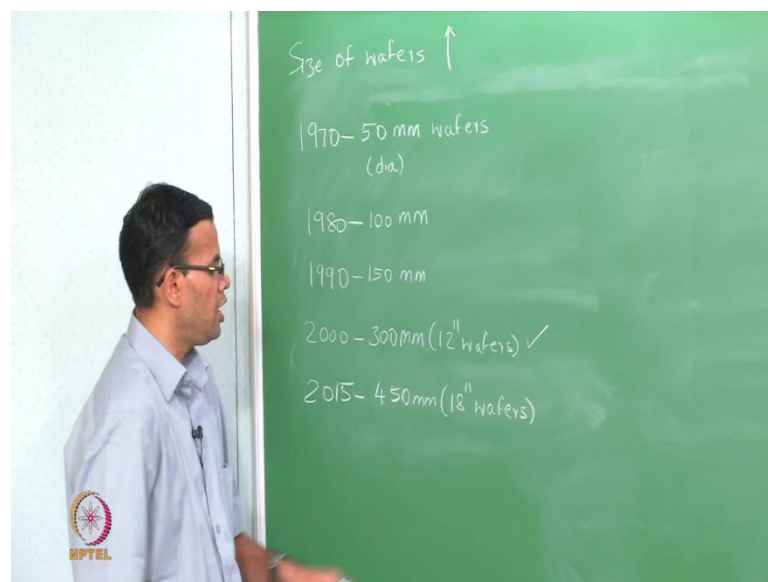
So if you look at the size of the wafers themselves, the size of the wafers has increased. So in 1970, typically 50 millimeter wafers were used, so this refers to the diameter of wafer. Then in 1980 you had 100 millimeter. Then the transition was to 150 millimeters.

In 2000, the transition was again from 150 to 300, if you want to write this these are 12 inch wafers.

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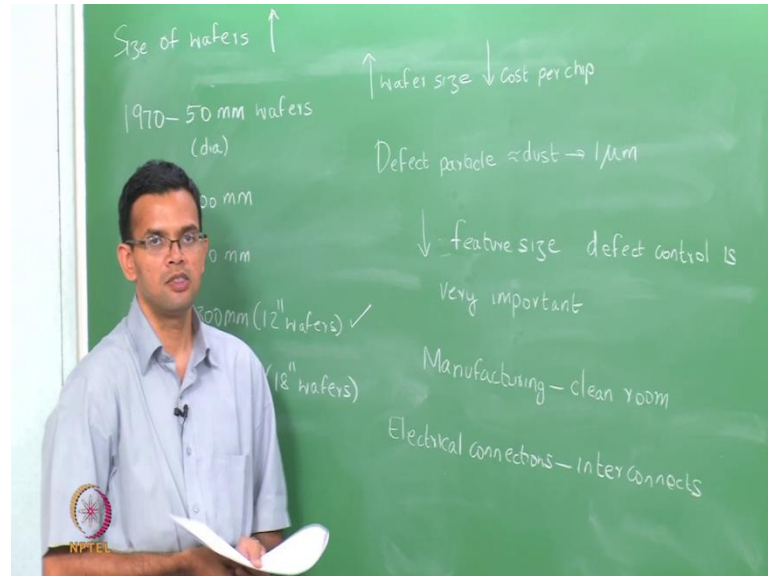
So, 12 inch wafers are what is currently being used in the industry right now. And then the expected transition is from 12 inch to 18 inch wafers or 450 millimeters. So, the advantage of increasing the wafer size is that, the larger the wafers more the number of chips that can be packed into it, which means, cost per chip will come down. So increasing wafer size, then lower the cost. The drawback is that, as we increase the size of the wafers, new equipments has to be manufactured in order to handle the large size. This process is called retooling the fab so that, when you change the size of the wafer, the entire fab has to be retooled, in order to use the larger size wafers.

So, with reducing feature size, controlling the defects in the wafers is also very critical. For example, if you have a defect particle, so this could be a typical dust particle, it usually has a size around say 1 micro meter. If the feature size is 10 micrometers as we saw in the earliest IC a 1 micrometer dust particle is but, with reducing feature size. So, if your feature size is of the order of nanometers a 1 micrometer particle, can essentially destroy the device.

So, with reducing feature size, defect control is very critical or it becomes very important. So if typical semi conducted manufacturing is carried out in clean room, where the contaminants are maintained in very strict control. So later we look at the

different classifications of clean rooms. So clean rooms are classified based upon the size of the smallest of the largest dust particle that is available or found in them. So with increasing or the decreasing feature size, maintaining the environment in semi conductor manufacturing becomes very critical. So manufacturing is done in a clean room.

The manufacturing complexity also goes up as the feature size is reduced. So if you think about transistors, so we can fabricate a lot of transistors on a chip but, these transistors have to be connected to 1 and other and they also have to be connected to the external circuit. So the electrical connections are made and these are called interconnects. So as the size of the device goes down or the size of the individual transistors goes down, the complexity of the interconnects increases.

So, usually interconnects are done in layers. So later when we look at IC device manufacturing, you will see some example how interconnect works but, interconnects is usually done in layers and as a size reduces, the number of layers increases.

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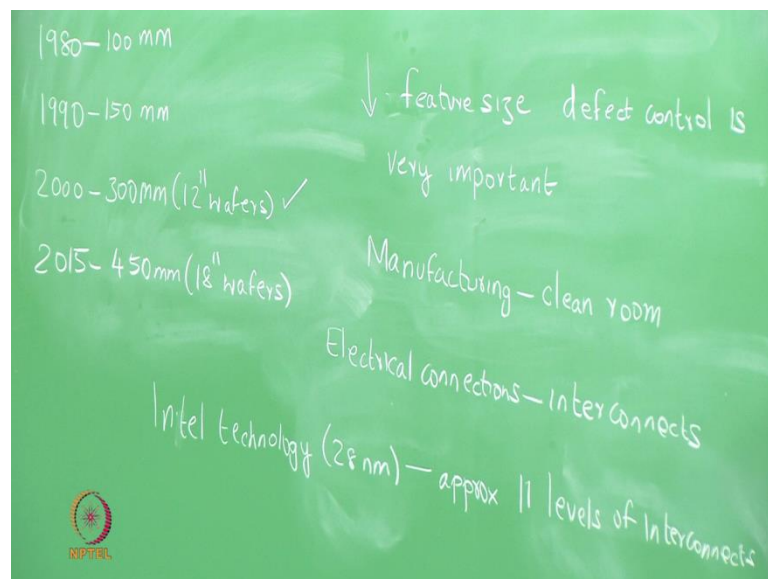
So, if you look at the latest Intel technology, which is the 22 or the 28 nanometer technology, it requires approximately 11 levels of interconnects. As I mentioned earlier, these interconnects not only connect the individual transistors but, they connect different parts of the chip to each other and ultimately they connect the chip to the outside world. So we reduce the size of the components, the complexity of interconnects go up.

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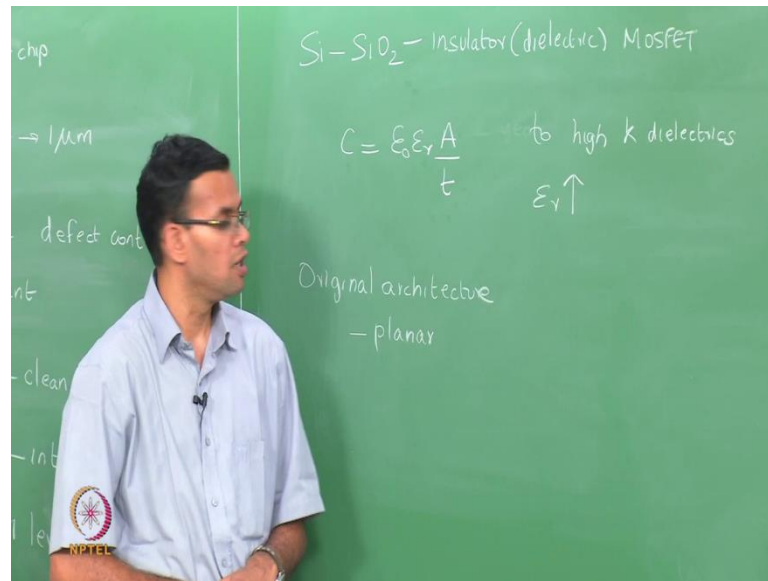
So, how we manufacture all of these on a single wafer again becomes critical, so that, the complexity of process increases. We also have new materials are constantly being used. So for example, 1 of the first reason for using silicon was that, in the case of silicon there is a naturally growing oxide, which is your silicon dioxide that can act as the insulator or the dielectric in your MOSFET. So in this case, the capacitance of the dielectric layer, again you have seen this before is nothing but, epsilon not epsilon not r A over t, where A is the relative permittivity of a device, A is the area and t is the thickness.

So as the device dimensions scale, the thickness also reduces but, if the oxide layer is very thin, then your electrons can basically tunnel through the oxide layer and destroy the channel. So this is 1 of the reasons, why you have transition made from oxide insulators to high k dielectrics, so that, you increase the value of epsilon r. So you increase epsilon r so that, you can have the high capacitance with a comparably thick dielectric layer, so that, tunneling can be prevented.

So we not only have advances in the reduction in feature size but, we also have to look at advances in terms of the materials that are used in your IC device. You can also have advances in the case of the device design itself.

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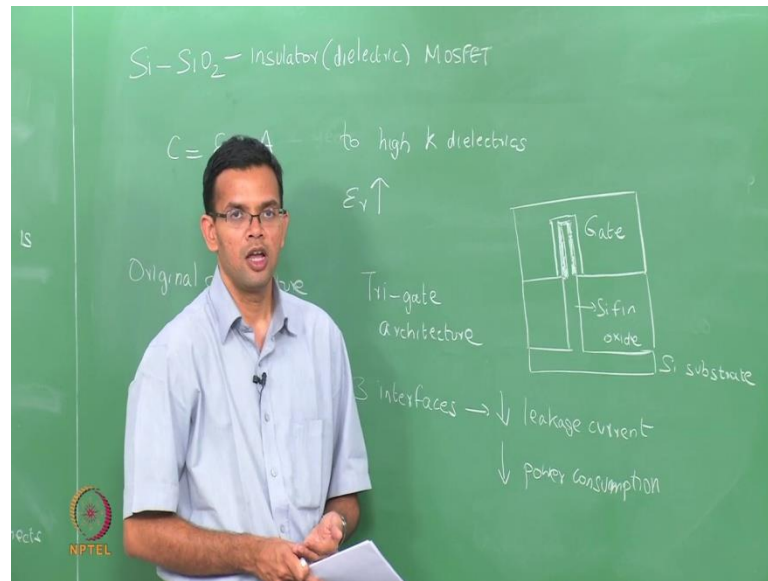
For example, if you look at the architecture of a transistor, the original architecture is plainer. So, in this case you had a source and the drain and a gate region that defines your channel. But, now as a size of the device is reduced, once again a plainer architecture leads to reduction in the signal to noise ratio so with there is a large amount saturation current. So 1 way to prevent that; is to change the architecture. So 1 example of that; is your tri gate architecture.

So in this particular case, you have a silicon substrate but, it is manufactured in such a way, so that, there is silicon fin that out. So there is the oxide layer, which acts as your dielectric material and the gate is wrapped around the silicon fin. So instead of having a plainer technology, you have the 3 dimensional technologies. The advantage is that, in the case of plainer technology, there is 1 interface between the gate and the silicon. But in the case of a tri gate technology, you have 3 interfaces. So this leads to a wider channel and thus improving the current in your transistor. So this reduces the leakage current in the device and correspondingly also reduces power consumption. This becomes very critical, when you are looking at devices for example, chips for mobile phones or rather tablets, where power consumption is critical. So in that case, you have process improvements in order to help your devices better.
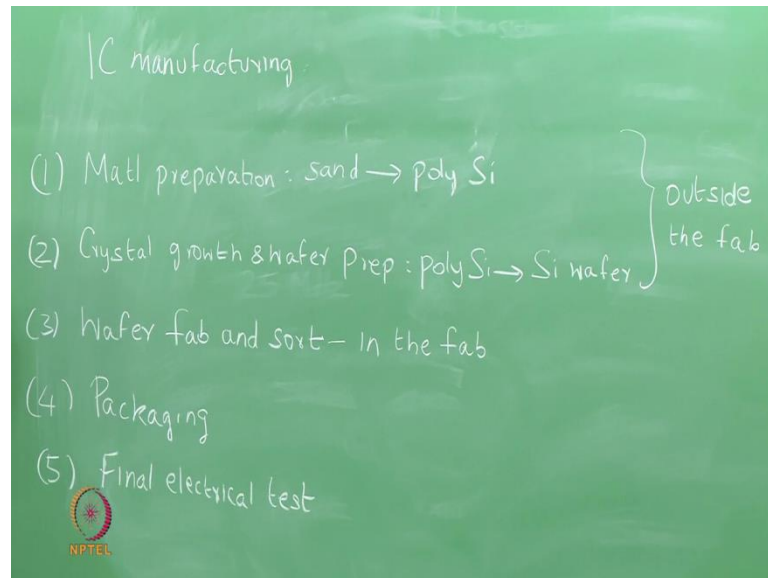
So when we look at IC manufacturing, there were broadly 5 stages we can classify. So if you look at IC manufacturing, so the first step is to get the silicon material out. So we want sand which is your starting material and you want get silicon from it. The first step is material preparation. So converting sand to polycrystalline silicon, I will just write it as poly S i. But, polycrystalline silicon is not what we use in the fab, for using in the fab we need single crystal silicon wafers.

So in the next step is converting the polycrystalline silicon to single crystal, so crystal growth, wafer preparation. So you are converting the poly silicon into your silicon wafer. So these 2 processes take place outside the fab, so that, they act as the input to whatever IC fabrication happens in the fab. So the input to your fab is a bar silicon wafer. So next step, which is the critical step that happens in the fab is; making the IC circuit within the fab and also sorting. So, sorting means once the circuits are made, testing the devices and separating the good and the bad ones. So this happens in the fab. Once sorting is done, the individual chip from the wafer, so given wafer can have 100s of chips. So the individual chips are separated and then they are packaged. And after packaging, a final electrical test is done and then the chips are ready for use.

So, in the next few classes, we will look at all of these stages. So, in next class, we will first start with how we have a S i O 2 as your starting wore and from there how we go to your silicon wafer. Then, we look at the various processes that take place in the fab and

also look at some of the issues and challenges that happen, in the case of silicon manufacturing.