Electronic Materials, Devices and Fabrication
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Lecture No-14
MOSFETS

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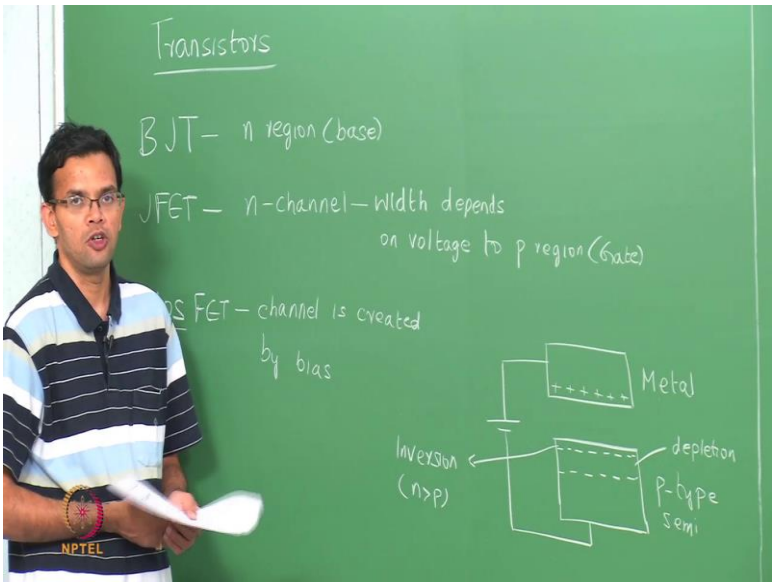

Let us start with a brief a view of last class, last class we started looking at transistors are 3 terminal to junction devices, we first started by looking a bipolar junction transistors BJT. So, in the case of a p n p bipolar junction transistor we had a n region, which was your base through which the minority carriers which are yours holes go, as a go from the emitter to the collector. After BJT we looked at a junction field effect transistor, JFET; the case of the JFET, we already had an n-channel and the width of the channel is control by applying the voltage to the p region.

So, this essentially forms the gate, while we had a source and the drain and the current went from the source to the drain through the n-channel. So, a BJT is a current control device and then a JFET is a voltage control device towards the end of last class, we started looking at a metal oxide semiconductor field effect transistor. So, in this particular case, the channel is not their initially when the devices in equally brim, for the channel is created by applying the bias. So, we show the example of metal oxide semiconductor junction and this case we have, a metal we have a P-type semiconductor.

So, we apply a bias between these to the metal is connected to positive and the P-type semiconductor connected to negative. In this particular case, we have a positive charge on the metal side. Now, there is a negative charge the exchange through the P-type material, not only are the surface, but also some with within the junction, within the a bulk. So, we have two regions; we defined one region, but we called a depletion region, the material still a P-type by the concentration of holes is less than n, which is your accepted concentration and we apply a further bias. We defined a region which is your inversion region; in which case you have, n greater than p.

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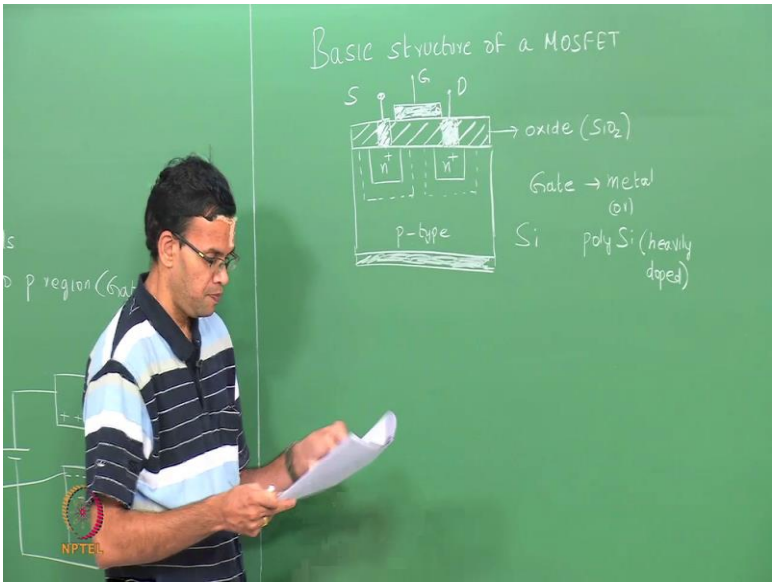

So, that you have a n channel the we created within a your p-type material. So, today we will take up this further and look at a MOSFET, the first thing an going to do is to draw the structure of a MOSFET device. So, that we can look at the I v characteristics. So, let us look of the basic structure of a MOSFET. So, I have my bulk semiconductor material means, still keep it to be P-type. There is a metallization layer.

So, we can form electrical contacts and then, there is an oxide layer on this surface, we have to regions within the MOSFET, which are heavily entire dote n plus. So, these are called the source and the drain and we again make electrical connection to the source and drains. So, let me call then s and d. So, that they are you source and the drain you also

have agate region through which you can a apply of a potential. So, the 2n plus regions form a junction with a p type. So, you have 2 p n junctions, since n plus is heavily dote most of the depletion region will be on the p side. So, this material was silicone.

So, you have P-type silicone and n-type silicone, then the oxide will essentially be Sio 2; the gate material, can eagle be a metal or it can be poly silicon which is heavily dote. So, that, it is conducted. So, we are going to look at how a n-channel is found, in this MOSFET and also the I v characteristics of this transistor. So, let me start by looking at the working of the MOSFET. So, I am going to re draw this figure, but then am also going to make electrical connections between the various terminals. So, you have a source gate and a drain terminal.

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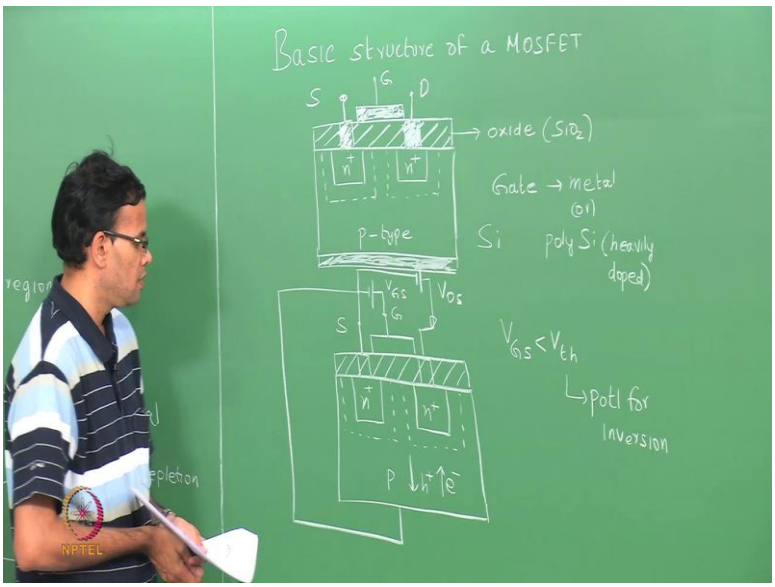

So, let me re draw we going to keep the MOSFET as a same. So, you have a bulk Pa have 2n plus regions. So, a have my source the drain and I have a gate. So, let me just mark them S G and D. So, how do we bias this MOSFET? So, let me first bias the source and the gate. So, on this particular case the gate, is connected to pause to potential and the source is connected to and negative potential. We call this VGs then, I will also bias the source and the drain. So, the drain is connected to a positive potential fresh facts this source. So, we are going to apply a potential to the gate, in such a way that holes will

flow away from the gate towards the bulk of the P-type and electrons will flow towards the oxide layer.

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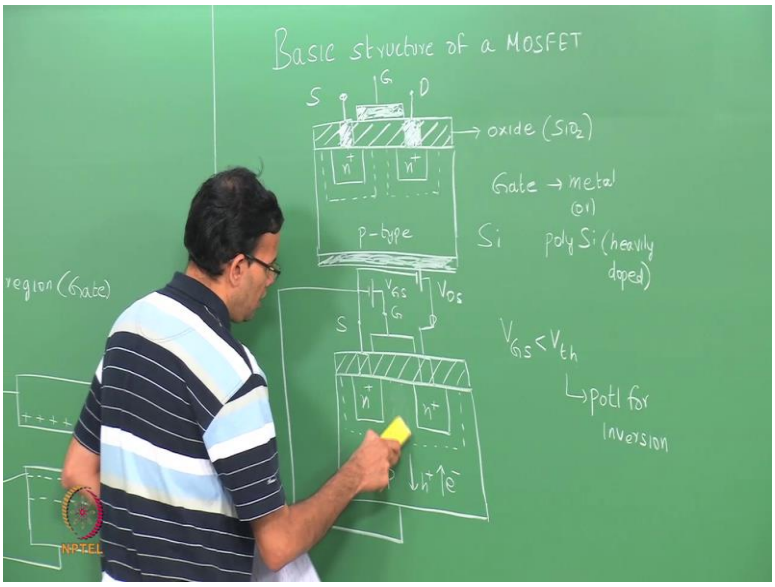

So, we 2 depletion region here where going to bias the material in such a way, that holes will flow down and electrons will flow of, but the potential is lower than the potential that is required for inversion. So, v g s useless than we threshold we show earlier that we threshold is the potential for inversion. So, in this particular case you are going to find that you will have a depletion region here. So, let me just erase this and joined the 2 depletion region together.

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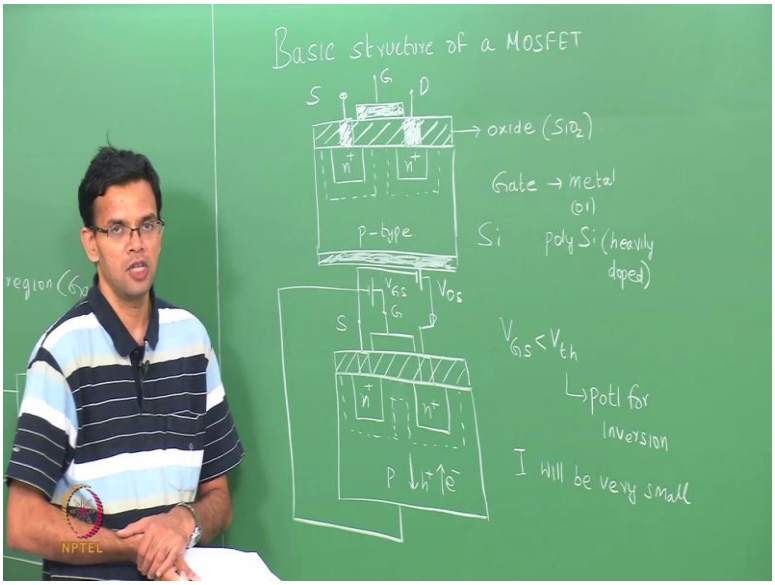

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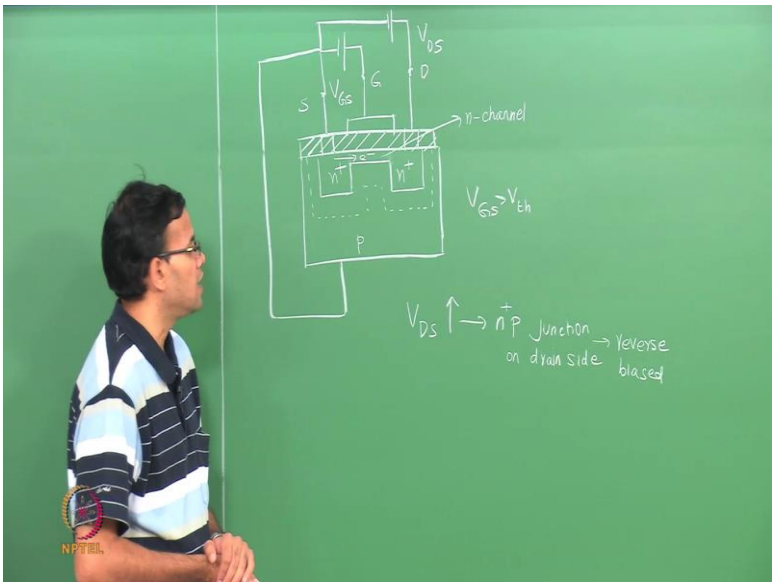

So, we now have a depletion region, but the material is still p-type. So, that electron at still the minority carious. So, current I will be very small and it will be equal to your minority carious flowing in a P-type material. So, it is would be very similar to reverse saturation current. So, as we keep increasing the gate and source voltage, the depletion region is going to increase and ultimately when the voltage is above, we threshold we are

going to form a channel between the source and the drain. So, let me draw that next. So, once again, I have my MOSFET a make to n plus regions a have a bulk p region and a have my gate. So, a have my source my gate my drain this is VGs this is VDs.

So, now, I am in a situation there a have the gate source voltage greater than V threshold. So, that I have an inversion region. So, once again I have a depletion region between the 2 p n junctions, but now I am at a higher potential. So, that I have an n-channel it forms between the 2n plus regions. So, this 1 is a n-channel and the n-channel forms because by gate source voltage is our V threshold. So, now, I can a have electrons flowing from the source to the drain and the electrons flows because, we have a positive potential that is apply to the drain compare to the source.

in the case of MOSFET even not have current conduction when the voltage is below V threshold, but above V threshold. We now, have an n-channel and we have conduction, thus the gate source voltage essentially aces as a controlling parameter in order to control the current in the MOSFET and this essentially is a transistor action, were the voltage between 2 terminals, determines the current or the voltage between other 2 terminals, in also say at this gate was source voltage aces access, which should helps to turn off or turn on the transistor.

Now, what happens as VDs increases, when VDs increases; VDs, is the voltage between the drain and the source. So, as VDs increases, if you look at the Pn junction on the drain site few look at, this P n junction n plus is connected to positive, P is connected to negative. So, that this is reverse biased. So, this essentially means the channels start to get narrower as VDs increases an ultimately above a certain voltage, the channel just gets spins to off figure to draw that.

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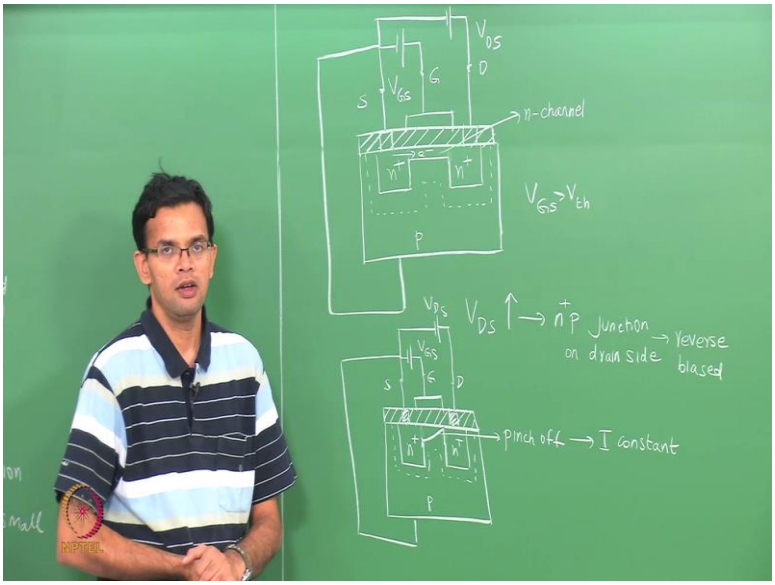

So, again I have my 2n plus regions, I have my bulk p s m o oxide layer and my gate source gate and drain. So, I have my gate source voltage above the threshold. So, that I have an n-channel, but when a start increasing VDs, the channel start to narrow towards the drain region. So, that ultimately you have pinch of to show this, in show the n - channel that is narrow in ask. We approach the drain region shall we have a depletion region that surrounding it, once pinch of acres the current is essentially a constant because the current is determine by the resistance of the n-channel and as long as the pinch of width is small. If will not affect the total current.

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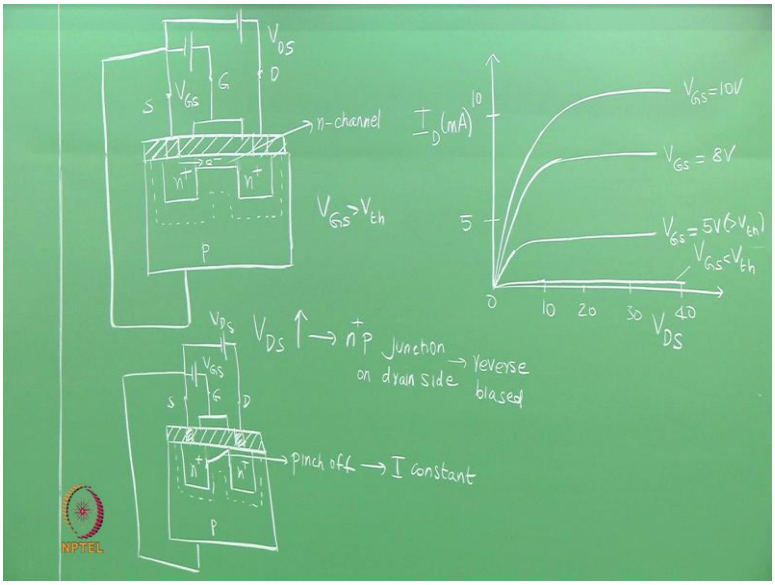

So, in the case of a MOSFET if you put all this information together, we can draw a current was a voltage characteristics will float the current through the channel as a function of the drain source voltage for different values of VGs. So, ID is the drain current. So, this is the current that is flowing from the source to the drain, as a function of VDs, choose the voltage between the drain and the source, if the gate source voltage, is below the threshold value the current is very small.

So, this is a line that is a very close to the access. So, this is as long as VGs is less than V threshold. So, when VGs goes above we threshold. We going to start to see an increase in current, ultimately that comes a point when pinch of acres and the current becomes a constant. So, this is for v g s equal to 5 volts which is greater than we threshold. Now, if we keep increasing the value of VGs, then you going to have a wider channel which means, there will be more current, but eventually there we pinch of this is VGs equals.

So, this is the I v characteristics in the case of a MOSFET the difference between this and the JFET were we show earlier was, there we would shrink the n-channel by applying the potential to the gate. In this case, you increase the n-channel by applying the potential to the gate. So, let us now do some calculations in order to figure out, the width of this depletion region and the inversion region and how that is a related to the doping

level, in your bulk semiconductor. So, will again look at the metal oxide semiconductor junction, and look more closely at the band picture especially band bending. So, let me again go back, to my picture of the metal oxide semiconductor.

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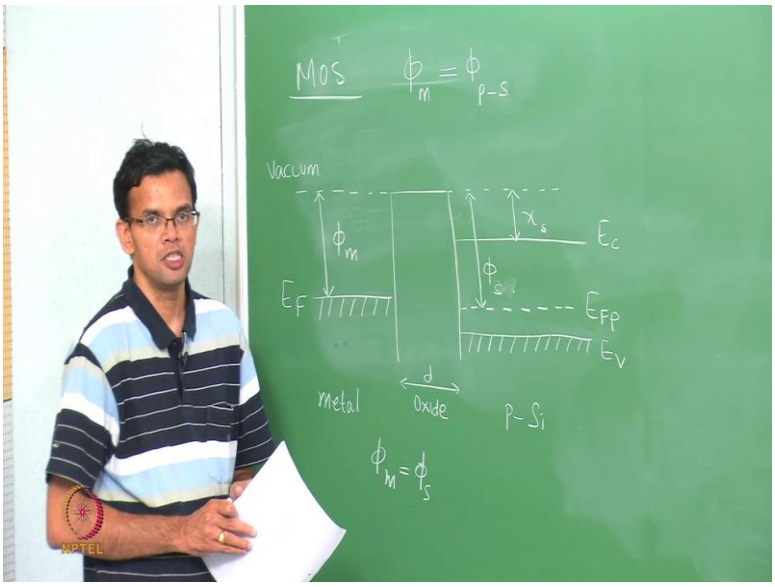

SO, I want to draw band diagram for this, for simplicity and going to say that, work function of the metal, is a same as the work function of the P-type semiconductor. So, instead of silicone, I will just say S. So, the gruesome generalized argument, but we will start with a work functions being to the same. The advantage is that to say, both work functions are the same in the absence of any external potential the fermi levels, you just line up. So, on the left I have my metal, which has a fermi level of EF, the dote would line represent my vacuum level.

So, that psi m is the work function of the metal, I then have a an oxide layer of some thickness D owards the end we will see, what role this oxide or more general and a insulate a place. So, we have an oxide layer and then, I have a P-type semiconductor EFP. So, this is a P-type material. So, the fermi level is close to the balance band this give V. So, for the semiconductor this will be my work function called psi Ps and then, this will be may electron a affinity. So, in this diagram let me just drop the subscript p.

So, I will just call this I. So, we just saying psi n is equal to psi s, but we know that we are starting with a P-type material. So, this oxide semiconductor can be bias and there are 2 way of biasing it, 1 particular way. If you connect the metal to a negative and the semiconductor to positive then, you injecting hole into the semiconductor in these holes will accumulate at the junction, but that is not what we want, we want to bias in such a way that, we are going to have holes moving away from the junction.

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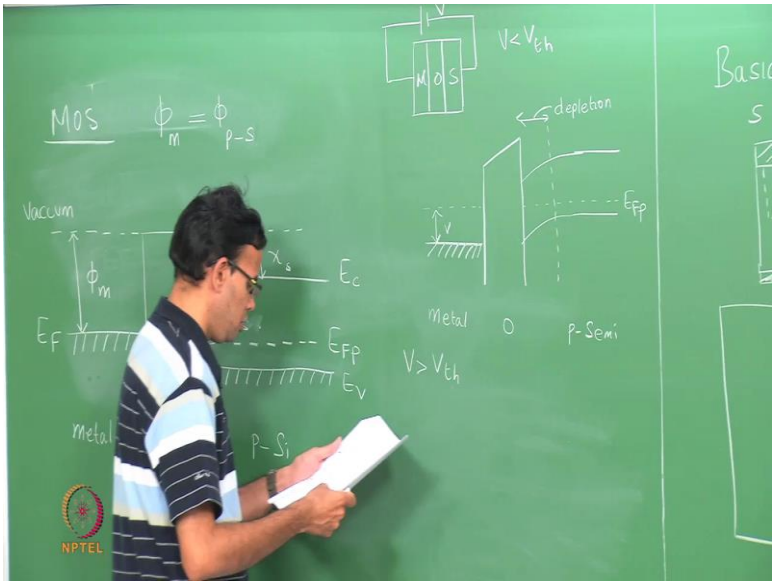

So, we have an n channel. So, let us look at the metal oxide semiconductor at the bias. So, I am just drawing a schematic we going to bias this in such a way that, the metal is connected to positive and the semiconductor is connected to negative, some voltage V. So, few were to draw the band diagram in this case, we are applying and external potential. So, that the fermi levels no longer line up sees my metal oxide and P-type semiconductor. This is the work function of the semiconductor; this is the externally applied potential. So, the fermi level shift by the applied potential, for away from the junction is still have a P-type, but as a go closer to as a junction moving electrons a way. Your material becomes a more and more intrinsic in the depletion region and ultimately in the inversion region you have an a n-type material.

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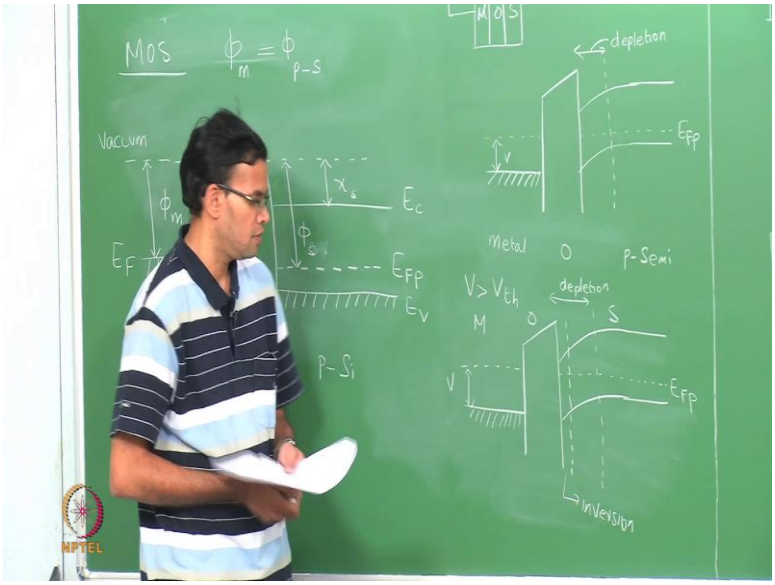

So, you have band bending as you go towards the junction. So, in this particular case V Is less than V threshold. So, that we can define a depletion region, if you have a situation where, we is greater than V threshold your bands have bends so, much; that towards or near the surface, you have inversion. So, if you have a draw that again. So, let me say metal oxide semiconductor, should V this is EFP. So, far away from the junction it still behaves like a P-type. Now, you have a depletion region, but within the depletion region there is another smaller region were n as more than P; so, that we have inversion.

So, this is what happens to the band diagram to case of metal oxide semiconductor, when we try to form an n channel. So, let us look mo more closely at the semiconductor side. So, we can a putting some of these potentials and use it to calculate the width of the depletion and the inversion region. So, we will look only at the semiconductor side of the junction. So, this is my oxide layer, this is my P-type semiconductor. So, let me mark EFP.

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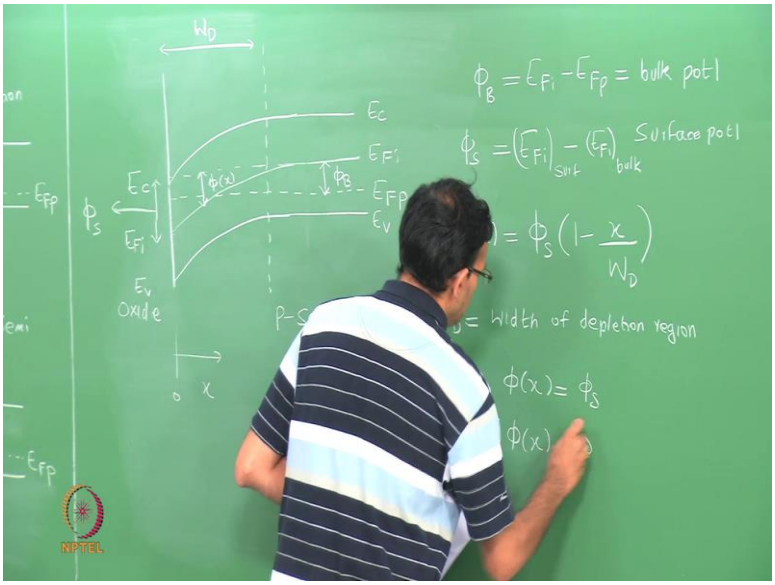

So, EFP; since to P-type will be closer to the valence band this is Ec and Ev; in this diagram let me also mark the intrinsic fermi level, EFI. Now, the extrinsic fermi level as you seen earlier is very close to the center of the band gap, it is not exactly a center cause a effective masses of the electrons in holes are different, but it is very close to the center. So, we also have drawn EFI that, gap between EFI and EFP. I am going to call phi b which is the bulk potential. So, let me call this phi b, phi b is nothing but, EFI minus PFp. So, is the bulk potential? So, now, we have applied a potential such that, you have an inversion layer at the surface and you also have a depletion layer.

So, I will also draw EFI; so, this is Ec Ev and EFI. So, in this case we can also defined a surface potential psi s, I will call surface potential which is the difference between the intrinsic fermi level in the bulk and the intrinsic fermi level in the surface. So, phi s is EFI at the surface minus EFI.

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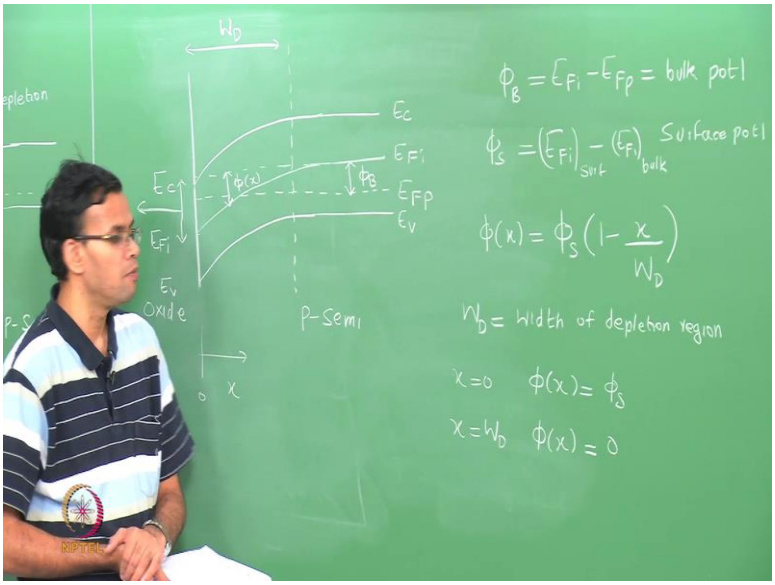

The bulk if I were to draw this let me just draw a dotted line. So, that this is phi s. So, we have a bulk potential, we have a surface potential, we can also define the potential at any distance x from the surface. So, in this particular case, the surface is taken as 0, and x is the distance as we go into the material. So, phi as a function of x is nothing but, phi s minus x over WD, where WD is the width of the depletion region. So, WD is the width of the depletion region. So, x is defined from the surface. So, that when x 0 psi of x is just surface potential and when x is equal to WDx is equal to 0.

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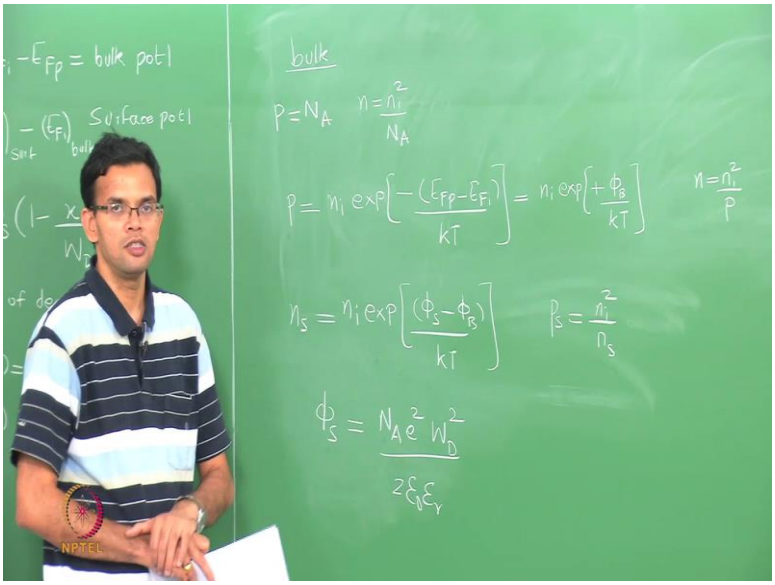

So, WD Represent the start of the band bending because, where is a measure of how much your intrinsic fermi level has shifter because of band bending. So, let us now relate these potentials to the concentration of electrons and hole in the semiconductor. So, within the bulk of the semiconductor P is equal to NA, which use our accepted concentration n is just be ni square over NA. We can also relate the position of P mean the position of the fermi level to P and if you were to do that P is nothing but, ni exponential Is ni exponential minus EFP minus EFI over kt.

So, this we have seen before EFP minus EFI is nothing but, the bulk potential. So, this is ni exponential minus phi b over kt or actually this should be plus phi b cause it is minus EFP minus EFI, which is minus phi b such plus phi b over kt same way at the surface we can also define a concentration of electrons and holes. So, few were do that ns. So, the concentration of electrons the surface it is again related to the position of the Fermi level.

So, ni exponential and this we can simplify to include the surface potential and the bulk potential such exponential phi s minus phi b over kt. So, that it is a difference between the surface potential and bulk potential or in other words, how much the Fermi level has shifted with respect to the intrinsic Fermi level Ps. We can just calculate from ni square and the same way here ni can calculate from just P this value of phi s.

Depends upon the concentration of a acceptors within the bulk p type material. So, we can relates phi s to the bulk concentration and also the width of the depletion region if we do that phi s is just related to NAe square WD square by 2 epsilon not epsilon not r.

So, this we can get the assuming the certain distribution of electric charge within the depletion region and thus calculating the electric field and linking that to the potential. So, we have done a calculation for this, when we will look at the P-n junction. So, the argument here is also similar. So, we can relate phi s which is just. Surface potential to NA which is the concentration of acceptors within your P-type semiconductor; in also WD, which is the width of the depletion region, in the case of a MOSFET we have inversion.

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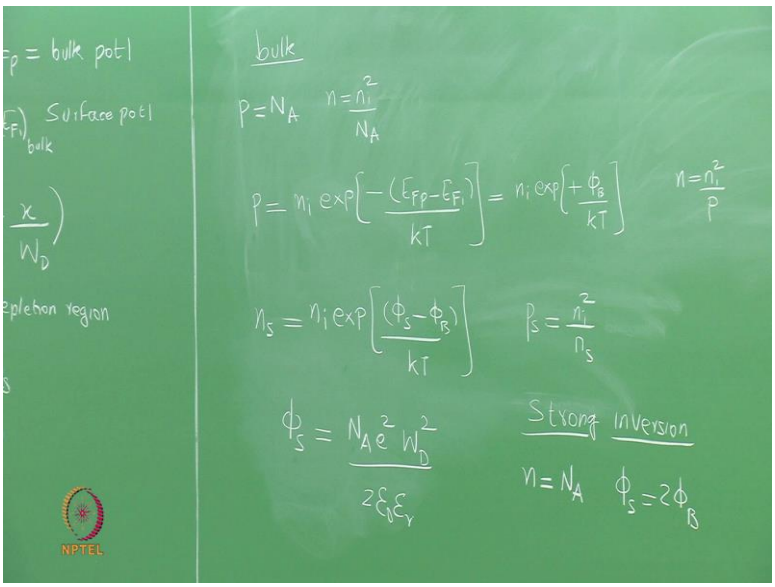

So, that we have an n-channel that is created we define a condition call strong inversion. In the case of strong inversion we create an n channel were the concentration of holes i am sorry the concentration of electrons is equal to NA. So, that we create a channel that is as strongly n-type as the bulk materials is P-type. So, when we have strong inversion an n is equal to NA, phi s will be just twice the bulk potential. So, this we can understand because phi b is a location of the Fermi level with respect though the intrinsic Fermi level.

The case of P-type this Fermi level is located below EFI and now, if I make it n-type the Fermi level goes about EFI and when, n is equal to NA the lo distance of the Fermi level from the intrinsic will be the same. So, its start phi b below EFI and when becomes n-type it becomes phi b above EFI. So, that the total potential is just 2 times phi b. So, this is a particular case, of inversion and it is call strong inversion. So, we will equate this in order to calculate the width at strong inversion.

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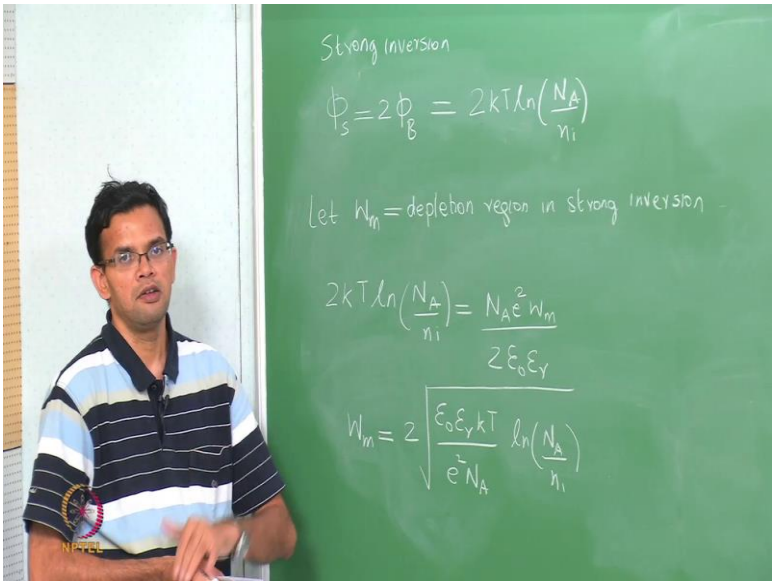

So, we have a case of strong inversion that phi s 2 times phi b; this even is related to the concentration of the acceptors laun NA over ni, we also saw and expression relating phi to the width of the depletion region. So, let Wm view the width of the depletion region in strong in version. So, in this particular case 2kT laun of NA over ni is related to NAe square WM over 2 epsilon not the epsilon not r is related permittivity of a semiconductor; can rearrange this to get to get the width of the depletion region that is just 2 square root of epsilon not epsilon rKT over E square NA laun of NA over ni.

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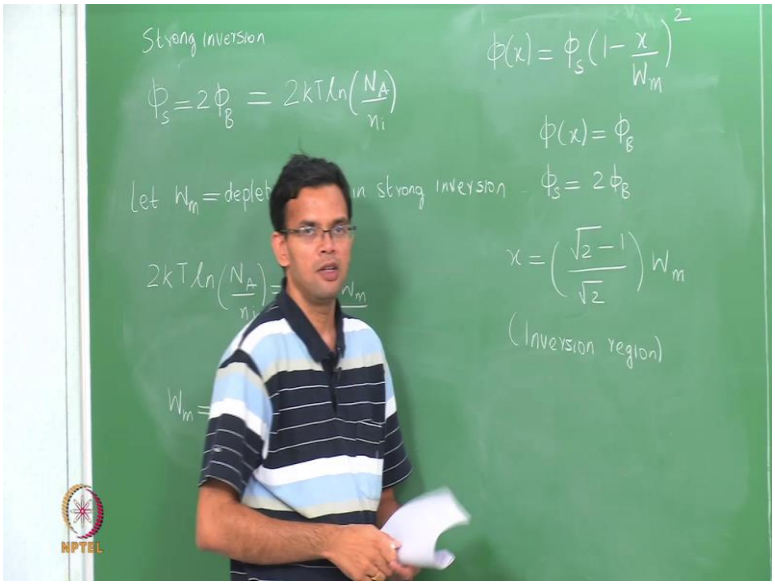

So, this equation gives the width of the depletion region. So, the total width when we have strong inversion and this is related to the concentration of acceptors within the material. We also wanted to find the width of the inversion region, the depletion region is both the inversion and the other region were we have p greater than n, but less than n a in order to that, we start with this expression phi of x minus x; and now, I am looking at a condition of strong inversion. So, I will put WN hole square will define the inversion region as where phi of x is equal to phi b. Remember the surface potential is 2 times phi b.

So, we can put this values here and simplified to get x equal to 2 minus 1 divided by root 2 times Wm. So, we can calculate both the total width of the depletion region. So, just given by this formula and the width of the inversion region. Let us, actually substitute some values, in order to get a sense of these numbers. So, I have P-type semiconductor and going to tech silicon with NA to be 10 to the 17th for centimeter cube.

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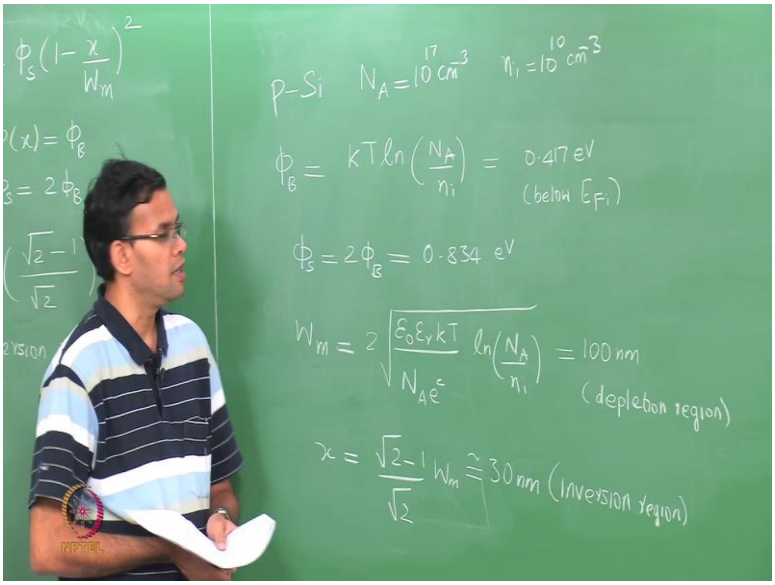

We can first calculated the bulk potential, which is the difference between the Fermi level in the intrinsic material and the Fermi level in your P-type that is nothing but, kT laun of NA over ni. If you have silicon we know that, ANI is 10 to the 10. So, that this gives you a value of 0.417 electron volte and this is below EFI. So, now, we want to create an n-channel in this P- type material and we want to make it strong inversion. So, that the material is as much n-type as the bulk is P-type.

In order to do that, we need to have a surface potential phi s were as 2 times phi b this is nothing but, 0.834 electron volts we also wrote down an expression for the total width of the depletion region. So, we can substitute the values here in that gives fy n to be 100 nanometers. So, this represents the total width of the depletion region. So, we want to calculate the width of the inversion region see is x; in this 1 approximately 30 nanometers. So, this 1 which is 100 nanometers which is Wn is the total width of the depletion region within this depletion region you have an n-channel.

So, inversion region this is approximately 30 nanometers wide, if you increase the value of NA. So, you make you material more P-type the total width of the depletion region will reduce corresponding the width of the channel will also reduce. So, 1 last thing before we look a before we end the MOSFET, the oxide layer in the case of a MOSFET

axes as an insulated.

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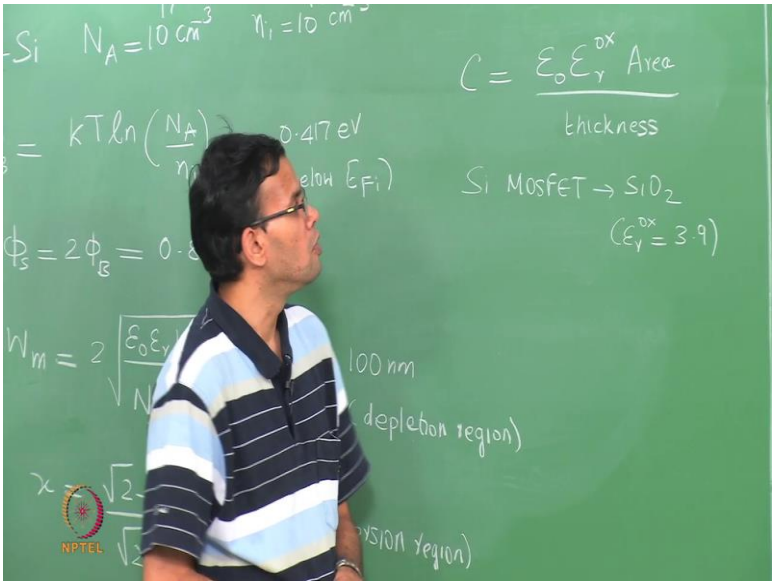

So, we can defined a capacitance for the oxide layer or for the MOSFET and the capacitance is nothing but, epsilon not epsilon r oxide trains area divided by the thickness of the oxide layer. In the case, of the IC industry silicone is a material of choice for the MOSFET. So, the oxide layer the disuse always Sio 2; an Sio 2 has a relative permittivity of 3.9. Now, as the dimensions of the transistor start to come down. So, this is a scaling, were have more transistor fat within given AIC as a dimensions starts to come down the dimensions of all the other components of a transistor there will also have to come down. So, as the thickness reduces the capacitance will be increase, but we your thickness becomes too small the oxide layer is very thin.

So, that you can have tangling between the made metal layer, which is your gate and the n-channel and this will affect the properties of the channel; In order to prevent that the oxide layer is replaced by other high cade dielectric material s. So, we can still have a reasonable thickness while at the same time having a higher capacity. So, we replace the silicon dioxide, the other material s with a higher epsilon not r.

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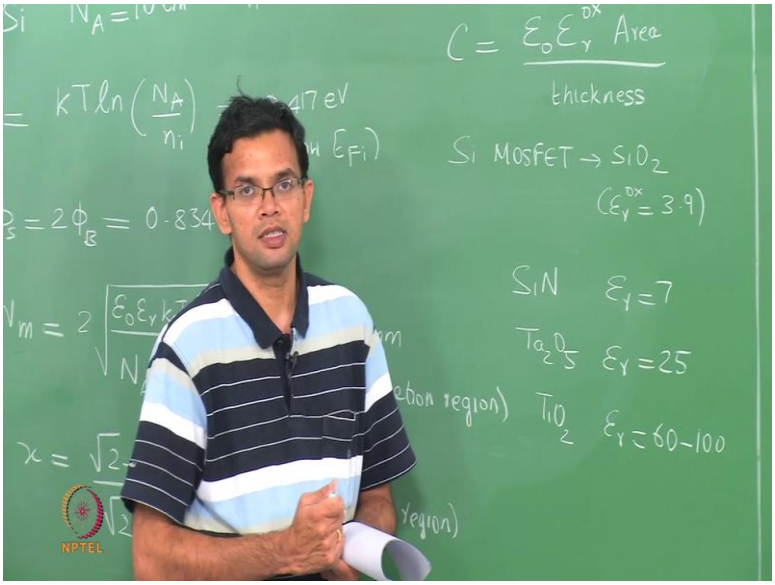

So, some of the other material s are used is silicon nitride, with earlier to permittivity of 7, but metal oxides are also used. So, tantalum oxide is 25 titanium oxides, is any way from 60 to 100. So, in the recent IC industry we replace the metal oxide semiconductor with an insulator that has a high dielectric value, with this we are done with the MOSFET part of the course, in the transistors is well; next we will start to look at what happens, when light interacts with yours semiconductors. So, we are going to look at of to well electronic devices like LED in solar sense before we that, you will first treat the general instruction of life with semiconductors.

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