Electronic Materials, Devices and Fabrication
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Lecture - 18
Transistors

Last couple of classes we have looked at p n junctions. A p n junction is two terminal devices we have one terminal on the p and one terminal on the n and it is the single junction that is the interface between p and n. Today, we are going to start looking a transistor.

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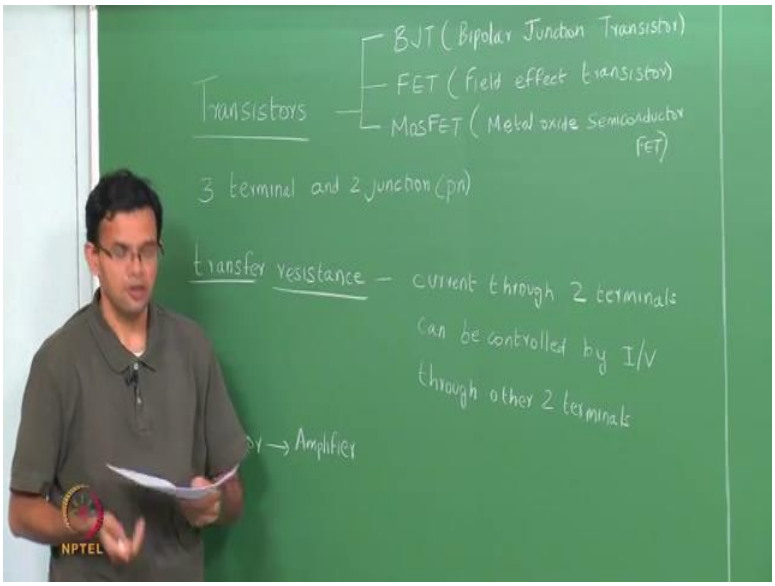

A transistor is a three terminal and two junction devices. When we mean a junction here, we mean a p n junction, so that we have two p n junctions in the device. The name transistor comes from the term transfer resistance. This means that the current through two terminals can be controlled by controlling the current or the voltage through other two terminals controlled by either the current I or the voltage through the other two terminals.

When we look at examples of transistors, this point will be make clear. A transistor can also act as an amplifier, in that you can take a small signal between a pair of terminals and then amplifier. So that the output signal between another pair of terminals is higher.

So, we will have first start by looking at bipolar junction transistors, so we will first start

by looking at BJT. Which is your bipolar junction transistor, from there we will move onto field effect transistors and then finally, a specific type of field effect transistor called a MOSFET metal oxide semiconductor field effect transistor conductor FET.

So, we will start with the BJT then go on to FET and then MOSFETs. So, we will spend most of the time looking at MOSFETs, because MOSFETs are what are used the current I C industry, but we will talk about the other two, to form the basis of understanding MOSFET. So, let us start by looking at a bipolar junction transistor.

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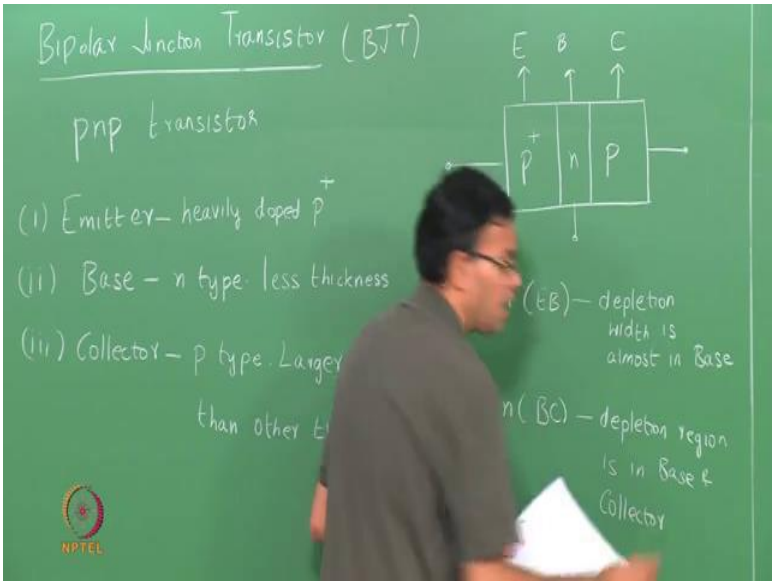

So, we will first start with example of a p n p device, so you have three regions you have two of them are p type. Then you have a central region that is n type so we have a p n p transistor. So, there are three differently doped regions in this transistor. The first region is called the emitter, it is usually heavily doped, in this case it is heavily doped p plus. We then have a base, the base here is n type, p n p so n type. The base usually has a lesser thickness compare to the other two regions.

And then finally, we have a collector. In this case the collector is also p type and it usually has a larger width or larger thickness then the other two regions. So, five way to show a schematic of a p n p transistor, I have an emitter region that is p plus, I have a based region that is n and I have a collector region that is p.

So, I will mark this E to mean the emitter, this is your base that is the collector. So, we have two junctions, one junction between the emitter and the base, one junction between

the base and the collector and you have three terminals. So, this makes your transistor, a three terminal, two junction device. So, if we look at the two junctions, the first junction is your p plus n, which is your emitter base. So, the p region is heavily doped, so that depletion width is almost entirely in the base.

You also have the junction between the base and the collector which is simple p and n. In this case, the depletion region is in both the base and the collector, so is in the base and the collector. So, there are various configurations, in the case of a p n p transistors, how we connect this different terminals. The first configuration we are going to look at is called a common base, this case the base is common between both the emitter and the collector.

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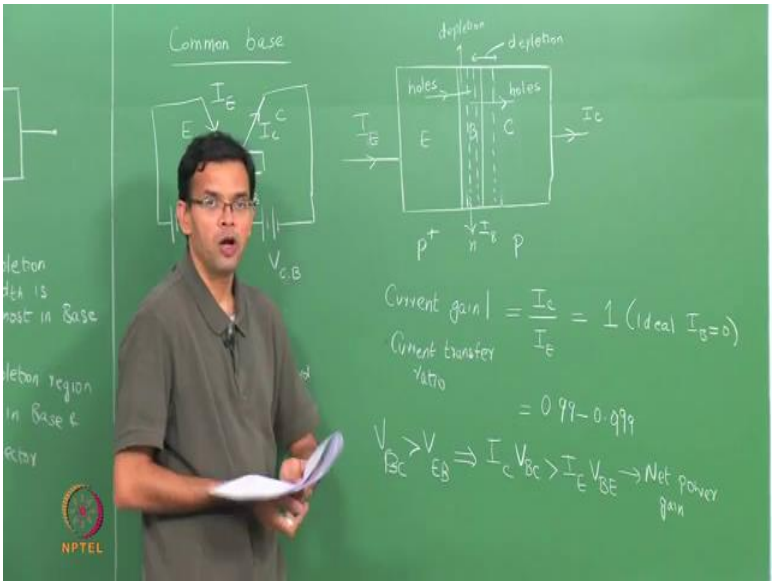

So, let me draw the electronic the configuration for the common base. So, this is the base, you have an emitter and you have a collector, so the emitter base junction is forward biased and the collector base junction is reversed biased.

This is C. So, this is the emitter based junction that is forward biased and then you have the collector based junction. So, in this particular example V CB is greater than V EB. So, let me just write down this is forward biased and this is reversed biased. We can also define three currents. One is an emitter current I E, then you have a base current and then finally, you have a collector current.

So, how does a p n p transistor work, let me again draw a schematic of the transistor, in

this I will also mark the depletion regions. We just redraw this, so I have three regions the emitter, the base, and the collector. So, the emitter is p plus, the based is n, and the collector is p. So, the emitter based junction you have a p plus and then n.

So, the depletion width is also entirely on the base side, on the other hand the base and the collector the depletion width is in both regions. So, we have two junctions which is why you have two depletion regions. So, we have the emitter current, we have the base current then we have the collector current. The emitter base junction is forward biased, so we have holes that are injected from the emitter in to the base.

So, these holes then goes through the base where there are minority carriers cause the base is n type, but the width of the base region is very small. Some of these holes can get these combined so they form the base current, but a majority of the holes go through the base and then go to the collector which is revised biased. We have holes go through the base and they form your collector current. So, we have a based emitter current that is because of the injection of holes. Some of these holes recombined in the base region they form the base current, and the remaining holes that go from the base to the collector constitute the collector current.

In the case of bipolar junction transistor, we can define a current gain. Another name for it is also current transfer ratio. This is nothing but the ratio of the collector current to the emitter current. Now in an idle case, if no holes are lost in the base due to recombination this current gain should be equal to one. So, this is if it is idle and there is no based current, but usually some of the holes will always be lost in the base due to recombination.

So, this current gain typically is around 0.99 also be up to 0.999. So, the current gain defined, defends upon the thickness of the base region, so typically we want a very thin base so not many holes are lost due to recombination. Instead of a p n p we had np n transistor the argument is entirely is the same expect that here you have injection of electrons instead of holes.

The transistor action here arises because there is a net power gain because we said V BC, which is your base collector voltage, is higher than V EB, which is your emitter base voltage. So, if we look at the net power, power is nothing but the voltage into the current. So, you have I C that is grater then the emitter V BE, so you have a net power gain, your

transistor. So, in this particular mode, we operated the BJT in a common base configuration. Let us look at one more configuration, we look at the configuration where we have the emitter being set as common.

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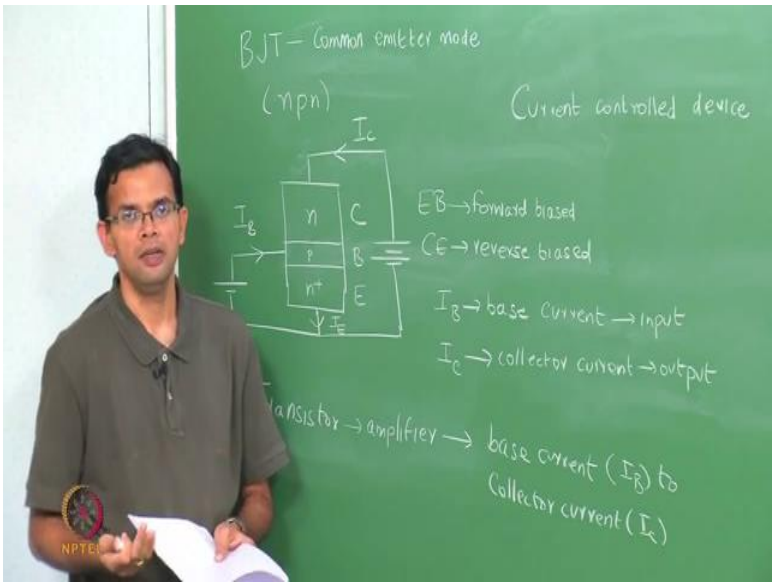

So, now you have your bipolar junction transistor, but it is in common emitter mode. So, if we redraw this and just for example, I will chose an n p n transistor instead of p n p. So, in this particular case I have an emitter that is n plus that is my emitter, I have thin base region that is p type and then have a collector that is n type. So, in this particular case, I have the emitter base to be forward biased and I have the collector base. So, in this particular case I have the emitter and the base to forward bias and I have the collector and the emitter because it is a common emitter mode to be reverse biased. In this particular case I B which is the base current is your input, and I C which is the collector current is the output.

In common emitter configuration is easy to see how your transistors act as an amplifier, the base current typically very small while collector current is much larger, this almost equal to the emitter current. So, you are taking a very small current and then amplifying it into the collector current so that your transistor works as an amplifier. So, it takes the small base current and gives out a larger collector current.

So, a bipolar junction device is essentially a current controlled device. So, we can say that the current from the emitter to the collectors, so I E and I C are control by a base

current, but overall it is a current controlled device. The next thing we are going to look at is, your field effect transistor, we are going to look at a junction field effect transistor.

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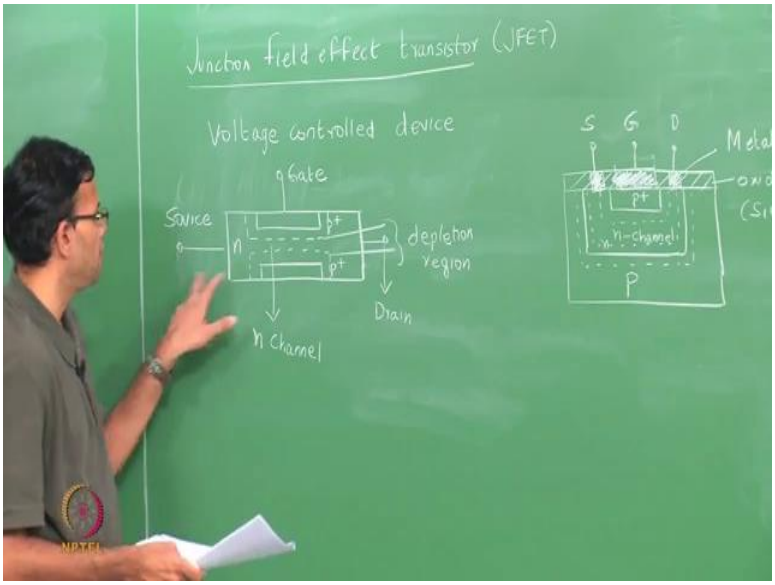

So, we are going to look at a junction field effect transistor called it JFET, so both the JFET and the MOSFET which is what we look after this our voltage controlled device. So, let me draw a schematic of a JFET. Remember once again we need two p n junctions, also need two terminals. So, in this case I start off with an n type material, I have to heavily doped p type materials or p type layer in this n.

So, both of these are heavily doped p, so I am going to called them p plus, so because they are heavily doped and we have a p and n we have p n junction and the depletion width is almost entirely on the n side. So, if I were to draw my depletion region so the dotted line represent the depletion region and between the depletion region you have an channel.

So, we can again define three terminals, you have one that is called a source you have one that is connected to the p plus it is called o gate and then you have drain, you just mark it here is drain. So, you have a source, you have a drain and then you have a gate. The more practical way the device you look. I will just draw that. So, I have a p region, within the p region I define a n regions. And then again I have another region which is heavily p plus. So, we can define three terminals usually there is an oxide layer on top. So, if your material is silicon which is almost always the case.

The oxide is S i O 2, so we can form the three terminals, one is your source, then you a gate, gate is here then you have your drain. So, the shaded regions essentially mean metal so that you have a good contact with your semi conducted, so I will just say a metal conductor. Once again in the device, you have two depletion regions, so you have two junctions one between the p plus and the n, one between the n and the p so that you have to depletion regions and you have n channel.

So, this schematic represents more of how the actual device will look. This particular diagram something that I am using in ordered to explain the functioning of a JFET. So, we will use this to explain how the current and voltage behavior works, but please keep it in mind more practical device will have a different schematic. So, will consider the behavior of JFET, so once again you have a current between a source and the drain, and this current will depend upon the voltage that is applied the gate. So, that is your transistor action where the current between two terminals depends upon the voltage or the current between the other terminals. So, let us first look at the current between the source and the drain when your gate is short circuit.

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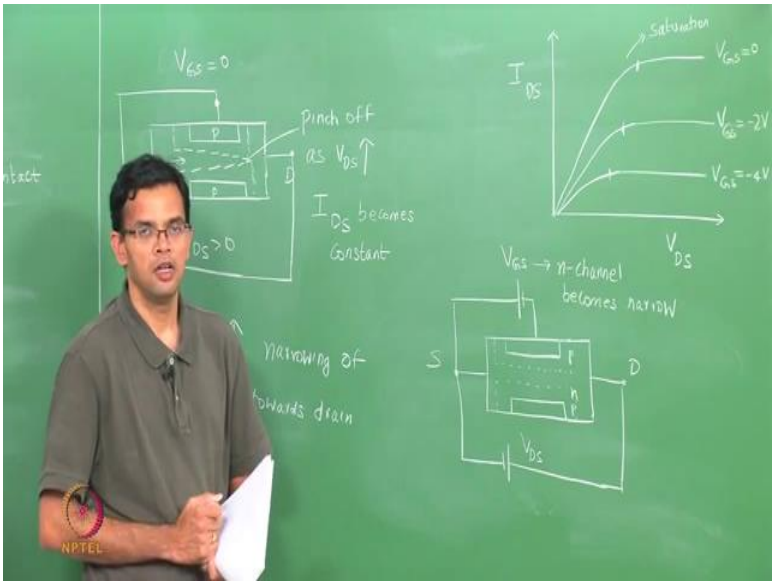

So, let me redraw the schematic of the device. So, you have a source when you have a drain that is my drain that is my source. I have my two p regions this is n, so I have my two p regions so that I have my two depletion regions and then I have my n channel. So, we are going to apply a biased between the source and the drain.

So, I will biased the drain positive with respect to the source, let me called this V DS this is greater than zero, which means the drain is biased positive with the respect to the source so that electrons can move from the source to the drain. Electrons can move and this constitutes your current. We will also set the gate at zero a potential, so that V DS zero, the gate is at zero potential. So, as we start to increase this value which is your drain and source voltage, we are going to have a current, keep on increasing the value there is going to be more current.

But, if u look at the two junctions, as we increase the value of the drain source voltage, there is going to be narrowing of the n channel. This is because this drain is reversed biased with respect to the gate so that as V DS increases. There will be narrowing of the n channel towards the drain, narrowing of the n channel towards the drain. So, I will just show the schematically of the same figure.

So, that if you looked at the channel, the channel is wider near the source and start to narrow near the drain. If you increase the value V DS further there is going to be further narrowing until both depletion region meets in which case we will have pinch off region. We can show that schematically on the same plot, so that your n channel is essentially pinched off hear at high values of V DS. When pinch off occurs, the current through this device essentially becomes a constant because it depends upon the resistance of n channel, this is again assuming we have a pinch off region that is small in width.

So, when one's pinch off occurs, the current I between the drain and the source so I called I DS become the constant. We can plot and I V characteristic for this a JFET if you do that. I have current so I DS, which is the current between the drain and the source, verses V DS. So, it is again the voltage between the drain and the source. Right now I am shorting the gate, so that the gate and source voltage is zero.

So, as you increase the voltage initially your current starts to raise because we have electrons going from the source the drain, but as currents starts to raise and voltage increases the width of the channel will also decrease and ultimately you will have pinched off and when that occurs the current is constant. So, your I DS initially increases until pinch off occurs and then current is constant.

So, this value where your pinch off essentially occurs is your saturation, in this plot is when your gate and source ((Refer Time: 34:20)), so that there is no bias between the

gate and the source, so what will happen, we now when have bias between the gate and the source. So, let me redraw this and introduce bias between the gate and the source. So, have again my n region, I have my two p regions, that is my drain that is the source and drain is positively bias with respect the source. And now I am going to bias the gate negative with respect to the source V GS.

So, when do this we now again you have depletion region, but if we look at the gate and this source gate is reverse bias repeat the source so that the depletion region is higher or other words the channel is narrower. So, once you have a bias the n channel becomes narrow and if we keep on increasing the value the channel will become narrower and narrower. What does it means? Is that if you plot you I V characteristics are going to find pinch of become issue her higher this between voltage in gate in this source.

So, we were to plot, so this is for V GS equal two zero. We have other value, V GS is minus two volts, once again your current for saturation is lower because you have a narrower channel and also the saturation occurs earlier. If you increase the voltage even more, so V GS minus four volts the current again go down and saturation also occurs earlier. So, in this particular case which is your JFET you have a situation where the current between source and the drains is depend upon the width of the n channel is expect by the voltage between the grace, the gate in the source V GS. So, higher that voltage smaller is the width of the channel and then lower is the current.

So, this again an example for transistor action where the current between two terminals is affected by the voltage between the other terminal. This is an example of JFET, so where you already have a channel that is created with in the materials.

The next thing we are going to look at is a MOSFET, so we have a metal oxide semiconductor which creates your n channel. So, the metal oxide semiconductor filled effect transistors are what there are commonly use the current micro fabrication industry. So, before we understand MOSFET s, let us just look at the metal oxide semiconductor junction and see how we form the channel in that particular case.

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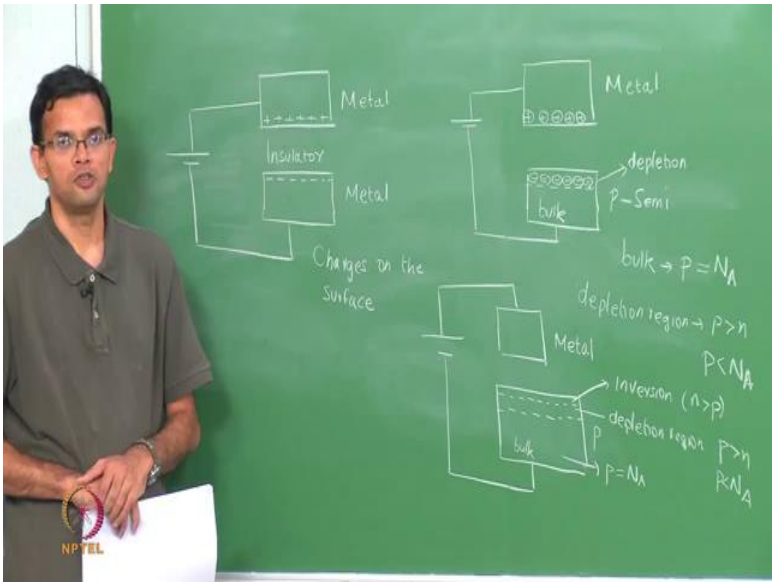

So, right now we only look at this part once we understood that you will put it together in order to look the MOSFET. So, consider a parallel plate capacitor form between two metals. So, you have metal one, you have another metal plate and then you apply a potential.

So, between the two metals you have an insulator so this insulator could be ((Refer Time: 39:44)) or it could be an oxide layer or some other layer which act as an insulator. So, you have two metal pleat connected to a potential, this case you have positive charge on one pleat and negative charge on the other so this act as a capacitor, and since these are metals the charges will reside on the surface. So, let me first take this device or let me take this arrangement and replace one of the metals with a p type semiconductor. And I have a metal and inside of the other metal I have p type semiconductor.

So, once again there is an insulator layer between this two, connect the metal to positive and the p type to negative. So, we have a positive charge on the surface of the metal, but the charge density in the case of the semiconductor is lower. So we have seen this example earlier in the case short key junctions so you have an negative charge on the semiconductor, but it is not only at the surface but it also extends a small distance into the bulk. So, in the case of a semiconductor we have a depletion region and then we also the have bulk.

So, within the bulk of the semiconductor it behaves as your regular n type, so p is equal

to N A, but in the depletion region you have less number of a holes less than N A. The material is still p type, so you still have p greater than n but the value of the p less than N A, and this is because your bias the semiconductor negative so that you pulling the holes away from the semiconductor or you pushing electrons. Now, if we keep increasing the bias we are going to get more negative charge in the semiconductor and you are going to find that at one particular point, the number of electrons will be more than the number of holes so that you create a region where you have n type conductivity is oppose to p type. This thing is called inversion.

So, let me the draw the again. So, once again I have a metal, I am going to draw my semiconductor slightly bigger so I can show the different regions that is my p type. So, i have the bulk of the semiconductor the bulk. I have the depletion region where semiconductor is still p type, but the concentration of holes less than N A.

So, I have a depletion region and then finally, I have region so closer to the surface where I have more electrons than holes so that I have inversion. So, in the bulk I have p equal to N A that is in the bulk, in the depletion region I have p greeter than n, so that it is still a p types, but it is less than N A. And finally, I have inversion region where n is greater than p. So, in the case of p type semiconductor I have formed a channel by applying a negative bias to the semiconductor.

So, this is the principle of your metal oxide semiconductor which will use in the transistor. The difference between this and JFET is that in the case of a JFET you already had and n channel that was present and by applying the voltage we shrank or decrease the width of the channel and control the current. In the case of a MOSFET, the channel is formed by applying an external potential so that the channel is not immediately there and by increasing the potential you can increase the width of the channel and control the current.

So, in next class we are going to the look at the working of a MOSFET, so once again we can draw this current which was voltage characteristic. We will also look into some more detail on the formation of the depletion and the inversion region and also calculates there widths. So, next class we will look at MOSFET s in detail.