Processing of Semiconducting Materials
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Lecture - 38
Low-k and High-k Materials

Today's lecture will be on the high-k and low-k dielectrics as discussed earlier during our discussion on the dielectric film deposition. That in semiconductor processing, we will have two types of materials; one is the low-k - k means the dielectric constant, another is the high-k or the high dielectric constant. Both type of materials, we have to make, we have to process for finishing a IC chip or a discrete device.

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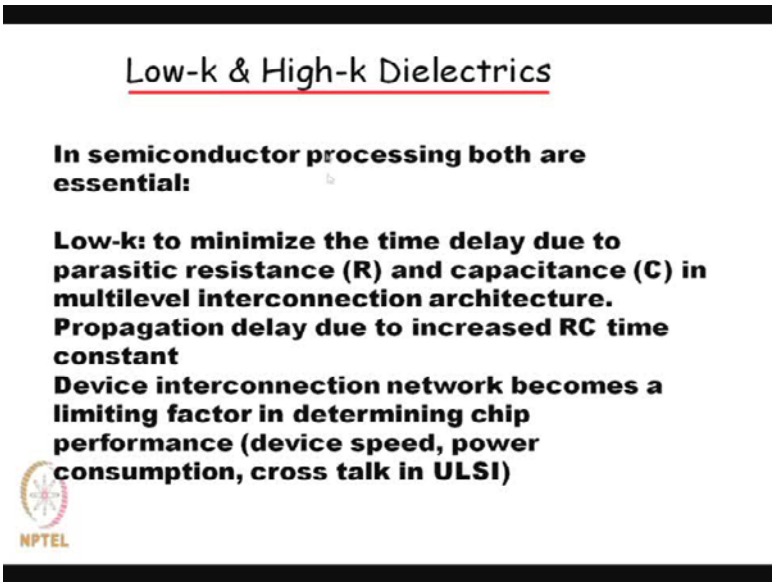

Now, if we see at the view graphs why this low k is required. As discussed earlier, this low k is required to minimize the time delay in an interconnection architecture.

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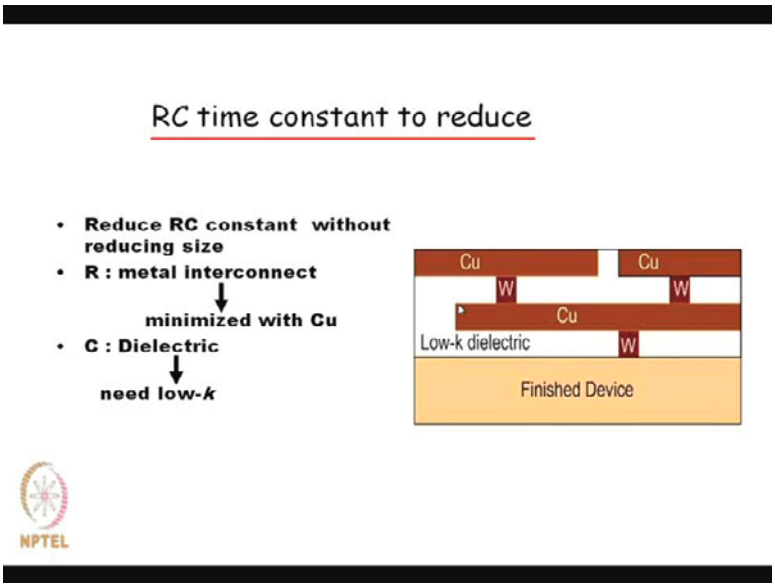

Now, if you consider this interconnection architecture, you can find that a large number of metal lines are there which were connected, say in this case the copper connected with the tungsten to another copper. So, there will be an interconnection of the metals, and that is required for the finishing of the device. That means, for the connections of the one device to the other one function with the other, and this is for the interconnection in the device itself. Now to minimize the time delay, now,what is the time delay? Time delay is basically, the product of R and C, where R is the resistance and C is the capacitance.

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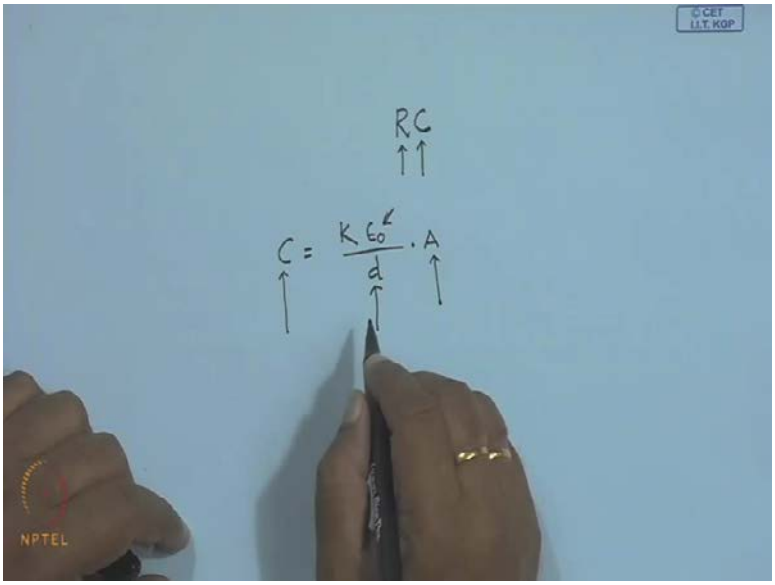

So, you can see that this time delay, which is a product of R and C that must be minimized. Now, how to minimize R and how to minimize C? Now, if you see that this R. R can be minimized by using say in case of copper if you compare with the aluminum R for copper is less. So, the metal interconnect which we shall use that will minimize the R. And the C the value of C will be minimized by the low dielectric constant, why because if you see that C the capacitance is given by the dielectric constant of the material multiplied by the free space permittivity divided by the thickness, and multiplied by the area. So, now if you want to minimize C you have to minimize A, but minimize A is a very difficult because in that case.

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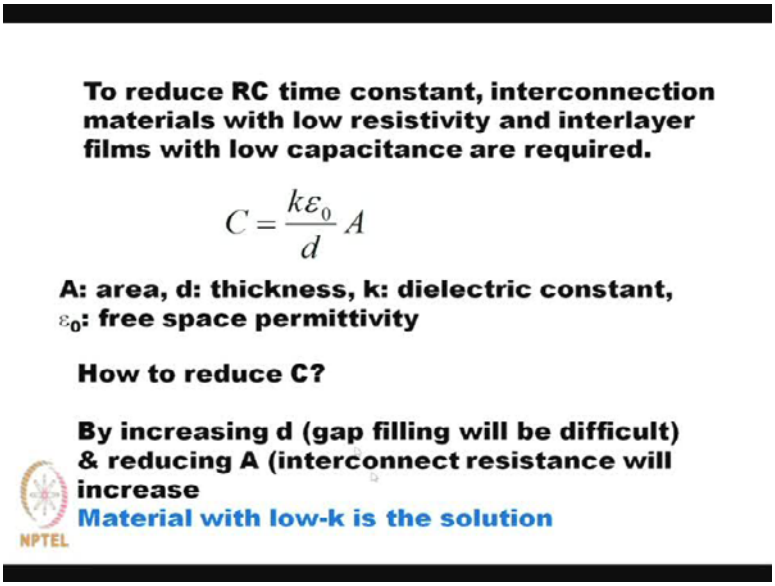

You see that if you reduce A, the interconnect resistance will increase. So, we do not want because the interconnect resistance in this case will be increased epsilon 0. That means, the free space permittivity it has a constant value 8.85 into 10 to the power minus 12 farad per meter. And d is the thickness one approach can be that you can minimize the, you can maximize d, you can increase d, but if you increase d then there will be a problem with the gap filling, the gap filling will be difficult. Because if you increase the thickness, then those gaps you have to fill with some materials and which will be very, very difficult.

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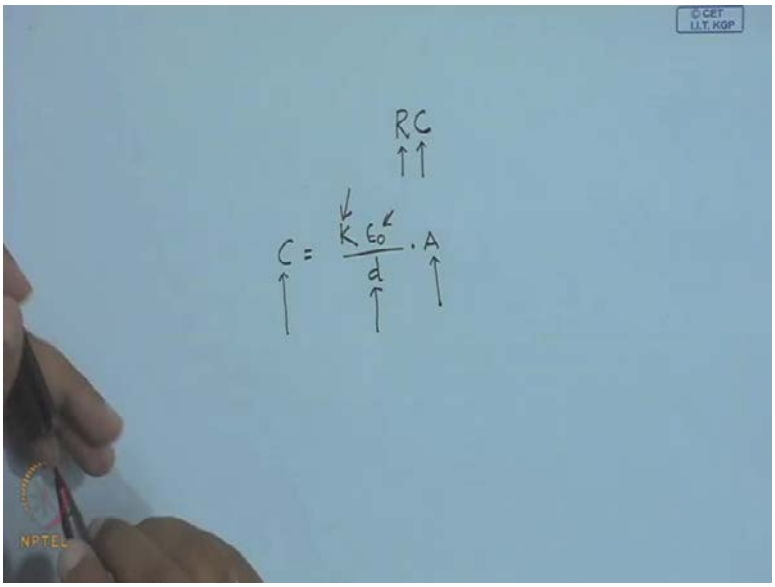

So, we have no other option, but to reduce the value k. So, that is the logic that for an interconnection architecture. If you want to make time delay as minimum as possible you have no other option, but to decrease both R and C, but so far as the R is constant, you can use any low resistive material say copper is widely used aluminum can be used, but copper is better than aluminum or even you can use silver and gold for discrete device in some cases.

So, that the resistance will be further minimum and the capacitance can be the can be minimized by the minimum value of k, which is the low dielectric constant material. Now, in that case if you minimize it is otherwise, what will happen the interconnection network becomes a limiter, limiting factor in determining chip performance. What are the chip performance such as, the power consumption will be high device speed will be low, there will be cross talk in ultra large skill integration. So, it is it justifies the use of low-k material in interconnection network, which is a basic processing in the U L S I or the ultra large scale integration chips.

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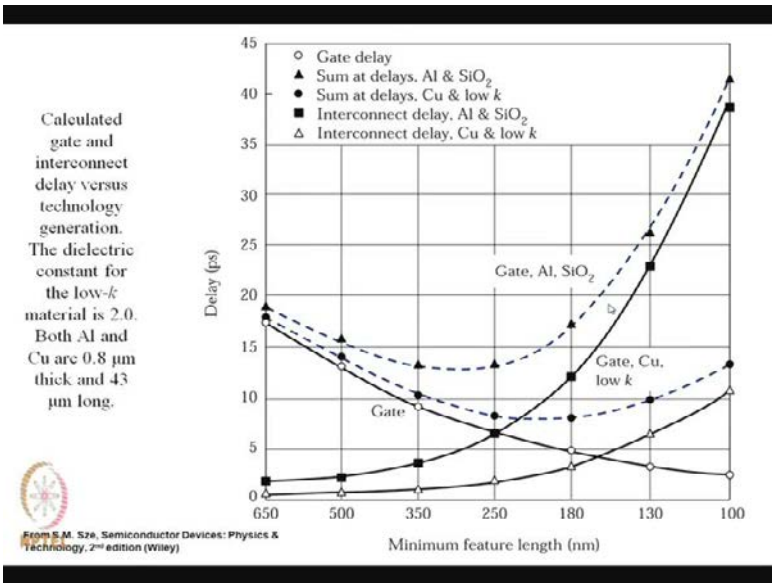

This figure, which we have shown earlier also in case of our discussion on the dielectric film deposition that if you reduce the feature length. That means, if you go on decreasing the length of the feature size that means, for nano devices say or scaling down. Then what happens the gate delay will be reduced, but at the same time the interconnection delay will be increased because you see that the interconnection delay is in a delay increases with the minimum feature, length here in the x scale you see that we have started from 650 to 100. So, that means it is decreasing. So, as the minimum feature length decreasing the gate delay increases, and it increases by such a factor that even if you take the some of the delays. So, it will be dominated by the gate delay.

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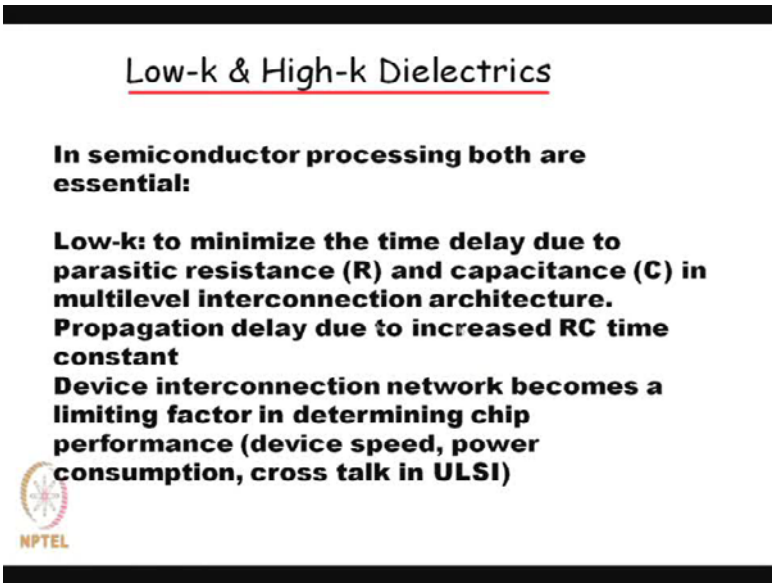

So, that is why here we have written that limiting factor will be the device interconnection network. So, device interconnection must have the minimum value of the time delay or R, C. Now, what should be the criteria?

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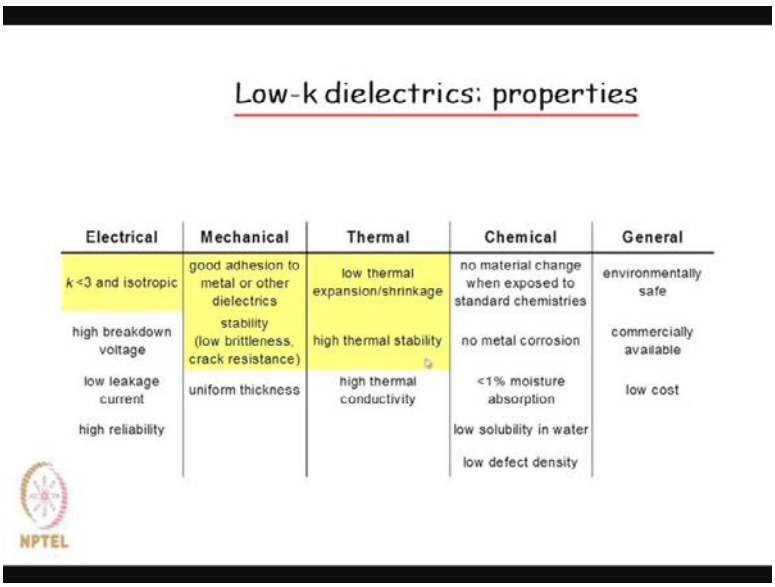

This is the criteria that low-k dielectric must have these properties and you see that when we talk about low-k dielectric it means, the value of the dielectric constant will be less than 3, it must be isotropic. So, far as the isotropic is concerned it must be the value will not have any direction dependence, in all the directions you will find that the value will

be same whether, you take in the x direction or the y direction. So, in all the directions the value of the dielectric constant will be same also, the dielectric must be able to have high breakdown voltage because otherwise, there will be breakdown there will be large tunneling. So, the leakage current will increase.

So, the property must be the value you have to choose or the material we have to choose in such a manner that the material must be very must support very low leakage current, or it will have very high breakdown voltage and the high reliability. Another properties are the mechanical good adhesion to metal or other dielectrics should must have, it must be low brittleness, crack resistance, uniform thickness processing is possible then it must have low thermal expansion on shrinkage, high thermal stability, high thermal conductivity then chemical properties that there will not be any metal corrosion, and it will have low solubility in water, low defect density and environment friendly.

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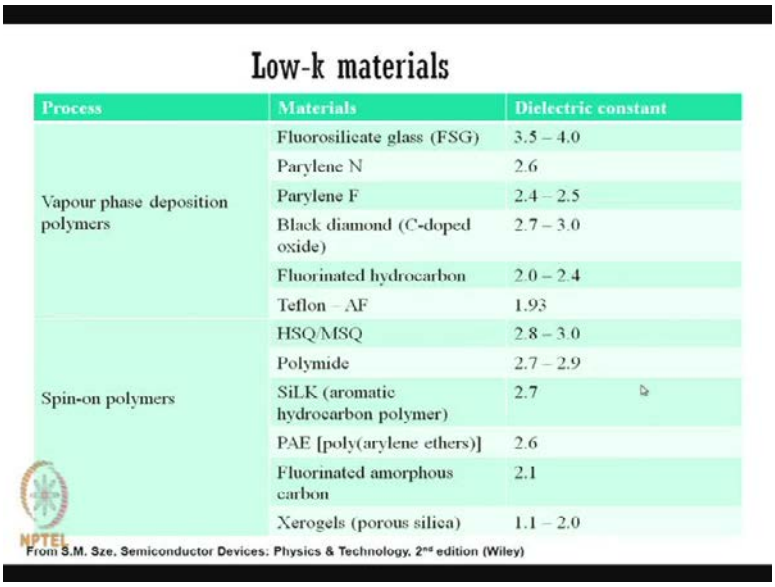

Now, a lot of materials these materials we have shown earlier also that a lot of materials are there, which we can make by either the vapor phase deposition or that means, the C V D or spin-on deposition, S O D these are almost all of them are polymers except a few and here you see that the dielectric constants are almost 3 or less.

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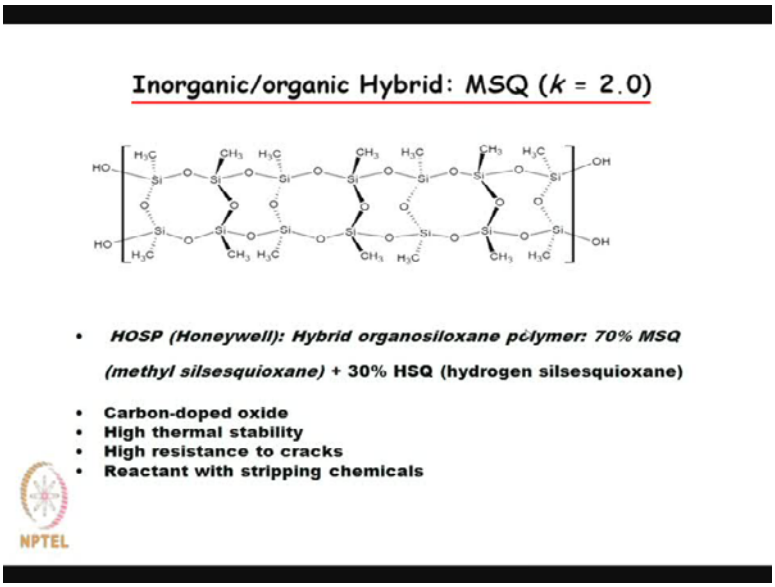

Now, one material can be say M S Q and this is inorganic organic hybrid material, the chemical structure is shown and the brand name of this material, which is available in the market is H O S P hosp, it is from the honey well and it has the dielectric constant low to this is an hybrid organosiloxane polymer and hybrid organosiloxane polymer, it has 70 percent M S Q. That means, methyl silsesquioxane and 30 percent H S Q. That means, hydrogen silsesquioxane and this material is basically, a carbon doped oxide it has very high thermal stability it has very high resistance to cracks, and reactant with stripping chemicals. So, these are the main feature of this material, which is available in industry.

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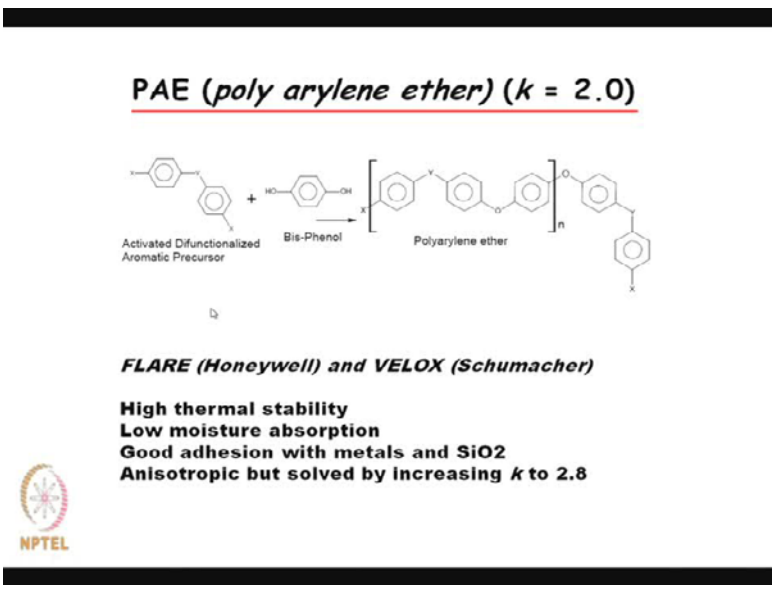

Then another material can be P A E poly arylene ether.

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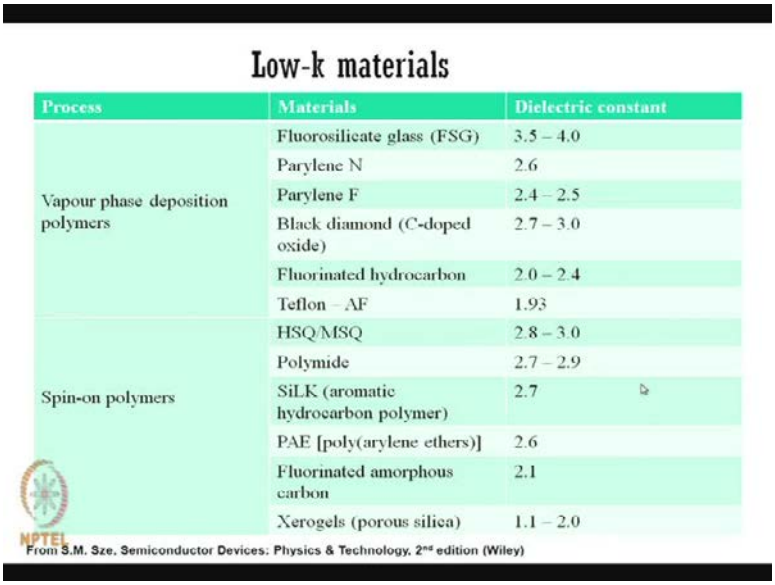

You can see that here we have P A E or poly arylene ethers. So, depending on its chemical structure it can have value 2.6 or even less in this particular case, which is known as the flare available from the honeywell or Schumacher, the velox these two material brand name those are the proprietary item of honeywell schumachar and it has the dielectric constant to the chemical diagram is shown.

And it has very high thermal stability, low moisture absorption good adhesion with metals and S I O 2 and anisotropic that we have discussed earlier, that this anisotropic is basically, the value is not a fixed one it can have different values at different directions. So, this is one of the problem, but it can be solved if we can go on increasing the k by say 2.6 or 2.8 then it will be isotropic and not anisotropic.

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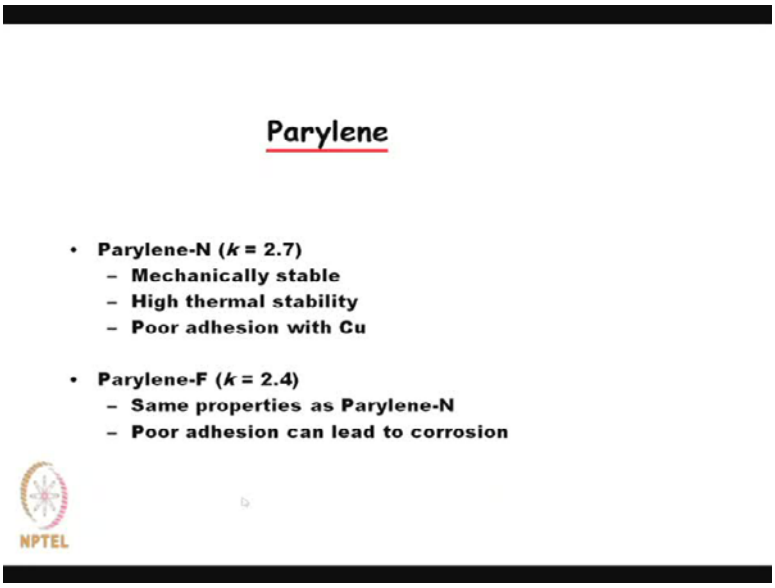

The next material can be parylene, parylene-n with k equals to 2.7 or parylene k, f k equals to 2.4 and parylene-n has mechanical stability, mechanically it is very stablehigh thermal stability poor adhesion with copper, and parylene-f has the same properties as parylene-n and poor adhesion can lead to corrosion. So, that is one of the disadvantage of parylene.

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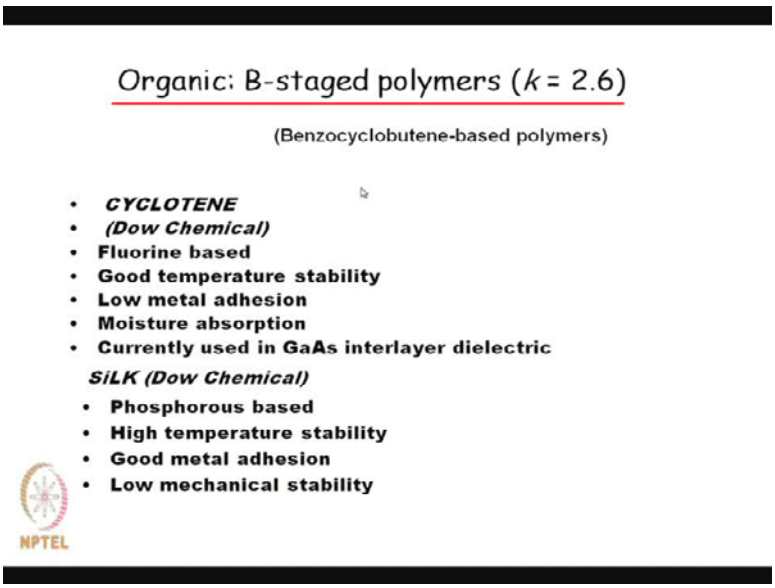

Then it can be another material can be organic material, which is known as b-staged polymer having value k equal to 2.6 b-stage means, benzocyclobutene based polymers

and there are two materials available from in the market, and both are from the dow chemical they are the proprietary items one is cyclotene another is silk S I L K. Cyclotene is a fluorine based material it has good temperature stability, low metal adhesion moisture absorption and currently used in gallium arsenide interlayer dielectric.

So, that is very important thing we shall discuss about this gallium arsenide because as discussed several times during our last 38, 39 lectures that gallium arsenide or (()) semiconductor has certain advantages over silicon, silicon dioxide system. So, far as the mos mos devices are concerned. And today we shall discuss some of the features of gallium arsenide based mos, where we shall use the high-k dielectrics. So, and in this case you see that the interlayer dielectric currently used with gallium arsenide is basically, the cyclotene available from the dow chemical, or the other material say silk S I L K it is a phosphorus based material, it has also high temperature stability, good metal adhesion and low mechanical stability.

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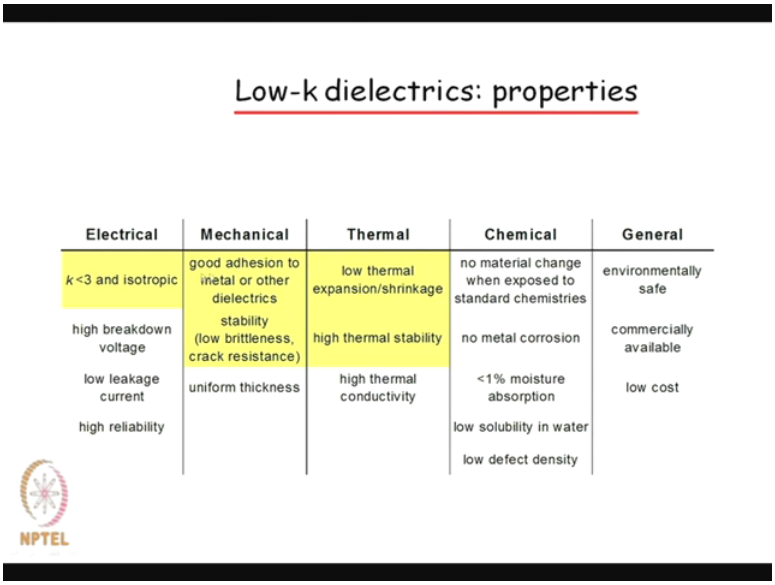

So, if we go back to these properties we have that the mechanical property will have to be good, good adhesion to metal that is very important and it will have high thermal stability also. So, in this case we see that it has low mechanical stability and cyclotene has low metal adhesion, some limitations are also there so far as those materials are concerned.

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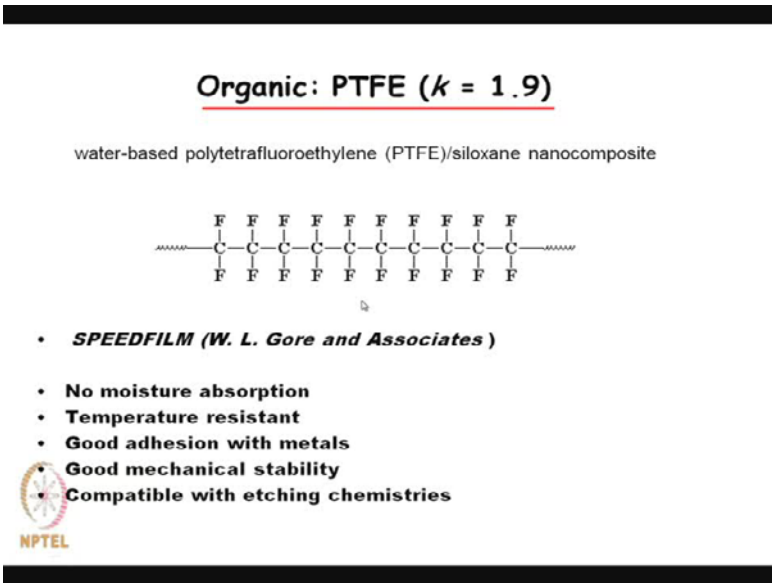

Another material is P T F E it is water based polytetrafluoroethylene P T F E. That means, teflon etcetera that is a siloxane nano composite, the chemical structure is shown and from W. L. Gore and associates one metal, one material is available having the polytetrafluoroethylene that is derivative of this thing is the speed film. It has no moisture absorption, it has it is it has the property of temperature resistance, it has good adhesion with metals, it has good mechanical stability and compatible with etching chemistries that is also important because in some of the cases, we will find that etching must be done.

So, this teflon or the P T F E is one such materials having k is very low 1.9 having these properties and it is also industrially available in the name of speed film from W. L. Gore and associates. So, now with this discussion we can, we can conclude so far as the low-k materials are concerned it is very, very important that this material is used in the interconnection, in the interconnection and these interconnection must have these interconnection network must have the low R C value and with this low R C value, we do not have to we do not change R.

Generally, the copper is used having very, very low r, but C we can have different types of materials as discussed earlier, then with that material it around two value of the dielectric constant is the best one and different materials, we have considered having some limitations as well also and industrially available. Some of the material are used in

the present day semiconductor process lines and now, we shall take one example numerical example using, which we can and substantiate our view that the value of C must be less in case of the low dielectric materials, which is the requirement one such example is that.

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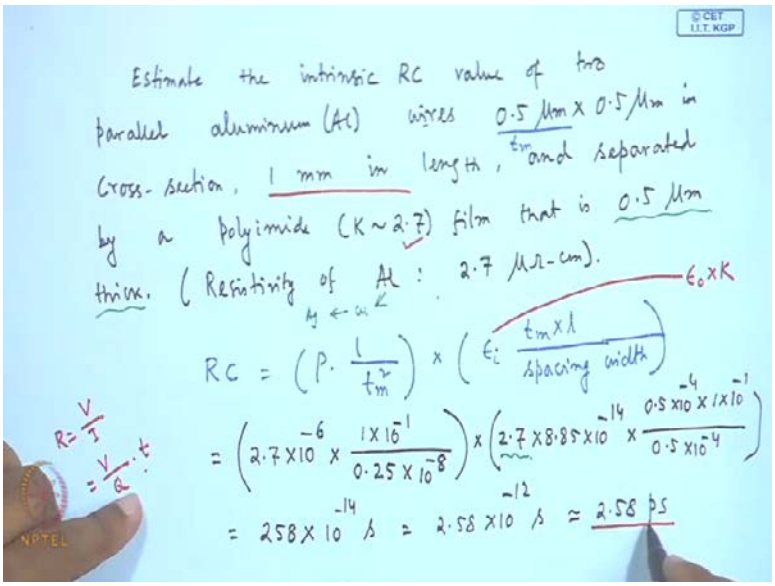

Estimate, the intrinsic R C value of two parallel aluminum wires 0.5 micrometer by 0.5 micrometer in cross section. So, this is basically a square cross section and one millimeter in length, and separated by a polyimide value k. That means, dielectric constant as 2.7 film that is 0.5 micron thick given resistivity of aluminum is 2.5 micro ohm centimeter. So, let me repeat estimate the intrinsic R C value of 2 parallel aluminum wires 0.5 micron by 0.5 micron in cross section, 1 millimeter in length and separated by a polyimide film that is 0.5 micron thick, and the dielectric constant 2.7 given resistivity of aluminum 2.7 micro ohm centimeter.

Now, if we want to solve this problem R C, R into C, R is equal to rho into we know l by a area and area is equals to here the cross section 0.5 by 0.5 micron. So, let us say that this is t m the dimension, and c is given by epsilon r multiplied by t m into l because area by the spacing S P A C I N G width d. That means, it is epsilon i, epsilon i is nothing but the epsilon 0 epsilon i in this case it is epsilon 0 multiplied by the k k is given.

So, now with this relation let us solve this problem and what is the value of rho, rho is given by 2.7 micro ohm centimeter. So, it is 2.7 into 10 to the power minus 6 then it

becomes ohm centimeter multiplied by l, l is 1 millimeter l is 1 millimeter you can find. So, it will be 1 into 10 to the power minus 1 centimeter by t m square is 0.5 micron by 0.5 micron. That means, 0.25 micron and square and it will be multiplied by 10 to the power minus 8 we arrive at the centimeter.

So, that is the value of rand in C G S unit and then epsilon r i is k into epsilon 0. What is k? K is 2.7 it is given k is 2.7 then multiplied by 8.85 into 10 to the power minus 14 in C G S unit farad per centimeter. Then t m is 0.5 micron into 10 to the power minus 4 in centimeter into l ones millimeter 1 into 10 to the power minus 1 centimeter and spacing d is again 0.5 micron 0.5 micron 3.

So, d is 0.5 micron and it is 0.5 into 10 to the power minus 4 centimeter. So, with this we find that the value of R C. That means, that delay is 258 if you multiply and work out with some manipulation 258 into 10 to the power minus 14 second. That means, 2.58 into 10 to the power minus 12 second and which is equals to 2.58 pico second. So, we find that this is very, very small 2.58 eight pico second and here we must say that the value of R C is basically the in the time is the dimension because R is equals to you can consider V by I and this I is Q by t.

So, V into by Q into t and then this is farad and that is also farad C is in farad, it is one by farad so that will be the second or the time. Now, if you go towards the lower resistive material, say from aluminum to copper or from copper to silver or silver to gold etcetera you can find that this is a 2.7, we will further go down and this is in the numerator. So, as this value will decrease, R C time constraint will further decrease so that is an and estimation of the time delay in a R C network, where aluminum and polyimide is used or if you can use that instead of polyimide some other film. So, this will go down and the resistivity will also go down at the same time, if you use the copper or silver. So, further reduction of the time delay is possible.

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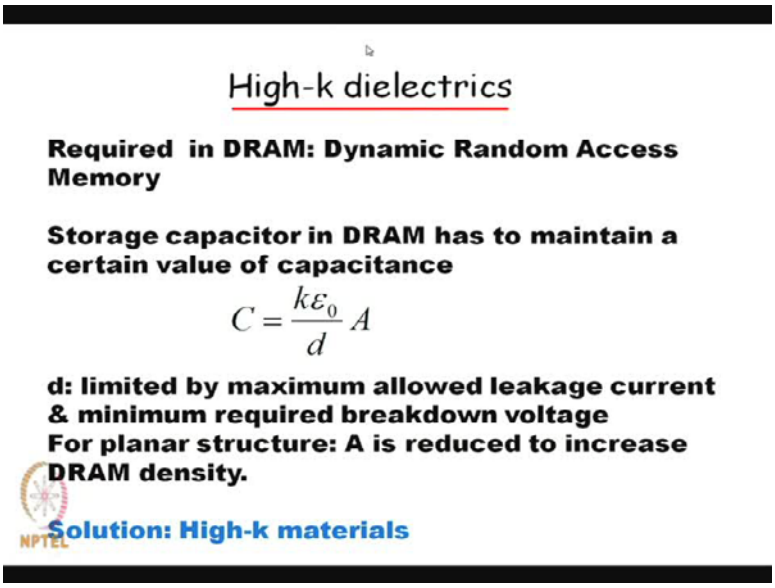

Now, we talk about the high-k dielectric this high-k dielectric is very, very important material for dynamic random access memory. This dynamic random access memory is useful in case of the memory devices and the storage capacitance, you can see that in d ram the storage capacitor has to maintain a minimum value, has to maintain a certain value of the capacitance certain value if the capacitance here, again we make use of this relation.

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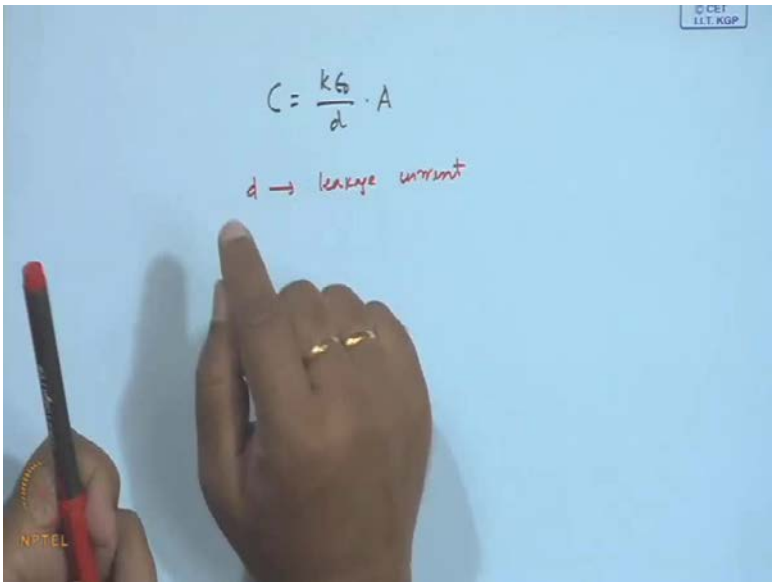

That means, the capacitance C is equals to k epsilon 0 by d into A, where k is the dielectric constant epsilon is 0 is the free space permittivity, d is the thickness and A is the area. Now, you can now, you if you want to increase C suppose we want to increase C because the storage capacitor must have some maintain, some certain value. Now, what is the requirement, requirement is that d can be less to increase C, d can be less, but if you can make d very, very small then there will be leakage current problem. So, d is limited by the leakage current. The thickness is limited by the leakage current, you cannot take any value of d if you want to take d very, very small value then there will be leakage current, there can be breakdown problem. So, it is limited by the maximum allowed leakage current.

So, it is limited by the maximum allowed leakage current and minimum required breakdown voltage. Now, for planar structure A is reduced to increase dram density by making stacks stack and string etcetera. So, that is possible. Otherwise, if you can make a very, very large then there will be the problem of the scaling down. You cannot go to very, very small structure. So, we have no other option, but to increase the value of k. So, that is why the high-k dielectric is the solution.

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Material	Dielectric constant	Band gap (eV)	CB offset (eV)	Breakdown (MV/cm)
SiO_2	3.9	9	3.1	14
Si_3N_4	6.3	5.3	2.1	6.3
Al_2O_3	8.5	8.8	2.8	6.2
HfO_2	21	6	4	4
Ta_2O_5	19	4.4	1.3	3.5
ZrO_2	25	5.8	2.7	3.8
TiO_2	30	3.9	1.7	3.4
$SrTiO_3$	183	3.3	1.75	1.1
PZT	300	3.2	1.34	0.87

Now, a large number of materials we find that are available in the market or one can synthesis these are the S I O 2 having dielectric constant 3.9 then S I 3 N 4, we have discussed the S I O 2 and S I 3 N 4 earlier. The dielectric constant is 6.3 then a large

number of materials like A L 2 O 3 hafnium oxide, tantalum oxide, zirconium oxide, titanium oxide, strontium titanate, P Z T.

That means, lead, zirconium, titanate, a large number of material having dielectric constant you see 3.9 is the lowest for S I O 2, which we regularly use for S I S I O 2 device to 300 very, very large value and band gap also you can see, the tabulation has been done then conduction band offset also been shown with minimum with the breakdown voltage in mega volt per centimeter for S I O 2 it is the highest, and for P Z T is the lowest. So, almost an inverse relation is obtained so far as the dielectric constant and breakdown is concerned.

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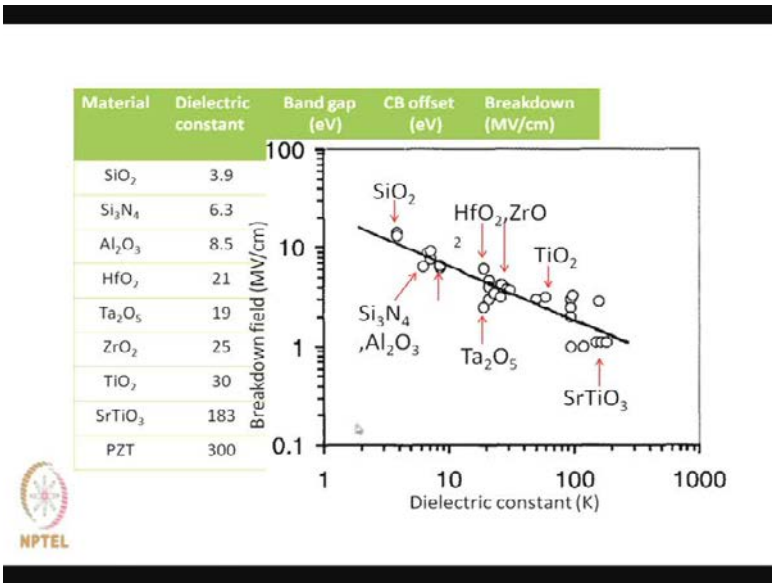

So, we see that if we plot this value the breakdown field it is in millivolt, megavolt per centimeter in the y axis and dielectric constant in the x axis, we can see that as the dielectric constant increases, the breakdown field decreases. So, we cannot take any value of the dielectric constant because in that case, we shall have the breakdown field we have to face or we have to encounter, the low breakdown field and so there will be breakdown and the device cannot have any stability or reliability. That is one of the major things that even that the S I O 2 has the lowest dielectric constant of 3.9 it is widely used till now.

However, if you find some of the metal material some of the dielectric metal oxides like say T I O 2, Z R O 2 hafnium oxide, tantalum oxide those are used because the dielectric

field, which have with they have for a particular dielectric constant is allowed in some of the cases. So, people can use T I O 2, Z R O 2 hafnium oxide, tantalum oxide etcetera because the dielectric constant is very high if you consider H F 2, H F O 2 it is 21 zirconium 25, titanium 30.

So, very high value almost eight times, seven times higher than S I O 2 and the breakdown field you see that the breakdown field of is say around eight point ten point something, whereas for zirconium or hafnium for zirconium etcetera it is say 1, 2, 3, 4 almost 4, 5, 2 etcetera. So, those are basically the values which one can make use of and so there is no harm if we can replace S I O 2 in some of the systems with the newer metal oxides.

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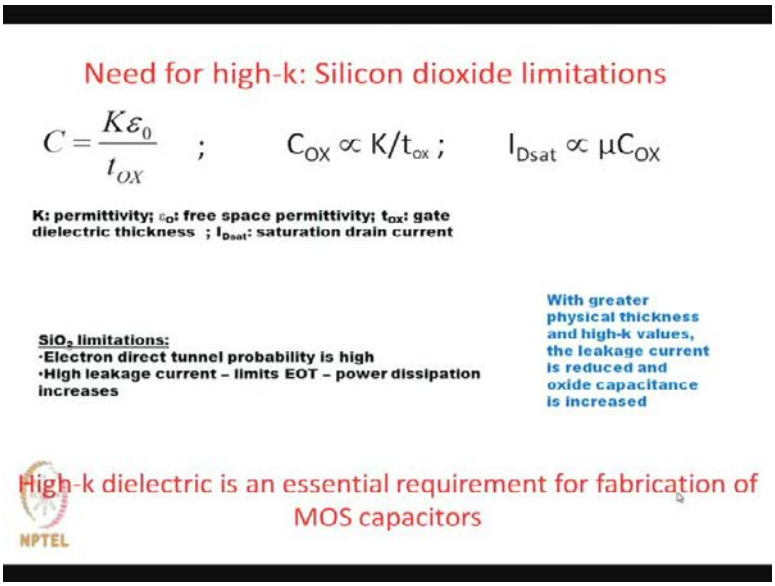

Now, problem with the silicon dioxide is that, it has some limitations like electron direct tunnel probability is high. As you go on reducing the physical thickness of the S I O 2 layer then there will be some electron tunneling probability, as you scale down the silicon device. So, the thickness of the silicon dioxide will have to be reduced, but in that case you see that this capacitance per unit area, it is given by this relation and the equivalent oxide thickness or the oxide it is basically K by t ox.

So, now the thickness if you can make very, very small C ox will be high, but with the T o x will if T o x is small then there will be direct tunnel probability, high leakage current will be there. The power dissipation will also increase and so equivalent oxide thickness

will be the limiting factor. And also we can see that the saturation drain current is basically the function of the mu the mobility multiplied by the oxide capacitance C o x.

So, if we want I D sat to be increase then C o x must be increased for a particular value because mu is fixed in that case. So, with greater physical thickness and high-k values the leakage current is reduced and oxide capacitance is increased. So, that is very important thing and for scaling down you cannot go with greater physical thickness. So, that these are the limitations of S I O 2. Now, if we consider that the replacement then there will be some high-k dielectric and that is an essential requirement for fabrication of MOS capacitor.

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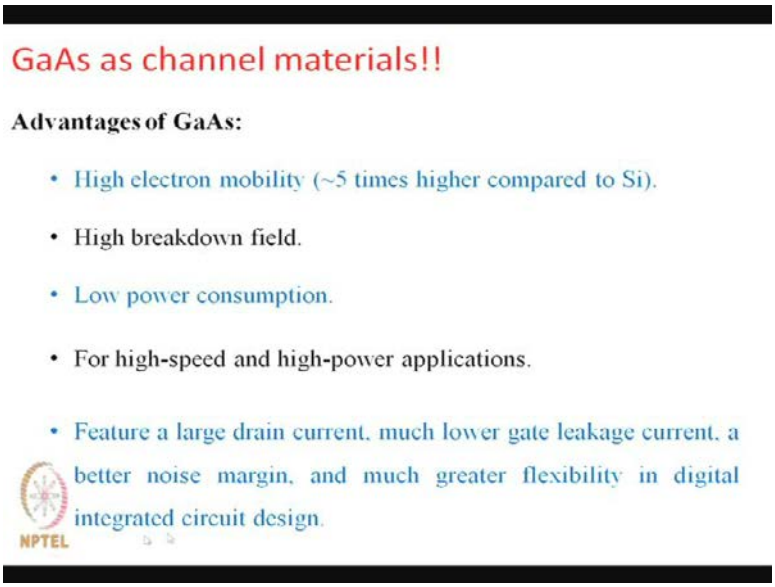

Now, this gallium arsenide what are the benefits of gallium arsenide channel materials, it has high electron mobility, the electron mobility of silicon is 1900, 1800 centimeter squared per volt second, but in case of gallium arsenide it is almost 9000 or above 9000. So, five times higher compared to silicon then it has high breakdown field, low power consumption for high speed and high power application it is used, and it feature say large drain current much lower gate leakage current a better noise margin, and much greater flexibility in digital integrated circuit design. So, these are the advantages of gallium arsenide over silicon. So, gallium arsenide can be a good choice for future generation MOS devices or say for memory devices.

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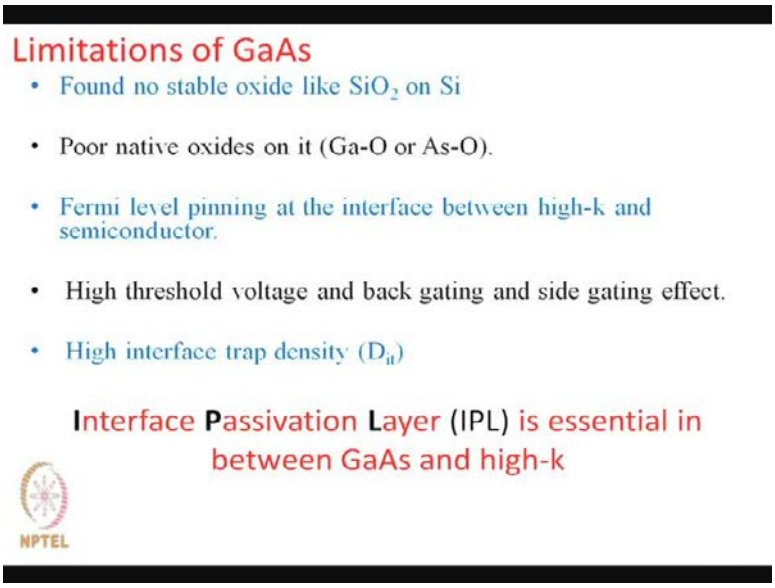

But it has some limitations also found no stable oxide like S i O 2 on silicon because you see that S I O 2 is the oxide it is basically, the oxide of silicon, but it is the native oxide. However, in case of gallium arsenide the native oxides are gallium oxide or arsenic oxide because that is the binary compound gallium will have its own oxides, arsenic will have its own oxides. And these are poor native oxides very poor properties electrical properties are very, very poor and fermi level pinning at the interface between high-k and semiconductor is also there fermi level pining and high threshold voltage back gating, and side gating effect and high interface trap density.

So, these are the limitations of gallium arsenide base, MOS devices if you want to mix some MOS devices to replace silicon with gallium oxide or arsenic oxide, then these are the problems. And so what one can do that you can make some interface passivation layer between gallium arsenide and high-k. Suppose, this is your gallium arsenide and with this is your gallium arsenide, and with this gallium arsenide before making a layer of say high-k dielectrics you passivate the gallium arsenide surface itself.

So, you can make use of the interface specification layer and different chemical treatments you can use, like people have been have made some sulphur treatment ammonium sulphite they have used chemically treated, the surface to reduce the native oxide etcetera. That means, to clean the surface to dip in the fermi level because from the gallium oxide or arsenic oxide bonds, there will be pinning of the fermi level and also

because of those oxides, poor native oxides, the interface trap density is also very, very high in case of gallium arsenide based device.

So, one can make use of the interface passivation layer and different types of interface passivation layer people have used S I O 2 have been used A L 2 O 3 has been used zinc oxide is used, indium phosphide as pseudomorphic layer is used. So, that is the solution that interface passivation layer is made and it is essential between gallium arsenide and high k.

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IPL	Thickness (nm)	Capacitance	Hysteresis (V)	D_{it} ($cm^{-2}eV^{-1}$)	Leakage current @-1V (A/cm^2)
Sulfur	10.5 (Al_2O_3)	0.6 μF/cm^2	0.43	5×10^{11}	3×10^{-8}
Ge	6.5 (HfO_2) + 1.5 Ge	2.6 μF/cm^2	0.27	5×10^{11}	3×10^{-4}
Si	7 HfO_2 + 1.5 Si	1.2 μF/cm^2	0.8	–	10^{-6}
AlON	10.8 (TiO_2) + 3.3 (AlON)	1 μF/cm^2	–	6.9×10^{12}	2.8×10^{-5}
TN	3 (TN)	4 fF/ cm^2	–	–	10^{-6}
Si/SiO_2	3-5 nm	5×10^{-11} F	–	10^{10}	10^{-5}

Now, if we consider different interface passivation layer say sulphur layer, germanium layer, silicon layer, aluminum oxynitride layer, titanium nitride layer S I S I O 2, we have shown as a benchmark because we shall compare the values of the different interface passivation layer are with the S I S I O 2 MOS. Now, if we use a sulphur interface passivation layer that means, sulphur passivation on gallium arsenide before the deposition of high-k then we can see that the some of the properties, these are the properties that we can compare what is the D i t value, D i t is the interface trap density the value has been shown in centimeter square inverse electron volt inverse.

So, with sulphur specification the gallium arsenide based MOS capacitor we will have D i t value 5 into 10 to the power 11, with a germanium treatment germanium layer 5 into 10 to the power 11 with silicon no such values is available, aluminum oxynitride 6.9 into

10 to the power 12 and for titanium nitride no such values available. Now, what we find that these treatment is made on the gallium arsenide surface.

However, the dielectrics or the oxides which are used over that gallium arsenide surface is different, in this sulphur treatment we have used aluminum oxide A L 2 O 3 the thickness of A L 2 O 3 is 10.5 and with this value of an dielectric layer over gallium arsenide with sulphur treatment, the leakage current is found to be very, very small 3 into 10 to the power minus 8 ampere per centimeter square at minus 1 volt. Then D i t is also reasonable and hysteresis is 0.43 volt then germanium with hafnium oxide as dielectric and germanium 1.5 nanometre thickness, the value of the leakage current is not very good 3 into 10 to the power minus 4.

So, it has basically so far as the leakage current is concerned, there is a increase in the leakage current at the same voltage of minus 1 volt. However, the D i t is same 5 into 10 to the power 11 and hysteresis has improved 0.27 from 0.43 then if we use a silicon layer this silicon passivation means, a take a gallium arsenide wafer on which you deposit 1.5 nanometer silicon and then 7 nanometer hafnium oxide with that structure, the leakage current is 10 to the power minus 6 ampere per centimeter square and hysteresis is 0.8. So, this is not a solution because we see that both the hysteresis and the leakage current has increased so far as the sulphur treatment is concerned.

Then with aluminum oxynitride it is 2.8 into 10 to the power minus 5 not bad, but even with sulphur it is very, very less compared to aluminum oxynitride and D i t value, the interface trap density is 6.9 into 10 to the power 12, which is very high and with titanium nitride with the value is 10 to the power minus 6, leakage current and if we compare with S I S I O 2 system.

That means, S I S I O 2 as a benchmark. So, D i t we have to go to 10 to the power 10 and till now, such kind such small value or such lower value of D i t is not possible. A leakage current we have found that lowest is in case of the sulphur treatment, which is 3 into 10 to the power minus 8 even S I S I O 2 has the large leakage 10 to the power minus 5, which is comparable, which is which is even worse compared to other sulphur surface treatment or sulfur surface passivated gallium arsenide MOS devices.

Now, the technology which one can use at this movement for the gallium arsenide surface passivation or treatment is the sulphur because the leakage current is very, very

less compared to S I S I O 2 as benchmark and D i t value is obviously greater than S I S I O 2, but it is 5 into 10 to the power 11 reasonable value.

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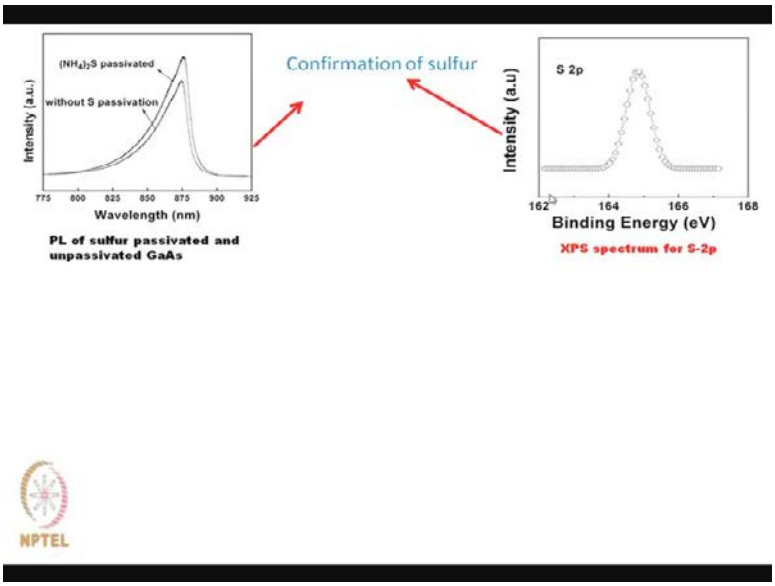

Now, with this thing, if you if you sulfur treat the surface.

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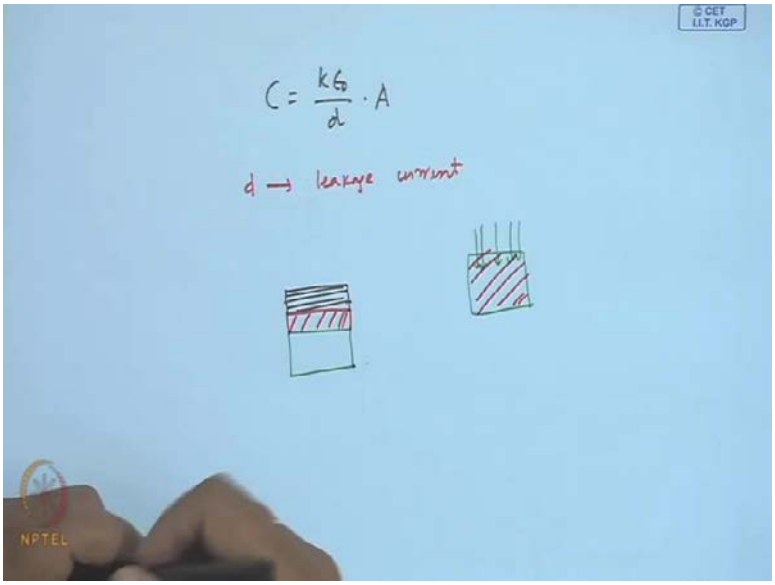

Suppose, if you take a gallium arsenide wafer on which you make some sulphur treatment, then you deposit the oxides then you deposit the oxides after treatment you deposit the oxides. So, that means effectively the cross sectional view will be this is the gallium arsenide on which there will be a sulphur treatment, the red region is the sulphur

treatment and on which you have can you can make use of different type of oxides. So, this is the black one is the oxides see with this treatment, what we find that.

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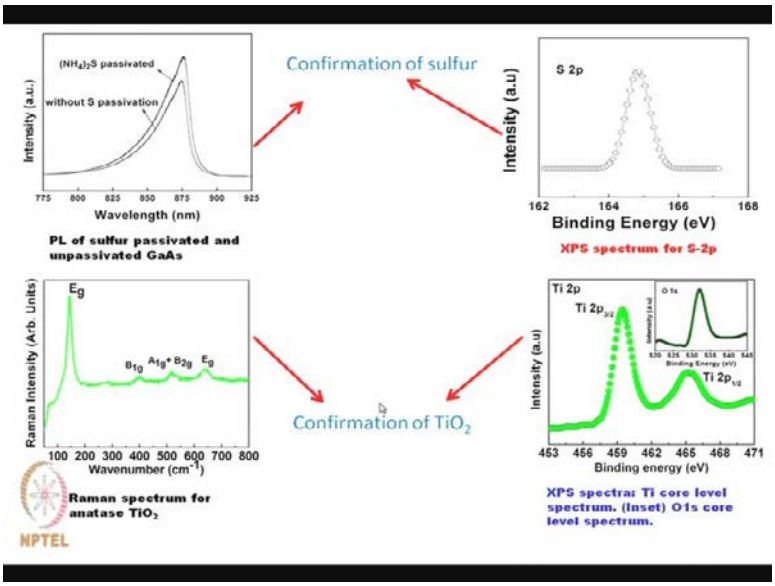

This is the photo luminations of sulphur passivated and unpassivated gallium arsenide with sulphur passivation, we see that the intensity increased and without sulphur passivation, if we compared these two the intensity increased with sulphur passivation and the treatment was done with the ammonium sulfite chemical solution. Why this is not this is not a perfectly Gaussian curve, we because this is at taken at room temperature.

So, there will be different kinds of broadening etcetera and another conformation that one can make with the X P S x-ray photoelectron spectroscopy, this is the x-ray spectrum for S 2 P in the x axis, binding energy has been shown and this is the characteristics binding energy for S 2 P, this is the conformation of sulphur. And with their thing on sulphur, we have used the titanium oxide as the dielectric layer.

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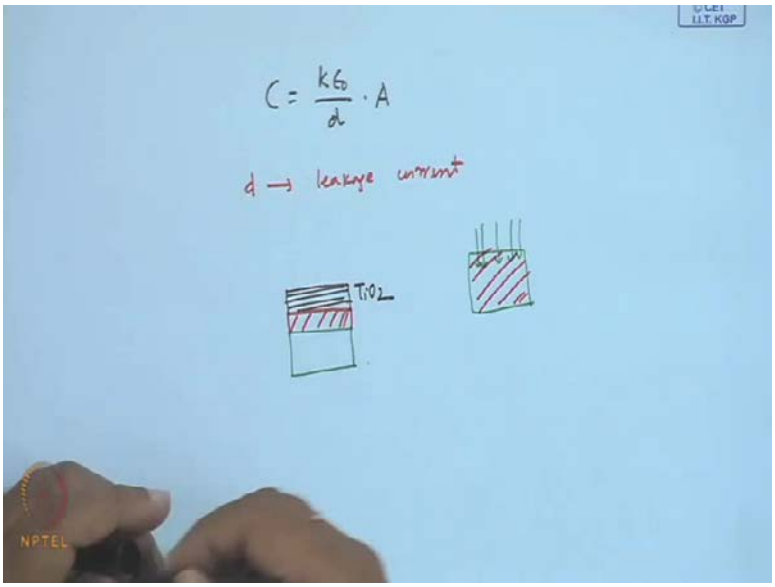

That means, this back layer which we have shown is T I O 2 titanium dioxide.

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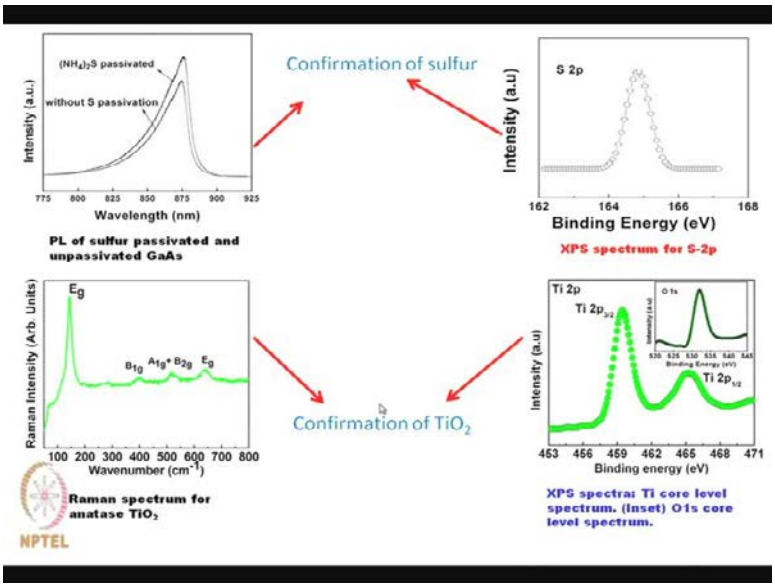

Then with titanium dioxide, we have used the Raman spectroscope, as well as the X P S to conform the formation of T I O 2 on the gallium arsenide substrate.

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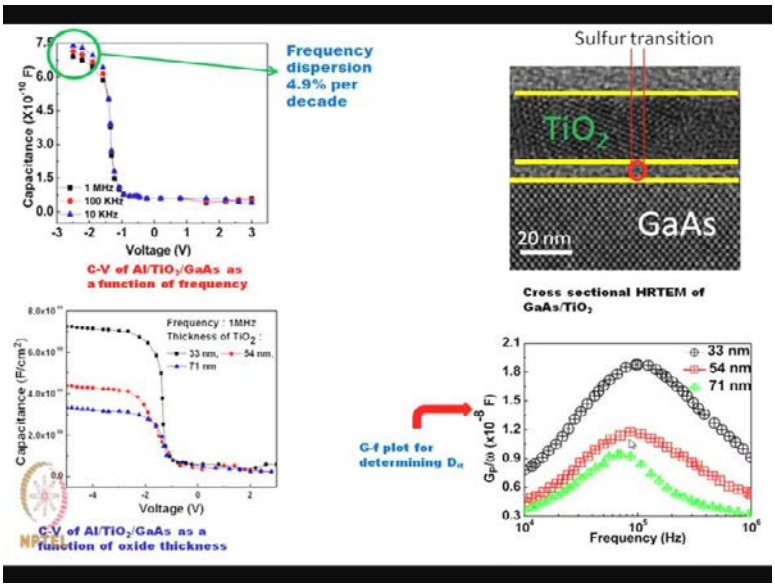

This is the frequency dispersion this is the C V characteristics of the sulphur treated devices, where we can see that we are we have used titanium oxide and aluminum as the gate electrode, the frequency dispersion is very, very small almost 4.9 percent per decade because here we have used 3 frequencies, the blue one is 10 kilohertz, the red one is 100 kilohertz and the black one is 1 megahertz.

So, at lower voltages you can see that point minus 2 minus 3 voltage that is obviously a dispersion, but the dispersion is very, very low 4.9 percent per decade this is the cross sectional high resolution T M of gallium arsenide T I O 2 structure, where between gallium arsenide T I O 2 we have made used of sulphur, this is the sulphur transition region gallium arsenide and T I O 2.

So, smooth interface is obtained and this is the C V characteristics that means, the earlier one that is a different frequencies, but here we have used different thickness of T I O 2. Three types of thickness, we have three thicknesses we have used one is 33 nanometer the black one, and red one is 54 nanometer and the blue one is 71 nanometer. The measurements we have taken at a frequency of 1 megahertz and it is the conductance frequency plot for three different thickness of the T I O 2.

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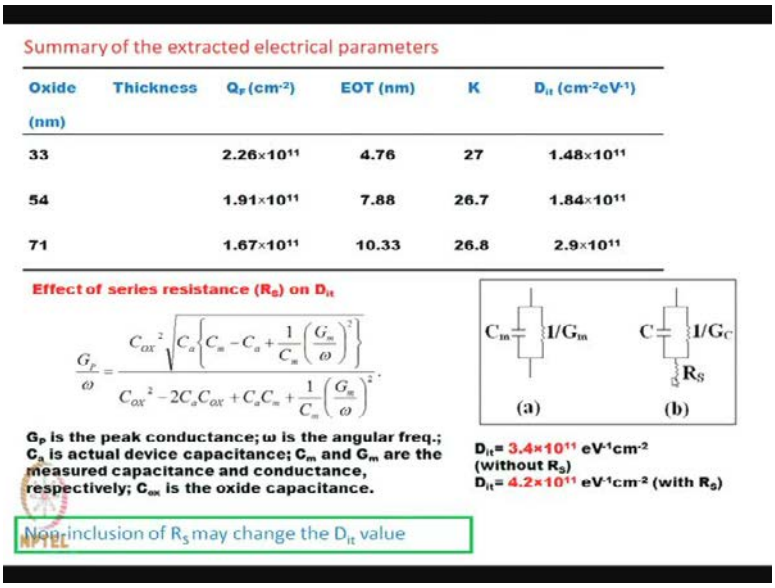

Now, from these measurements we have calculated the D i t value, D i t value we have calculated and we see that oxide thickness value if you increase 33 to 54 to 71 the equivalent oxide thickness also increases, the dielectric constant is almost same from 26.7 to 27. And D i t value we can find that it is increased 1.4 into 10 to the power 11 to 1.84 into 10 to the power 11 to 2.9 into 10 to the power 11.

Now, the values we have measured the D i t value we have measured from the conductance technique. That means, from this plot with this equation and we see that in one case if you use the series resistance R S is the series resistance, and this series resistance you can include or you cannot, if you include series resistance the value will be high 4.2 into 10 to the power 11, however without series resistance 3.4 into 10 to the power 11. So, non inclusion of series resistance may change the D i t value so that is very, very important thing that one must consider.

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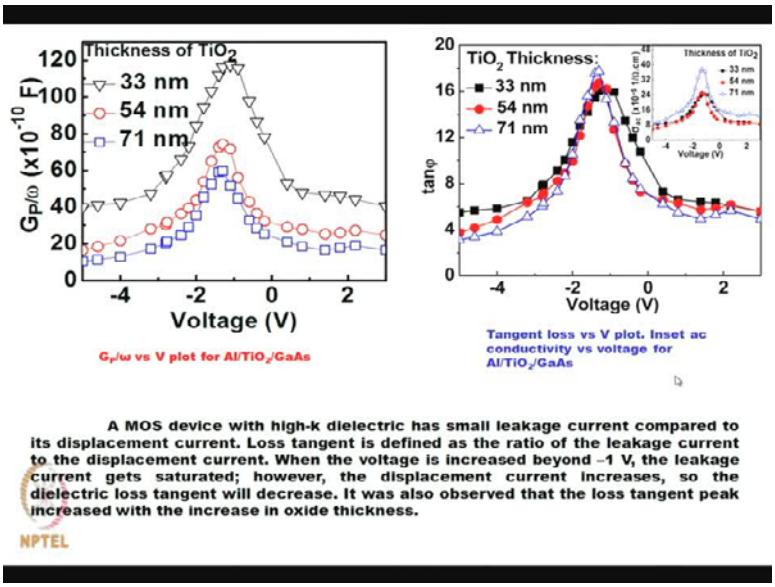

And this is the this plot we have shown earlier also, here the tangent loss versus voltage plot and in the inside it is the conductivity versus voltage plot for different types of thickness, we have measured the conductance versus voltage. If MOS device with high-k dielectric has small leakage current compared to its displacement current. Loss tangent is defined this is a loss tangent, it is defined as the ratio of the leakage current.

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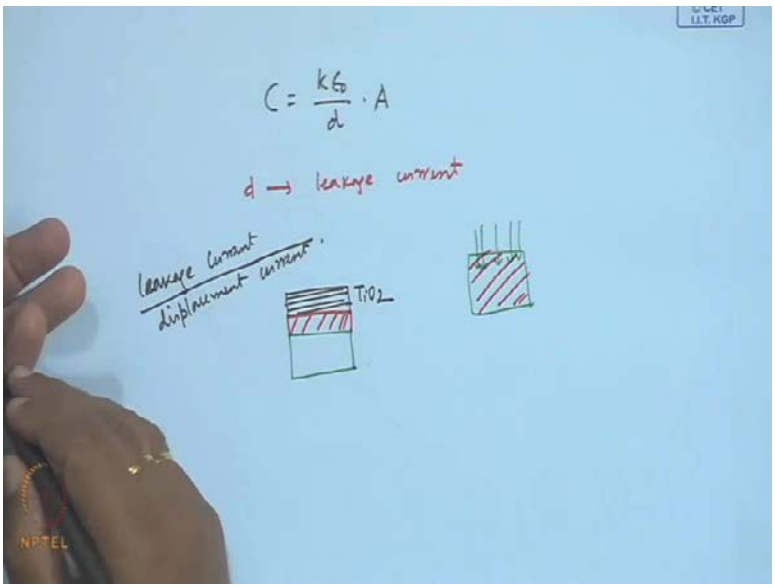

As the ratio of the leakage current to the displacement current, and when the voltage is increased beyond minus 1 volt in case beyond minus 1 volt, the leakage current get saturated.

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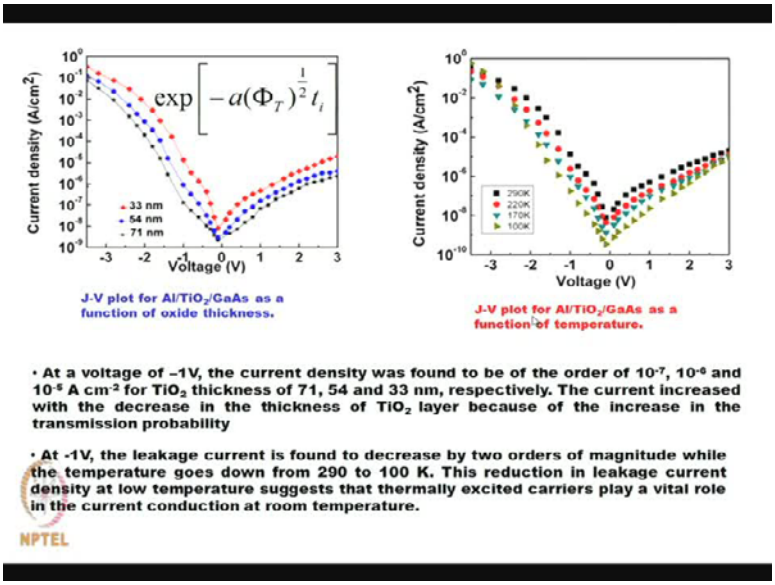

However, the displacement current increases. So, the dielectric loss tangent will decrease so displacement current increases that is why the dielectric loss tangent decreases, it was also absorbed that the loss tangent peak increase to increase in oxide thickness, and at a voltage of minus 1 volt the current density was found to be the order of 10 to the power minus 7, 10 to the power minus 6 and 10 to the power minus 5 ampere per centimeter square for T I O 2 thickness of 71, 54 and 33 the red one is 33 and the blue one is 54 black one is 71.

So, this is the I V characteristics, that means current density versus voltage. At a particular voltage say minus 1 volt, we have compared and with a TIO 2 thickness of 71 it is very, very high 10 to the power minus 7 ampere per centimeter square is very, very good value because with sulphur treatment and with say and here with sulphur treatment and A L 2 O 3, we have seen that it is 3 into 10 to the power 8 and here we have not use the A L 2 O 3 rather we have used the T I O 2 and it is 10 to the power minus 7. The current increased with the decrease in the thickness of T I O 2 layer because of the increase in the transmission probability.

Now, here the a current density is plotted as a function of voltage at different temperatures from 100 k, to 290 k in the 4 values at minus 1 V the leakage current is found to decrease by 2 orders of magnitude, while the temperature goes down for 290 k to 100 k, two orders of magnitude, this reduction in leakage current density at low temperature suggest that thermally, excited carriers play a vital role in the current conduction at room temperature.

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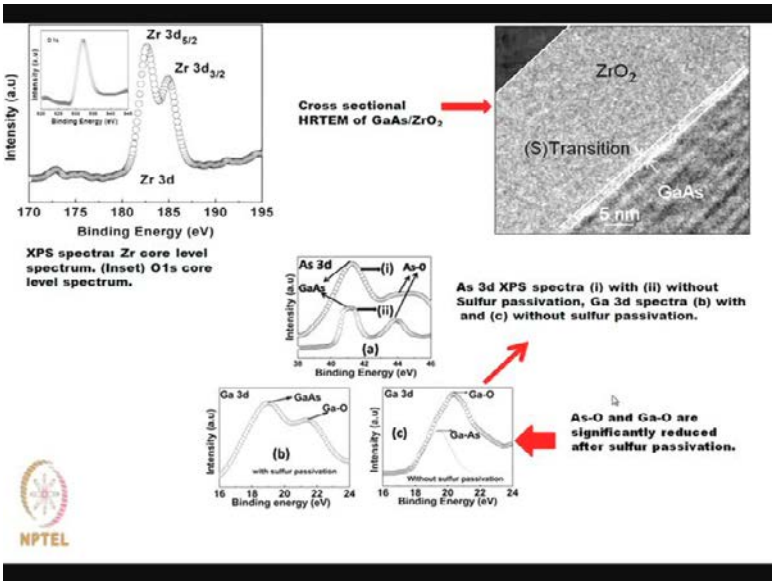

And here with zirconium then the sulphur passivation has been done earlier works were related to T I O 2 and this is related to a zirconium we can find that the X P S spectra has been shown to prove the formation of Z R O 2, Z R 3 D 5 by 2, Z R 3, 3 D, 3 by 2, 2 pic's are obtained and in the inset oxygen one a core level spectrum has been shown. In this case it is the H R T M image that between gallium arsenide and zirconium, a sulphur passivation layer is obtained and then S P X spectra has been taken with and without sulfur passivation in one it is with sulfur passivation, in two without sulfur passivation. So, what we find that this is the arsenic 3 D spectrum and this is the arsenic oxide, this arsenic oxide has been decreased this is very sharp pic here it is mere doubt.

So, with sulfur passivation we find that there is a considerable decrease in arsenic oxygen bond, here also the gallium oxide is very high here the gallium oxide you see that this is without sulfur passivation, and compare to this it is very high. So, the sulfur passivation has reduced both gallium oxygen and arsenic oxygen bonds on the gallium

arsenide sulphate. So, the poor electrical performance due to this native oxides of gallium arsenide could be eliminated, which can be enhanced the characteristics can be enhanced and at the same time, we find that this is the origin of the fermi level pinning. So, there is a possibility that deepening has been obtained.

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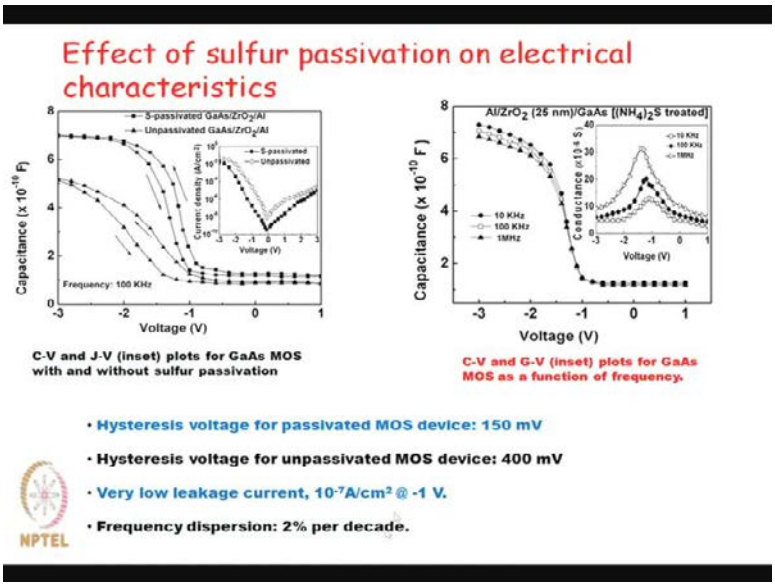

Now, what are the effect of sulfur passivation on electrical characteristics, the effect of sulfur passivation on electrical characteristics is that, here the upper curve is the sulfur passivated structure, and the lower the bottom one is the structure without any sulphur passivation. And in the inset, we have shown the current density versus voltage here also we can find that the very low leakage current with sulfur 10 to the power minus 7 ampere per centimeter square at minus 1 volt, and hysteresis voltage is 150 millivolt for passivated, and without passivated it is 400 millivolt. So we see that the very low leakage current is obtained with sulfur passivation, and the hysteresis also has gone down from 400 millivolt to 150 millivolt the frequency dispersion is we have seen that it is two person per decade.

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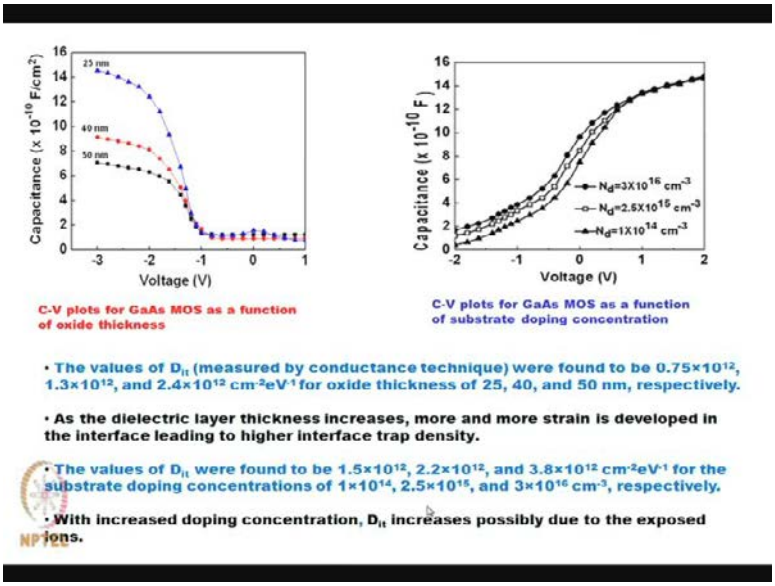

Then the values of D i t, which is measured by the conductance techniques, it is obtained as 0.75 into 10 to the power 12 to 2.4 into 10 to the power 12 not very encouraging. And as the dielectric layer thickness increases more and more strain is developed, in the interface leading to higher interface trap density, and this value of D i t were found to be 1.5 into 10 to the power 12, 2.2 into 10 to the power 12 and 3.8 into 10 to the power 12, for the substrate doping concentration of 1 into 10 to the power 14, 2.5 into 10 to the power 15 and 3 into 10 to the power 16. So, basically this is the capacitance voltage characteristics with different thickness of Z R O 2 this is the C-V characteristics with surface substrate concentration different 10 to the power 14, 10 to the power 16 it is found that with increase doping concentration D i t increases possibly due to the exposed ions.

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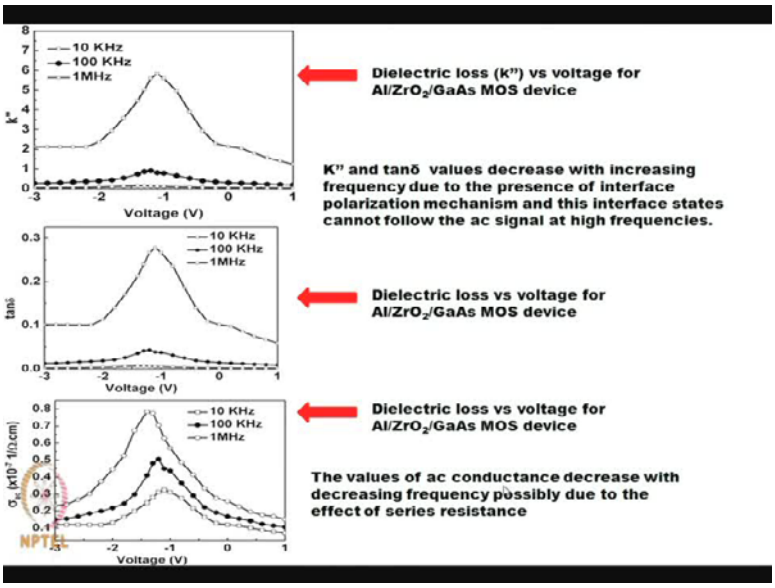

Now, dielectric loss k double prime versus voltage for aluminum, zirconium, gallium arsenide and MOS devices and this is the dielectric loss tan delta and this is the A C conductivity. So, both all the properties that means, the dielectric loss that loss tangent and A C conductivity, we can find that these values decrease with increasing frequency due to the presence of interface polarization mechanism, and these interface states cannot fallow the A C signal at high frequencies. And the value of A C conductance decreases with decreasing frequency possibly due to the effect of series resistance.

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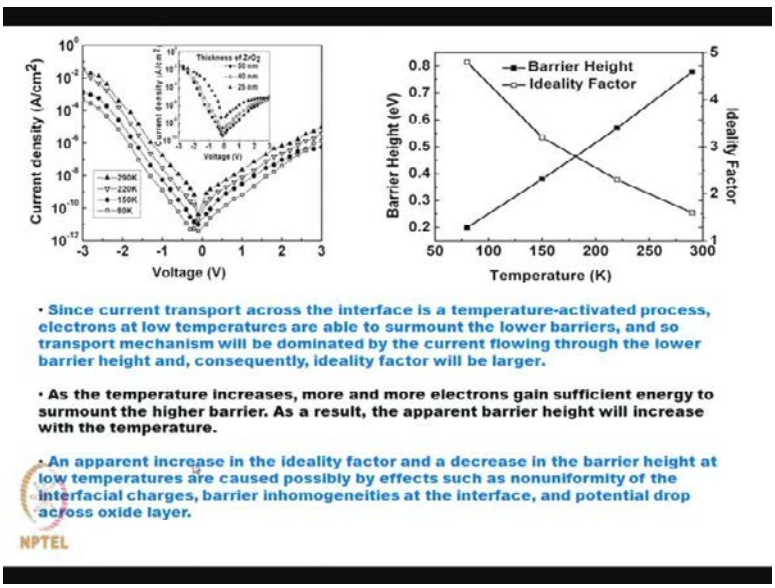

So, we find that this is very important technology that if you use the gallium arsenide based MOS devices, then better you make a sulfur treatment and if you do not have some facilities like the atomic layer deposition or M O C V D deposition of very thin pseudomorphic layers of 3, 5, or 2, 6 semiconductors over gallium arsenide, which also have been found to specify the passivate, the surfaces to reduce the interface trap density and to depinning the fermi level.

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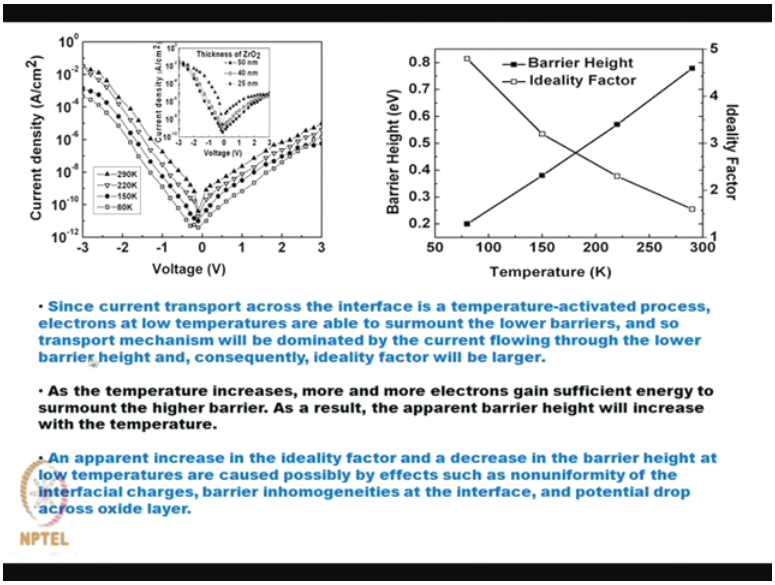

Now, here you see that a different temperatures the current density is plotted as a function of voltage and since, the current transport across the interface is a temperature activated process, electrons at low temperatures are able to surmount the lower barriers. And so transport mechanism will be dominated by the current flowing through the lower barrier height and consequently, ideality factor will be larger as the temperature increases more and more electrons gains sufficient energy to surmount the higher barrier, and as a result the apparent barrier height will increase with the temperature.

So, the we see that the barrier height increases with temperature at the same time the ideality factor decreases. And increases an apparent increase in ideality factor and decrease in the barrier height at low temperatures, are caused possibly by effects such as non uniformity of the interfacial charges, barrier in homogeneities at the interface and potential drop across oxide layers.

So, these are the things that one can evaluate. So, what are the parameters that one can evaluate from the MOS devices, one is the leakage current which must be very, very small. Second one will be the hysteresis will also will be very, very small because in that case we can conclude that if the hysteresis is very low then the trapping charges are low. So, D i t value will be obviously low and the value of the hysteresis will be low at the same time the interface trap density.

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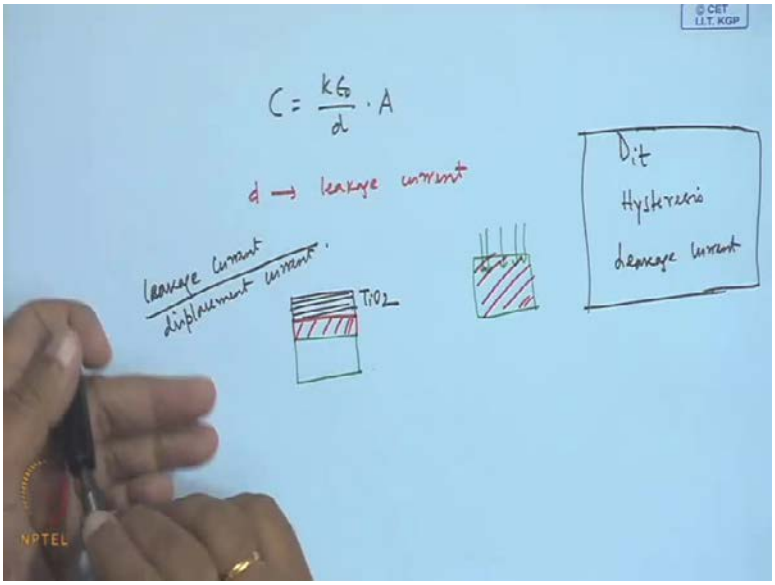

So, that means one factor is the interface trap density, number 2 is the hysteresis and number 3 is the leakage current. These are the three important parameters that one can evaluate for a particular MOS devices and in this view graph as discussed earlier that we have the benchmark as S I S I O 2.

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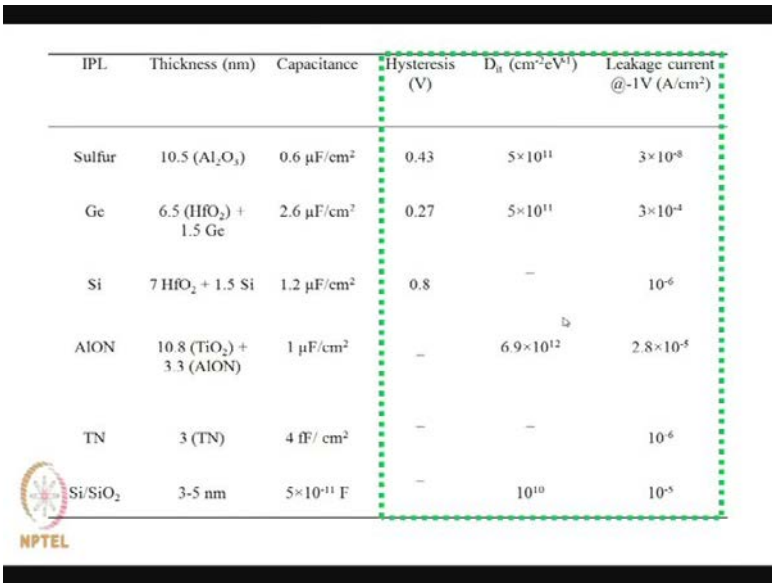

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Sulfur	10.5 (Al_2O_3)	0.6 μF/cm²	0.43	5×10^{11}	3×10^{-8}
Ge	6.5 (HfO_2) + 1.5 Ge	2.6 μF/cm²	0.27	5×10^{11}	3×10^{-4}
Si	7 HfO_2 + 1.5 Si	1.2 μF/cm²	0.8	–	10^{-6}
AlON	10.8 (TiO_2) + 3.3 (AlON)	1 μF/cm²	–	6.9×10^{12}	2.8×10^{-5}
TN	3 (TN)	4 fF/ cm²	–	–	10^{-6}
Si/SiO_2	3-5 nm	5×10^{-11} F	–	10^{10}	10^{-5}

So, these three parameters that means the hysteresis D i t and leakage current, one must be comparable with the S I S I O 2 system to obtain the low values of these parameters for application in the gallium arsenide based MOS devices. So, if we conclude today's discussion, what we find that one thing is the application of the low-k dielectric material in the R C network interconnection network system, we must have R C value low as low as possible and these low value of the delay, which is the multiproduct of R C is coming from the value of the C.

So, the value of C must be very, very low and C is a function of both area an inversely proportional to the thickness of the material, but thickness we cannot make very, very small because of the breakdown as well as the leakage current, and also because of the scaling of the MOS devices one or the ultra large scale integration. You cannot go beyond a certain value of the of the area, and at the same time if the area is becoming large then obviously, there will be.

If the area is becoming small then there will be the increase in the resistance of the interconnection network, at the same time the for the high-k material we have seen that, that is very important in case of the MOS devices in case of the d ram devices and for scaling down, we cannot go we cannot make a very, very large or d very small because making d very small, we will have the possibility of breakdown at the same time of very high leakage current.

So, we have no other option, but to increase the value of c and both the high-k and low-k materials, we have seen that they have their own advantages in different systems. We have discussed many materials in this connection, and one important thing we have seen that for low-k, it must be less than 3 and it can be an organic material, it can be an organic, inorganic hybrid material. There are many materials available in the industry particularly which are being regularly used in the existing semiconductor process lines. And for high-k material one important aspect is that if we increase the dielectric constant of a particular material then the breakdown field will be decreased and so if the breakdown field decreases, your devices will be will have no stability, no reliability and there will be breakdown of the device.

So, one must play around that what should be the value of the breakdown voltage, and with that voltage, what are the possibilities that one can use of a material one can use what type of material with the value of the breakdown voltage. And there are many choices like we have seen apart from S I O 2 then hafnium oxide, titanium oxide, zirconium oxide, tantalum oxide, many oxide metal oxides are also available.

And those one can make use and so at the end of this lecture, we can say that for large ultra large scale integration apart from S I O 2 silicon nitride is important S I O 2 has been seen to use as afield oxide as a gate oxide, silicon nitride for passivation for anti-scratching for resistor barriers for moisture and different type of impurities. Then we have make use of poly silicon, and finally the high-k and low-k materials for different applications.

Thank you.