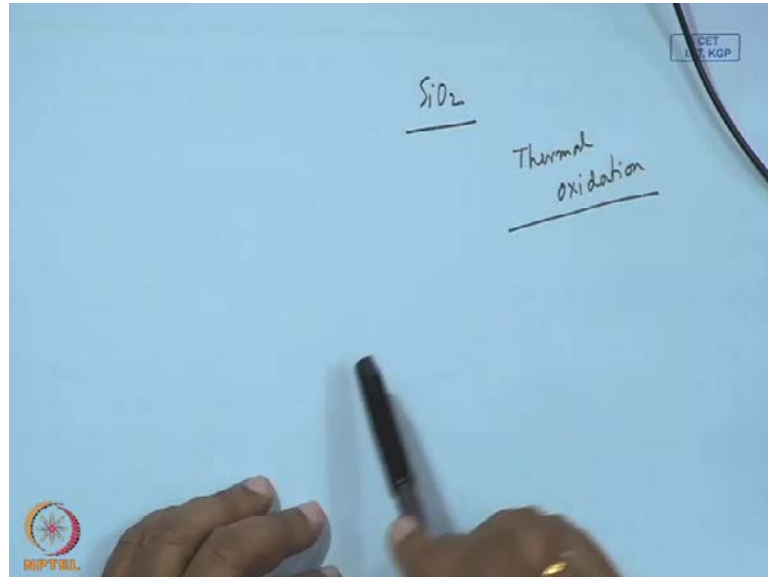


**Processing of Semiconducting Materials**  
**Prof. Pallab Banerjee**  
**Department of Material Science Center**  
**Indian Institute of Technology, Kharagpur**

**Lecture - 37**  
**Dielectric Films**

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In the previous class we have come across the silicon dioxide thin films  $\text{SiO}_2$ , which were mainly grown by thermal process, this is meant by thermal oxidation, and in details we have seen that during thermal oxidation very uniform thin films of  $\text{SiO}_2$  could be grown and those films are basically serves the purpose of the gate oxide in any MOS devices. Apart from gate oxide we also discussed that  $\text{SiO}_2$  are, films are also used for the field oxide.

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## CVD of Silicon Dioxide

**Not a replacement of thermally grown oxides  
rather to complement the thermal oxides**

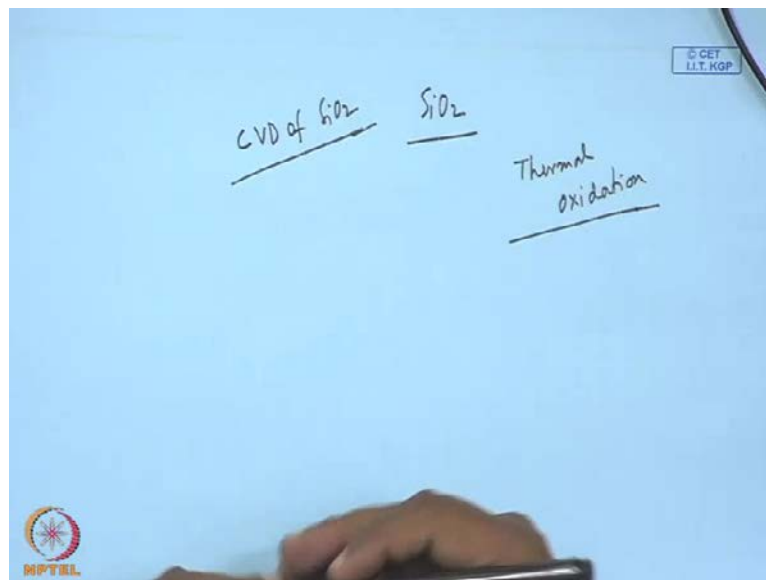
- to insulate multilevel metallization
- to mask ion implantation and diffusion
- to increase the thickness of thermally grown field oxides

**Phosphorus-doped silicon dioxide is used  
both as an insulator between metal layers  
and as a final passivation layer over device**



And in this case today we shall discuss the CVD of silicon dioxide. This CVD of silicon dioxide is basically is a replacement, is not a replacement of thermally grown oxides rather to complement the thermal oxides.

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So, that means if we proceed through CVD of silicon dioxide, that means it is not a comparative process of the thermal oxidation. It is basically the supplement or the replacement of the  $\text{SiO}_2$  grown by thermal oxidation. Remember, that thermal oxidation grown thin films of  $\text{SiO}_2$  are very excellent in electrical properties. They are

very thin, the growth rate is very small and in CVD basically you can grow thicker layer of  $\text{SiO}_2$  in fact and those are used basically to insulate multilevel metallization to mask ion implantation and diffusion to increase the thickness of thermally grown field oxides.

This is very important issue that in thermally grown field oxides you see that the thickness is very small. So, if you want to increase the thickness you have to go for the CVD process. CVD means the chemical vapour deposition. Now, this CVD of silicon dioxide is obviously is not as good as the thermally grown, but even then it will serve many various purposes of the semiconductor processing technology. Phosphorous doped silicon dioxide is used both as an insulator between metal layers and as a final passivation layer over device. So, it means that the silicon dioxide films can be doped even by phosphorous. However, it is not this; this doping is not like silicon for making n type of p type rather it is used as an insulator between metal layers and as final passivation layer over the devices.

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### Deposition methods of Silicon Dioxide

**Low temperature deposition (300 – 500 °C):  
silane**

**CVD or LPCVD: low temperature suitable for  
layer over aluminum**

**Intermediate temperature (500 – 800 °C):  
TEOS**

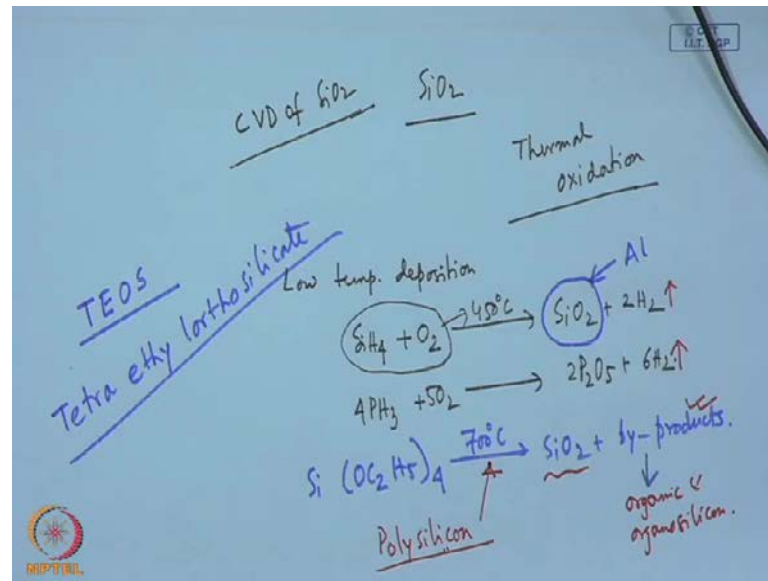
**LPCVD: suitable for polysilicon gates  
requiring a uniform insulating layer with good  
step coverage.**

**High temperature deposition (900 °C):  
dichlorosilane**



Now, how we can deposit the silicon dioxide films? There are three regimes of temperature which one can use. One is the low temperature regime where one can use 300 to 500 degree centigrade, another regime is the intermediate temperature range where one can use the 500 to 800 degree centigrade and around 900 degree centigrade there is high temperature process. So, obviously three different region of temperature one can use. So, let us start from the low temperature deposition.

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In the low temperature deposition we can use silane, the basic ingredients or the precursors which we use or the reactants is the silane  $\text{SiH}_4$ . So, that is basically the decomposition of silane, it is basically the decomposition of silane that takes place at this temperature. So, if we made to react silane with oxygen at say 450 degree centigrade what we shall get? We shall get  $\text{SiO}_2$  plus twice  $\text{H}_2$  that means hydrogen or you can dope it like say 4 phosphine  $\text{PH}_3$  reacts with oxygen, simultaneously it will give twice  $\text{P}_2\text{O}_5$  plus 6  $\text{H}_2$ .

So, we see that for the reaction of the silane and oxygen low temperature is used and since this temperature is quite low. So, this  $\text{SiO}_2$  which we can grow using this CVD process at low temperature can be made to grow on the aluminium layer. So, that means if you have some aluminium metal layer then over aluminium you can grow  $\text{SiO}_2$  and aluminium melting point is around six 600 degree centigrade. So, very high temperature you cannot use so far as the aluminium is concerned and for depositing  $\text{SiO}_2$  over aluminium.

However, this temperature is suitable for making a layer deposited over aluminium. So, that is very important concept or the applications of this low temperature deposition process. In the semiconductor process, we often see that different kinds of layers could be grown on different types of materials. In this particular example of  $\text{SiO}_2$  we can grow aluminium, it we can grow  $\text{SiO}_2$  over aluminium that means the metal, metal

layer and in this case the temperature is the driving force because of the melting point of aluminium which we just discussed.

Then in the intermediate temperature range we can use TEOS  $\text{TEOS}$ , this TEOS which is known as tetraethyl orthosilicate. So, it is a compound tetraethyl orthosilicate, it is a, an organometallic compound which is decomposed basically at this temperature of say 700 degree centigrade and to obtain  $\text{SiO}_2$ . So, this TEOS which chemically can be written as  $\text{C}_2\text{H}_5\text{SiO}_4$ , this is made to decompose at 700 degree centigrade to obtain  $\text{SiO}_2$  plus some by products. What are these by products? These by products are basically the, a mixture of organic and organosilicon, this is by product is a mixture organics and organosilicon compounds, mixture of organic and organosilicon compounds.

So, basically we find that here in the low temperature deposition process only the hydrogen gas is evolved and which can be vented very easily, but when we decompose TEOS at intermediate temperature range say 700 degree centigrade apart from  $\text{SiO}_2$  by products are also obtained. So, care must be taken and at this temperature of 700 degree centigrade obviously it is not used over aluminium. So, this  $\text{SiO}_2$  cannot be grown over aluminium rather it can be grown over polysilicon.

As we have discussed earlier also that polysilicon is the polycrystalline silicon which is widely used for or the preparation of the gallium, preparation of the MOS devices particularly the silicon MOS devices and we see that this polycrystalline silicon, which is in abbreviated form known as the poly silicon. This polysilicon is grown over the gate oxide. Sometimes, polysilicon is grown over say silicon to for making the Ohmic contact or making some shallow junction on silicon.

So, a large number of applications are there for polysilicon and this polysilicon and temperature is high so melting point, so one can use this tetraethyl orthosilicate that means TEOS compound for making  $\text{SiO}_2$  over polysilicon. So, the the difference between these two process that is the low temperature process and the intermediate temperature process is that in intermediate temperature process the, since the temperature is very high one cannot deposit  $\text{SiO}_2$  over aluminium rather it can be grown over polysilicon.

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## Deposition methods of Silicon Dioxide

**Low temperature deposition (300 – 500 °C):  
silane**

**CVD or LPCVD: low temperature suitable for  
layer over aluminum**

**Intermediate temperature (500 – 800 °C):  
TEOS**

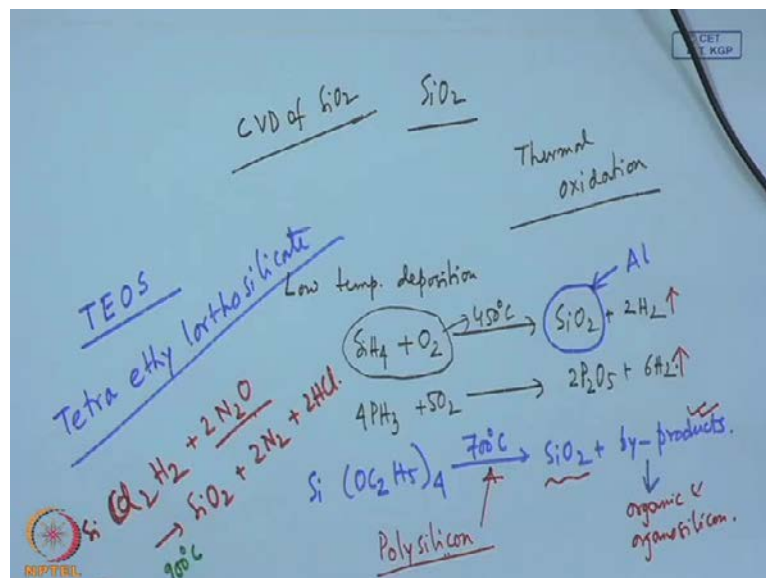
**LPCVD: suitable for polysilicon gates  
requiring a uniform insulating layer with good  
step coverage.**

**High temperature deposition (900 °C):  
dichlorosilane**



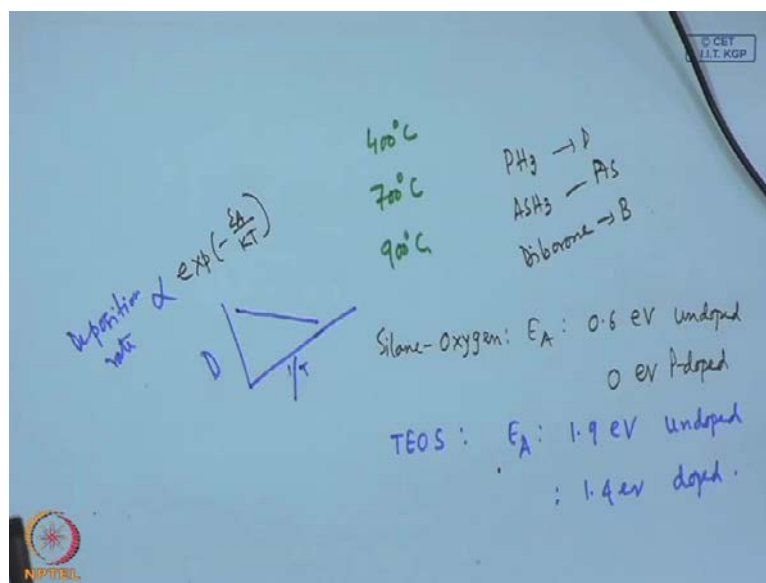
However, in this case we see that good step coverage is this, is there or in case of this TEOS growth and you see that CVD or LPCVD that means either chemical vapour deposition, it is basically the atmospheric pressure or the low pressure or reduced pressure CVD are used for making low temperature. However, for intermediate temperature one must use the LPCVD, the atmospheric pressure CVD is not used. And obviously for high temperature deposition say about around 900 degree centigrade dichlorosilane are used.

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This dichlorosilane which are nothing but the  $\text{SiO}_2$ ,  $\text{SiCl}_2\text{H}_2$  that is dichlorosilane and this dichlorosilane is used for making the growth of  $\text{SiO}_2$  with  $\text{N}_2\text{O}$  the nitrous oxide when we get  $\text{SiO}_2$  plus  $\text{N}_2$  plus  $\text{HCl}$ . So, this is basically the high temperature growth where the temperature is almost 900 degree centigrade. So, three different temperatures we have used.

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One is the 400 degree centigrade, another is 700 degree centigrade and third one is 900 degree centigrade. Three different precursors also we have used and in this TEOS growth we can find that the good step coverage and this step coverage comes from the migration of the reactant atoms or the vapour atoms on the surface where we can deposit the  $\text{SiO}_2$ . Then one can dope  $\text{SiO}_2$  also. The doping can be done using phosphorous that means the precursor material is phosphine or arsine or diborane that means for phosphorous or arsenic or boron, this is arsenic or boron.

So, diborane can be used and the deposition rate has been found to vary with the deposition rate in this case  $\text{SiO}_2$  deposition rate is vary as exponential minus  $E_A$  by  $KT$  where  $E_A$  is the activation energy and this activation energy is different for different materials; for silane oxygen reaction the activation energy is 0.6 electron volt when it is undoped and the activation energy is 0 electron volt that means no energy is required if it is doped that means phosphorous doped.

Similarly, we can say that the activation energy of TEOS decomposition to obtain the  $\text{SiO}_2$  the activation energy in this case is quite high compared to silane oxygen reaction it is 1.9 electron volt for an undoped and it is 1.4 electron volt if doped. So, always we find that the deposition rate, it is deposition rate is a function of the activation energy exponential minus  $E_A$  by  $K T$ . That means one can obtain the deposition rate versus temperature one, if you, if one can plot  $1/T$ , then it will be a straight line and from the straight line slope one can determine the activation energy.

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### Properties of $\text{SiO}_2$ films

Property	Thermally grown (1000 °C)	$\text{SiH}_4 + \text{O}_2$ (450 °C)	TEOS (700 °C)	$\text{SiCl}_2\text{H}_2 + \text{N}_2\text{O}$ (900 °C)
Composition	$\text{SiO}_2$	$\text{SiO}_2(\text{H})$	$\text{SiO}_2$	$\text{SiO}_2(\text{Cl})$
Density (g/cm <sup>3</sup> )	2.2	2.1	2.2	2.2
Refractive index	1.46	1.44	1.46	1.46
Dielectric strength (10 <sup>6</sup> V/cm)	>10	8	10	10
Etch rate (Å/min) (100:1 $\text{H}_2\text{O}:\text{HF}$ )	30	60	30	30
Etch rate (Å/min) (buffered HF)	440	1200	450	450
Step coverage	---	Nonconformal	conformal	conformal



From S.M. Sze, Semiconductor Devices: Physics & Technology, 2<sup>nd</sup> edition (Wiley)

Now, another important concept that we can use that the high temperature growth which is 900 degree centigrade and we have seen that in that case the dichlorosilane is used. Now, if we compare the properties of  $\text{SiO}_2$  which is shown in this view graph. You can see that this properties of  $\text{SiO}_2$  films four types of growth mechanism we have adopted. One is the thermally grown which is carried out at 1000 degree centigrade quite high temperature or silane oxygen reaction, which is a low temperature process 450 degree centigrade, another is the intermediate temperature range TEOS 700 degree centigrade. It is basically the decomposition or the reaction of nitrous oxide with dichlorosilane at 900 degree centigrade it is high temperature process.

So, four processes we have adopted and the properties we have enlisted in this table which can be described like this say composition in all the cases  $\text{SiO}_2$ . However, in case of silane oxygen reaction we find that hydrogen, some atomic percent of hydrogen

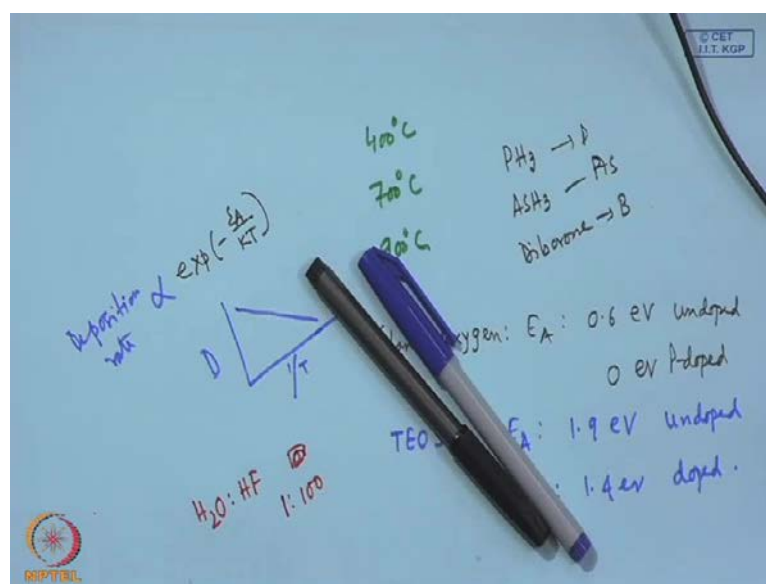


is obtained with SiO<sub>2</sub> that means it is hydrogen embedded SiO<sub>2</sub> or in the case of dichlorosilane a nitrous oxide reaction we see that some atomic percent of chlorine is obtained or presence, the presence of chlorine or hydrogen is there with SiO<sub>2</sub> in case of silane or dichlorosilane reaction respectively.

Now, if you see the density the density in gram per centimetre cube for thermally grown it is 2.2, for silane oxygen reaction it is 2.1, for TEOS decomposition it is 2.2 and for dichlorosilane nitrous oxide it is 2.2. So, except this case of silane oxygen reaction the density is almost same. However, there may be some porosity due to the presence of chlorine in case of the dichlorosilane nitrous oxide reaction. Refractive index we can find and the refractive index in, is in in most of the cases 1.46, for thermally grown it is 1.46, for silane oxygen reaction it is less 1.44, for TEOS decomposition it is 1.46 and for dichlorosilane nitrous oxide reaction it is 1.46.

Now, if we come to the dielectric strength which is measured at 10 to the power 6 volt per centimetre then we see that thermally grown oxide has the superiority, it is greater than 10 the dielectric strength and the the lowest one is obtained in case of silane oxygen reaction which is 8. So, that means we can say that some porosity is developed during the reaction of silane and oxygen to obtain SiO<sub>2</sub>. However, for two other methods like the decomposition of TEOS or dichlorosilane with nitrous oxide the dielectric strength at 10 to the power 6 volt per centimetre is almost 10.

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Then another property is the etch rate, how fast one can etch  $\text{SiO}_2$  over some material because we know that for doping of silicon generally  $\text{SiO}_2$  masking is made. Now, with this doping of silicon you can see that the etching is very, very important because after masking you have to remove the  $\text{SiO}_2$  from the surfaces. So, that means for making some window or making some masking on  $\text{Si}$ ,  $\text{Si}$  for doping of say p type, n type, for ion implantation, for diffusion one can use some kind of  $\text{SiO}_2$  layer over silicon.

So, then the etch rate which is 30 angstrom per minute if you use a solution of  $\text{H}_2\text{O}$  and  $\text{HF}$  with the ratio of 100, 1 is to 100 that means take 1 ml of, 1 ml of water and 100 ml of  $\text{HF}$  then make a solution with that solution the etch rate is found to be 30 angstrom per minute in all the cases except silane oxygen where it is 60 angstrom per minute that means per minute 60 angstrom can be etched out. So, that means the porosity is there.

Obviously it is obtained from the, it is, it is confirmed by the other data also like the dielectric strength, like the density is less so the etch rate will be higher. However, if we use a buffered  $\text{HF}$  the etch rate becomes very high almost 450 in case of thermally grown, TEOS and dichlorosilane, but in case of silane oxygen reaction it is 1200 angstrom per minute.

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#### Buffered HF

Buffered oxide etch (BOE), or BHF, is a wet etchant used in microfabrication. Its primary use is in etching thin films of silicon dioxide ( $\text{SiO}_2$ ) or silicon nitride ( $\text{Si}_3\text{N}_4$ ). It is a mixture of a buffering agent, such as ammonium fluoride ( $\text{NH}_4\text{F}$ ), and hydrofluoric acid ( $\text{HF}$ ).

Concentrated  $\text{HF}$  (typically 49% water) etches silicon dioxide too quickly for good process control. Buffered oxide etch is commonly used for more controllable etching.

Some oxides produce insoluble products in  $\text{HF}$  solutions. Thus,  $\text{HCl}$  is often added to BHF solutions in order to dissolve these insoluble products and produce a higher quality etch.

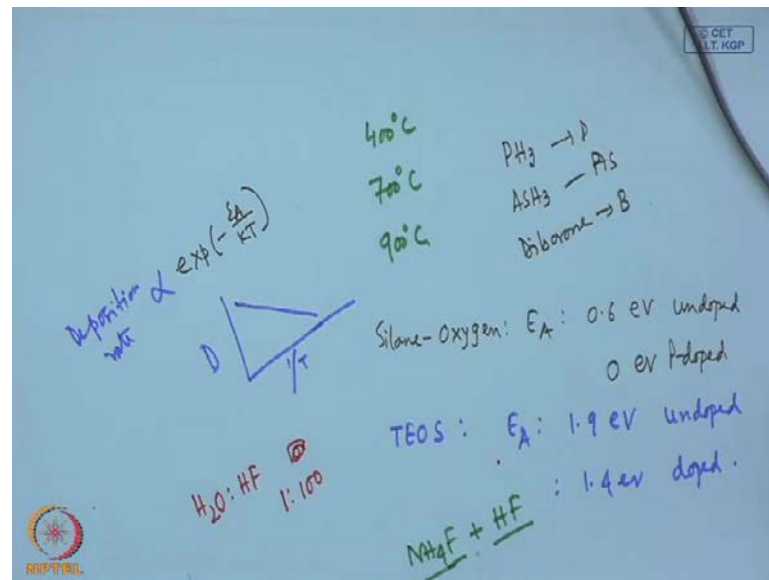
A common buffered oxide etch solution comprises a 6:1 volume ratio of 40%  $\text{NH}_4\text{F}$  in water to 49%  $\text{HF}$  in water. This solution will etch thermally grown oxide at approximately 2 nanometres per second at 25 °C. Temperature can be increased to raise the etching rate. Continuous stirring of the solution during etching process helps to have homogeneous solution which may etch uniformly by removing etched material from the surface.



Now, let us talk about the buffered  $\text{HF}$ . What is buffered  $\text{HF}$ ? Buffered  $\text{HF}$  is also known as buffered oxide  $\text{H}$  and it is a wet etchant used in microfabrication in

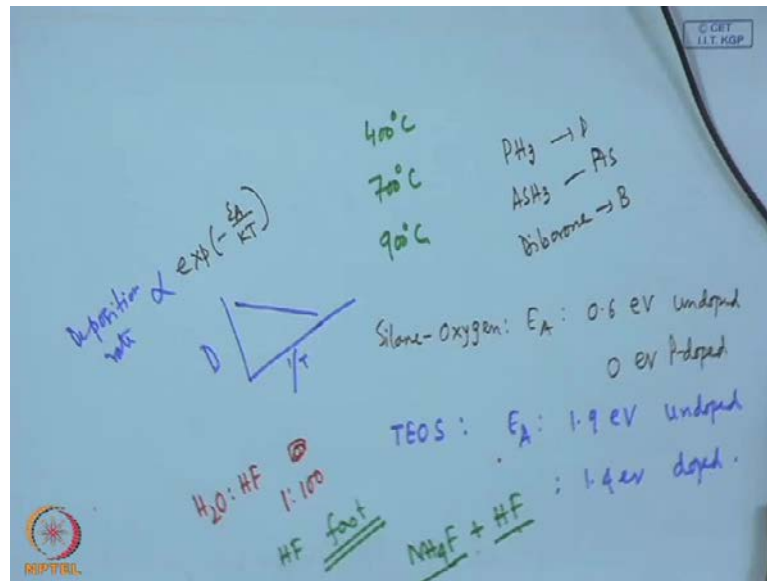
semiconductor industry. Its primary use is in etching thin films of silicon dioxide or silicon nitride. It is a mixture of a buffering agent such as ammonium fluoride and hydrofluoric acid. So, when we talk about the buffer solution it is nothing but a solution made of ammonium fluoride plus hydrofluoric acid.

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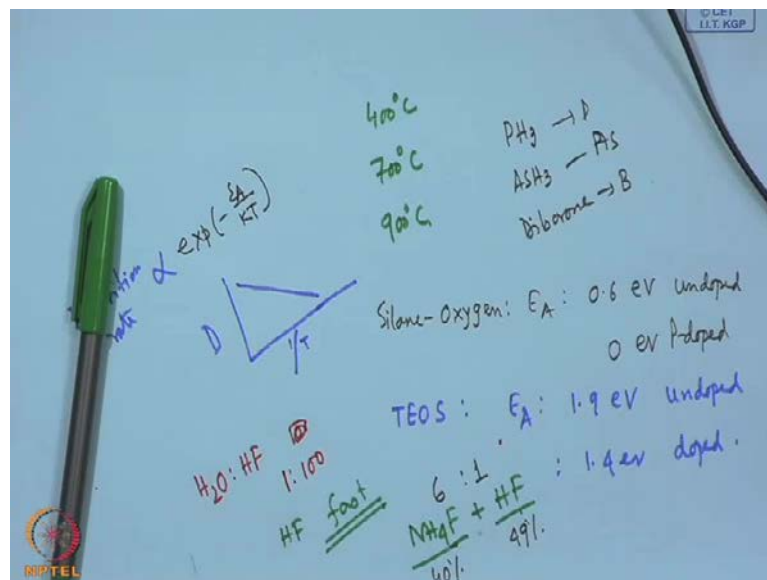
So, so composition must be changed or or or monitored in such a way that a particular percentage of ammonium fluoride is mixed with the H F, with the H F solution to obtain the buffered solution. Now, control hydrofluoric acid where typically 49 percent water is there, then etches silicon dioxide too quickly for good process control. Buffered oxide H is commonly used for more controllable etching.

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So, the difference between normal H F etching and buffered H F etching is that it is fast. If you use hydrogen fluoride simple solution then the etching is fast.

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However, in case of buffered solution it is controllable. The the rate is not so high. Then some oxides produce insoluble products in H F solutions thus H C l is often added to buffered H F solution in order to dissolve these insoluble products and produce a higher quality H. A common buffered oxide H solution comprises a 6 is to 1 volume ratio of 40 percent N H 4 F, so that means one can take 40 percent in water and 49 percent of H F in

water and then 6 is to 1 volume that means 6 m l of N H 4 F with 1 m l with that of H F with that ratio and this solution will etch thermally grown oxide at approximately 2 nanometres per second, 2 nanometres per second at 25 degree centigrade.

Now, if you want to increase the etch rate say, if you want faster etch rate then you have to increase the temperature from 25 degree to say 30, 40, 50 degree that means you need some heating and at the same time you can stir the solution for the faster etching of the S i O 2. So, continuous stirring of the solution during etching process helps to have homogenous solution which may etch uniformly by removing etched material from the surface.

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### Properties of SiO<sub>2</sub> films

Property	Thermally grown (1000 °C)	SiH <sub>4</sub> + O <sub>2</sub> (450 °C)	TEOS (700 °C)	SiCl <sub>2</sub> H <sub>2</sub> + N <sub>2</sub> O (900 °C)
Composition	SiO <sub>2</sub>	SiO <sub>2</sub> (H)	SiO <sub>2</sub>	SiO <sub>2</sub> (Cl)
Density (g/cm <sup>3</sup> )	2.2	2.1	2.2	2.2
Refractive index	1.46	1.44	1.46	1.46
Dielectric strength (10 <sup>6</sup> V/cm)	>10	8	10	10
Etch rate (Å/min) (100:1 H <sub>2</sub> O:HF)	30	60	30	30
Etch rate (Å/min) (buffered HF)	440	1200	450	450
Step coverage	---	Nonconformal	conformal	conformal



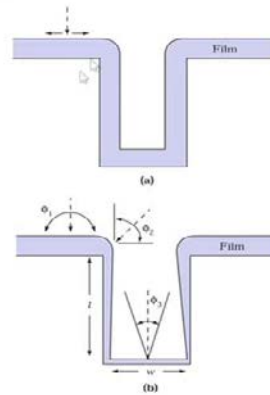
From S.M. Sze, Semiconductor Devices: Physics & Technology, 2<sup>nd</sup> edition (Wiley)

So, if we use a buffered H F, so then it is say 450 angstrom per minute or 440 angstrom per minute, but if you use a only solution of H F then it will be more fast and then the control will be lost. Now, another important property is the step coverage. The step coverage means that how the the semiconductor piece or how the substrate is covered. In thermally grown oxides obviously there is no need for the step coverage that, because that is the physical vapour deposition. So, the step coverage cannot be compared with other CVD processes. Here the CVD processes you see that it is non conformal for saline oxygen reaction. However, for TEOS or dichlorosilane it is conformal. Now, what is conformal, what is non conformal?

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### Step Coverage

**Uniformity of the film thickness regardless of topography of the surface is due to rapid migration of reactants after adsorption on the step surfaces. Reactants arrive along different angles**

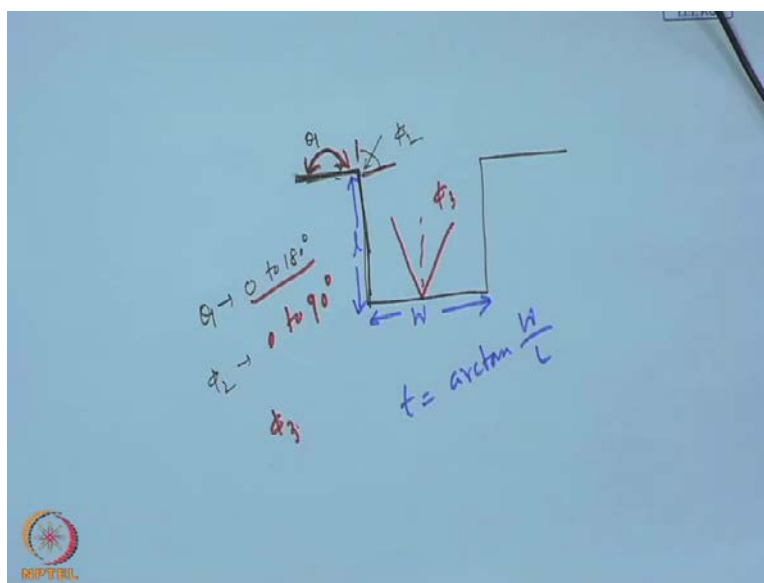


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The, it is the conformal. Conformal means where the thickness of the grown film is uniform regardless of the topography of the surface, regardless of the topography of the surface the uniformity is there. However, in the figure which is shown below in section b one can find that in some of the regions it is not uniform like here or at this window area it is not uniform, but the surfaces parallel to the plane then it is the uniform film which has been grown. Now, why is this kind of step coverage is obtained for different processes? Actually, this step coverage will be uniform or conformal if rapid migration of the reactants takes place after adsorption on the step surface.

Suppose, one molecule of reactants comes here it is adsorbed and then it takes the rapid migration. Then it migrates very rapidly throughout the length and breadth of the surface. However, if that migration of the vapour molecules does not take place very fast then there will be non conformal step coverage. And here you see that in silane oxygen reaction it is non conformal, in TEOS and dichlorosilane it is conformal. So, that means during reaction of silane with oxygen the migration of the reactant molecules will not be there, rapid migration is not found, so there will be non conformal.

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So, and you see that the thickness will depend on the reactants arriving along different angles, arriving along different angles. In this case one can see that say for this surfaces which is parallel to the plane let it comes at an angle  $\theta_1$  and  $\theta_1$  can have value between 0 to 180 degree. Obviously, when we consider this vertical plane, this vertical surface then here we find that the reactant molecules will come at an angle  $\phi_2$ , but  $\phi_2$  will have values between say 0 to 90 degree.

So, obviously one can see that it will be double, the thickness here will be double because thickness will be dictated by the arctan value and since it is wide angle is there. So, the thickness will be more. Here the thickness is restricted because the reactants molecules are arriving on the vertical surface at a, an angle  $\phi_2$  which is less than  $\phi_1$ . So, it can be double and in the picture also in the diagram also one can see that this thickness is half of that thickness.

And another case can be the opening the window area, the opening area and where the angle can be say  $\phi_3$  and this  $\phi_3$  will be any angle, but it is less than 90 degree obviously and the thickness in that case will be obtained by  $\arctan W/L$  where  $W$  is the width of the window or the opening area and  $L$  is the height or the distance up to the top surface. So, then thickness will be  $\arctan W/L$ . Now, this step coverage is obviously is a temperature activated process and because the rapid migration you need

the temperature because from rapid migration the energy is obtained from the temperature or the source is hid in this case.

So, we see that when TEOS is decomposed that means the temperature is 700 degree centigrade or when the dichlorosilane reacts with nitrous oxide at 900 degree centigrade the temperature at 700 or 900 is favourable for or rapid migration of the reactant molecules over the surface. However, in case of of silane oxygen reaction the temperature is very small 450 degree centigrade compared to the intermediate or high temperature region and in that case that energy is not sufficient for making rapid migration of the reactants over the surfaces.

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### Silicon Nitride

**Difficult to grow by thermal nitridation  
(using ammonia)**

**LPCVD: 750 °C. Films are stoichiometric  
( $\text{Si}_3\text{N}_4$ ), high density (2.9 – 3.1 g/cm<sup>3</sup>): mask  
for selective oxidation of silicon.**

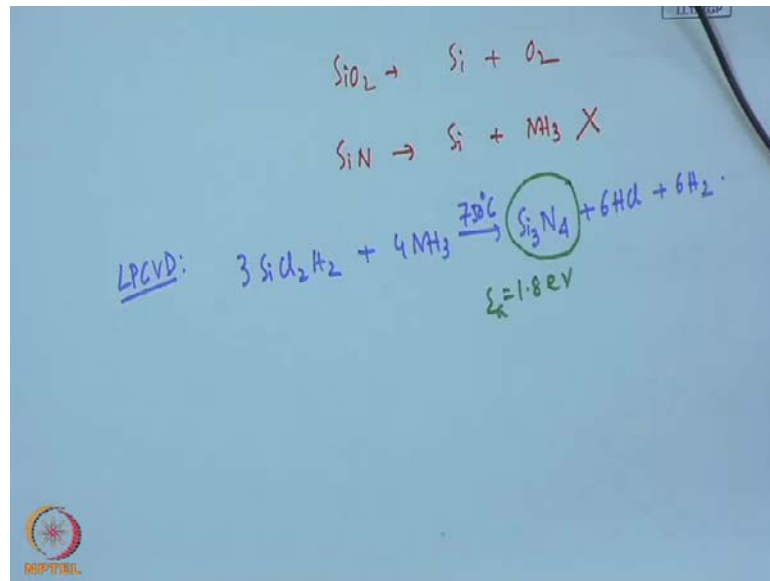
**Plasma-assisted CVD: 300 °C. Not  
stoichiometric, lower density (2.4 – 2.8  
g/cm<sup>3</sup>): excellent scratch protection,  
moisture barrier, and Na diffusion.**



Next is the silicon nitride film. This silicon nitride film it is not grown by nitridation, it is not grown by nitridation like oxidation.



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In case of  $\text{SiO}_2$  we have seen that silicon reacted with oxygen. So, it is oxidation. However, silicon nitride is not silicon with ammonia say not possible because there is very difficult and very high temperature requirement is there, special apparatus is there. So, it is very difficult to grow by thermal nitridation. So, what are the processes one can use the LPCVD or the low pressure chemical vapour deposition or the plasma assisted CVD. Now, in plasma assisted CVD one can follow that more energy is supplied apart from the thermal energy because plasma energy is coupled with the thermal energy.

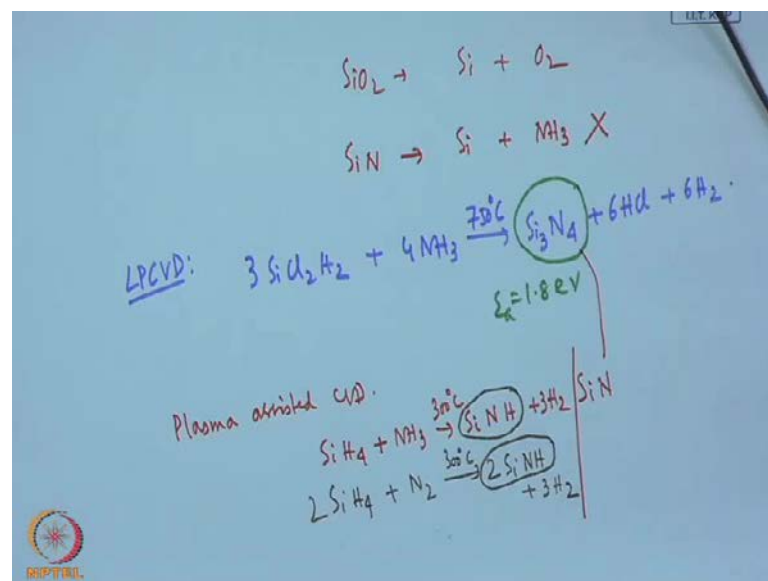
So, more energy is supplied for making the reaction to happen. In case of LPCVD low pressure CVD the reaction can be by dichlorosilane, so  $3 \text{SiCl}_2\text{H}_2$  which reacts with  $\text{NH}_3$ . Remember, that this is not a direct nitridation it is LPCVD or low pressure chemical vapour deposition. It takes place at 750 degree centigrade and in this case you will get  $\text{Si}_3\text{N}_4$  and this is the silicon nitride apart from the by products hydrogen chloride and hydrogen and this activation energy for this reaction is 1.8 electron volt activation energy. This silicon nitride  $\text{Si}_3\text{N}_4$  is basically stoichiometric.

It is stoichiometric and you can see that the, because it is stoichiometric we can write the formula as  $\text{Si}_3\text{N}_4$  and it is the, it is high density 2.9 to 3.1 gram per centimetre cube. So, the films are stoichiometric that is why we can say that  $\text{Si}_3\text{N}_4$  is the formula for this LPCVD grown silicon nitride. The density is high 2.9 to 3.1 gram per centimetre cube and it is used as a mask for selective oxidation of silicon. Selective

oxidation of silicon means if you mask with Si<sub>3</sub>N<sub>4</sub> on a silicon; let us take a piece of silicon. Suppose, this is a piece of silicon and we want to oxidize it and we want to mask it for diffusion. Suppose, this area we want to mask, this area we want to mask and this area we want to mask; that masking can be done by Si<sub>3</sub>N<sub>4</sub>, why? Because Si<sub>3</sub>N<sub>4</sub> etch rate is very small.

The etch rate of Si<sub>3</sub>N<sub>4</sub> is very small and so the underlying silicon layer, this white white piece of paper say it is silicon layer, the underlying silicon layer will not have any etching if you coat this silicon surface with Si<sub>3</sub>N<sub>4</sub>. So, that is a important for this silicon nitride, it is used for masking for selective oxide. Another is the plasma assisted CVD which is a low temperature process as mentioned earlier that plasma energy is coupled with thermal energy. So, one can use very small temperature or just 300 degree centigrade, but remember that this plasma assisted CVD is not a stoichiometric compound. It is a non stoichiometric compound so the formula one cannot write like this.

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Rather, Si<sub>3</sub>N<sub>4</sub> is used. So, it is plasma assisted CVD. In this case the reaction takes place like this SiH<sub>4</sub> that means silane we use and it reacts with ammonia at 300 degree centigrade to obtain SiNH plus 3 H<sub>2</sub> or one can use this kind of a reaction like SiH<sub>4</sub> twice plus nitrogen to obtain twice SiNH plus 3 H<sub>2</sub>. So, that means this is silane reaction that means in both the cases this plasma assisted CVD we find that silane is

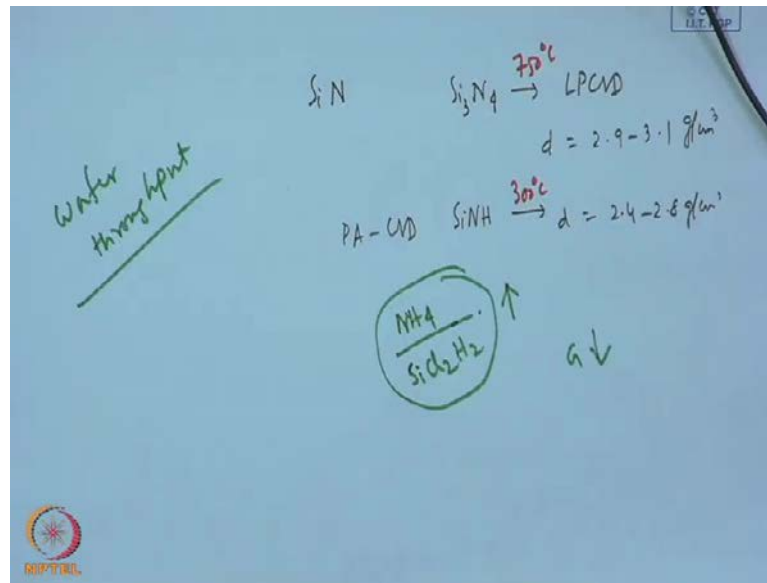
reacting with either ammonia or with nitrogen to obtain silicon nitride, but from the output or the product what we are getting from this reaction you see that this is Si<sub>3</sub>N<sub>4</sub>.

So, substantial amount of hydrogen is there, obviously and that is why it is the non stoichiometric film. It is not stoichiometric like LPCVD and it has lower density. The density is 2.4 to 2.8 gram per centimetre cube. You compare with the earlier one grown by LPCVD where it is 2.9 to 3.1 and this plasma assisted CVD is, has the excellent scratch protection, it has moisture barrier and sodium diffusion. So, that means it is resistance to moisture and also sodium diffusion. Therefore, we can say like this you grow Si<sub>3</sub>N<sub>4</sub>, it will be Si<sub>3</sub>N<sub>4</sub> if it is LPCVD.

In this case the density will be 2.9 to 3.1. However, if you grow by plasma assisted CVD it will be Si<sub>3</sub>N<sub>4</sub>H rather and the density will be 2.4 to 2.8 gram per centimetre cube in both the cases. So, that means it is porous compared to this LPCVD grown. Another important aspect is that here the temperature is very high 750 degree centigrade. Here, the temperature is 300 degree centigrade. So, for normal scratch protection that means this silicon nitride is grown over the device to protect it from any kind of scratches, moisture, humidity and it, this silicon nitride acts as a barrier for the diffusion of sodium etcetera.

So, these properties can be obtained even if you grown by plasma assisted CVD not necessary that for such cases one has to use the LPCVD which is very high temperature process. And LPCVD grown has the advantage that this silicon nitride is stoichiometric in nature and this silicon nitride can be used as the mask for Si processing. So, that is very interesting topic and you see that in LPCVD dichlorosilane and ammonia when it is used, it has very good uniformity, high wafer throughput. This is we must define with what is known as the wafer throughput.

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Wafer throughput is the number of wafers that one can handle at a time or suppose we want some processing say we want oxidation, how many number of wafers can be made to oxidation, how many number of wafers can be used at one go in one particular batch. So, that is the wafer throughput for any particular process. So, in this case here it is the high wafer throughput that means many wafers can be used at a time and the number of wafers at the process end will be very high. Then the control factors are temperature, pressure, reactant concentration and deposition rate increases with increasing total pressure or dichlorosilane partial pressure and decrease with an increasing ammonia to dichlorosilane ratio.

So, that is a important thing that deposition rate increases with increasing total pressure or dichlorosilane partial pressure, but decreases with an increasing ammonia to dichlorosilane ratio. So, that means is if you use a particular value of ammonia to dichlorosilane, if you increase it that means if and and if you increase this ratio, if this ratio is increased then growth rate will decrease. So, that means deposition of Si<sub>3</sub>N<sub>4</sub> will be less if you increase this ratio of ammonia to dichlorosilane.

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### Silicon Nitride

**Silicon nitride deposited by LPCVD is an amorphous dielectric containing upto 8 atomic percent hydrogen.**

**Etch rate: less than 1 nm/min in buffered HF.**

**High tensile stress:  $10^{10}$  dynes/cm<sup>2</sup> (10 times that of TEOS deposited SiO<sub>2</sub>).**

**Films thicker than 200 nm may crack due to high stress.**

**Resistivity :  $10^{16}$  Ω-cm, Dielectric constant 6, Dielectric strength:  $10^7$  V/cm.**



This N H 4 induced process, it is you see that it is silicon nitride deposited by LPCVD is an amorphous dielectric containing up to 8 atomic percent hydrogen. So, very high hydrogen percentage is there and the etch rate is less than 1 nanometer per minute in buffered H F, we have already defined what is buffered H F. It has high tensile stress, 10 to the power 10 dynes per centimetre square. It is basically 10 times that of TEOS deposited S i O 2 that means the tensile stress of TEOS deposited S i O 2 is 10 to the power 9 dynes per centimetre square whereas, for silicon nitride grown by this LPCVD process is 10 to the power 10 dynes per centimetre square.

Films thicker than 200 nanometre may crack due to high stress. So, very thick film of silicon nitride is not recommended. Now, if we come to resistivity we see that it is very high 10 to the power 16 ohm centimetre, dielectric constant is 6 and dielectric strength is 10 to the power 7 volt per centimetre. Then if we compare this value of say tensile stress, resistivity, dielectric constant etcetera with plasma assisted CVD because we have come across two processes one is plasma assisted another is the LPCVD. And in this case you see that the plasma assisted nitride silicon nitride deposition films it contains 20 to 25 percent hydrogen, atomic hydrogen is very high.

Here it is 8 atomic percent, here it is 20 to 25 atomic percent. Then if you come to the resistivity value the resistivity value is in this case it is 10 to the power 16 LPCVD, but here it can be 10 to the power 5 to 10 to the power 21 ohm centimetre depending on

silicon to nitrogen ratio. So, if one make silicon to nitrogen ratio very high, then it will be very high otherwise the value of the resistivity is not very good one,  $10$  to the power  $5$ . Then dielectric strength is  $10$  to the power  $6$ ,  $1$  into  $10$  to the power  $6$  to  $6$  into  $10$  to the power  $6$  volt centimetre.

In case of silicon nitride the dielectric strength is  $10$  to the power  $7$  volt per centimetre and tensile strength here it is  $10$  to the power  $10$  dynes per centimetre square. Here it is  $2$  into  $10$  to the power  $9$  dynes per centimetre square that means compared to LPCVD grown silicon nitride it is low, the low tensile strength. So, that means plasma assisted CVD which is grown by reacting silane with ammonia or silane with nitrogen, we can find that the quality of the film is not so good what we obtained from the LPCVD grown silicon nitride films.

So, that means quality wise if we consider the quality of the grown film from plasma assisted CVD that is very bad compared to the LPCVD grown, so far as the dielectric strength is concerned, so far as the tensile strength is concerned, so far as the resistivity is concerned, so far as the hydrogen amount is concerned. However, this atmosphere, this plasma assisted CVD films are good enough for making a the protective coating which is protective for any kind of scratches or it acts as a barrier for the moisture as well as the sodium and water.

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### Low-k & High-k Dielectrics

**In semiconductor processing both are essential:**

**Low-k: to minimize the time delay due to parasitic resistance (R) and capacitance (C) in multilevel interconnection architecture.**

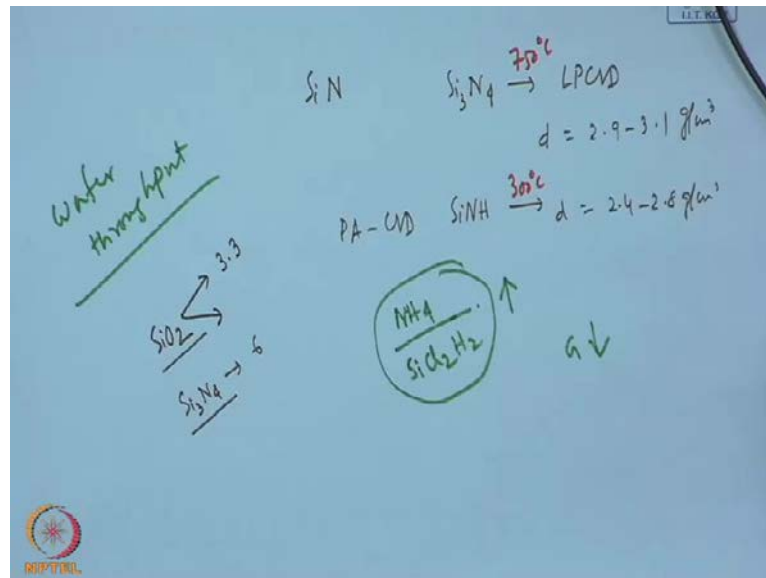
**Propagation delay due to increased RC time constant**

**Device interconnection network becomes a limiting factor in determining chip performance (device speed, power consumption, cross talk in ULSI)**



Then we come across the low-k and high-k dielectrics, that is very important thing in this in this discussion of the semiconductor device processing or the processing of semiconductor materials.

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This high-k and low-k, remember that S i O 2 is also a dielectric. Whatever be the method of process, you grow its 3.3 is the dielectric constant and S i 3 and 4 it is almost 6. So, almost double than S i O 2. So, this S i O 2 or S i 3 and 4 which we have discussed in detail are also dielectric films, but in semiconductor device processing two dielectrics we must discuss in detail, one is the high-k dielectric another is the low-k dielectric and both are essential.

In some of the cases we will find that say for MOS device, for making memory device, for making dynamic random access memory out of gallium arsenide MOS or silicon MOS. Then one must use the high-k dielectric. We shall justify that thing also, but for making very small devices for say sub micron region the interconnect is very important, the RC value, RC time constant of the interconnect must be low enough and for that case low dielectric strength material low-k materials are required. This thing one must take into account when discussing the different kinds of dielectrics available and also used for the processes of the semiconductor materials.

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**Propagation delay due to increased RC time constant**

**Device interconnection network becomes a limiting factor in determining chip performance (device speed, power consumption, cross talk in ULSI)**



Now, let us start from low-k. What is low-k dielectric? Low-k dielectric means the materials the dielectric materials having very low value of the dielectric constant. It is basically around 2, less than 2 or in some textbooks you will find that they have taken it as less than 3. So, any dielectric material having dielectric constant less than 3 can be termed as low-k dielectric. Above that it is known as the high-k dielectric. Now, the justification of this low-k dielectric is that to minimise the time delay due to parasitic resistance and capacitance in multilevel interconnection architecture and that is required for the submicron technology.

As we go down scaling the device to submicron technology the RC time constant must be minimised otherwise it will give you the time delay. Now, propagation delayed due to increased RC time constant. If you increase the RC time constant then there will be propagation delay and device interconnection network becomes a limiting factor in determining chip performance. Now, what is this limiting factor? The limiting factor is the time constant and if it is increased then many of the performance we have to sacrifice like device speed, power consumption, cross talk in ultra large scale integration. So, these are the things that one must take care.



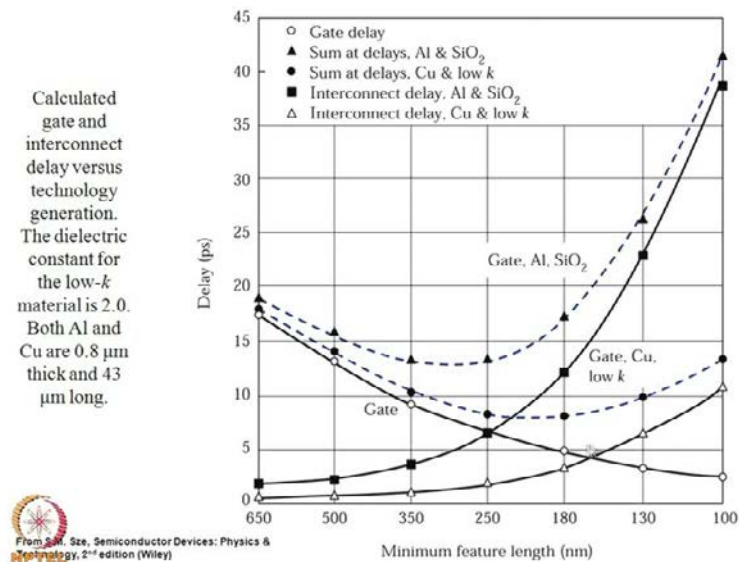
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- 
- Low-k dielectric
- Finished Device



So, so far as the RC time constant is concerned R is low because we take copper and C we have to make the choice. However, this must be some low-k.

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Here, you see that this figure on the y axis we have seen the delay in pico second and on the x axis we have shown the minimum feature length in nanometre. So, as the feature length decreases we see that this gate delay decreases, but the interconnect delay increases. Whether you use aluminium with S i O<sub>2</sub> or copper with S i O<sub>2</sub> or copper with a low-k material we can see that it increases. So, at around say 250 nanometre one can see that they are almost equal and if you go down, if you go down then the sum of the delays increases, sum of the delays means gate delay and as well as the interconnect delay.

So, two interconnects we have seen one is copper with low-k that means this triangular feature, open triangular shape and this is gate delay. So, one must play around here at say 170 or 160 nanometre they are almost equal, but if you go down we can see that this some delays with copper low-k and gate delay that means this blue dotted line, this is increasing and if you use aluminium with S i O<sub>2</sub> it is very, very high compared to low-k and copper. So, we see that the benefit of the gate delay because the gate delay is less if you can have minimum feature length towards say less than 100 nanometre or so but the benefits of this gate delay we cannot compensated by the interconnect delay rather due to interconnect delay the delay overall delay will be high.

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**To reduce RC time constant, interconnection materials with low resistivity and interlayer films with low capacitance are required.**

$$C = \frac{k\epsilon_0}{d} A$$

**A: area, d: thickness, k: dielectric constant,  $\epsilon_0$ : free space permittivity**

**How to reduce C?**

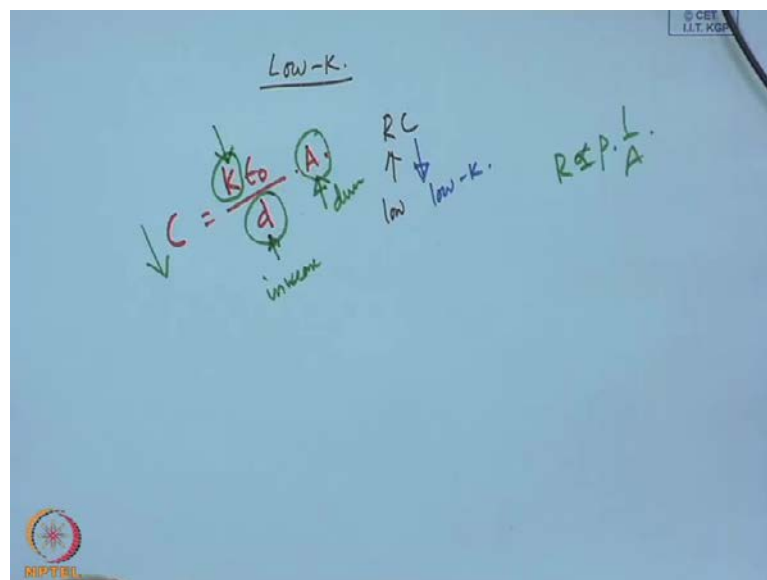
**By increasing d (gap filling will be difficult) & reducing A (interconnect resistance will increase)**



**Material with low-k is the solution**

Now, to reduce RC time constant interconnection materials with low resistivity and interlayer films with low capacitance are required. So, let us consider this point elaborately.

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We know that the capacitance can be written as  $k$  which is a dielectric constant and  $\epsilon_0$  it is the free space permittivity  $8.85 \times 10^{-14}$  farad per centimetre. Then divided by the thickness  $d$  multiplied by the area  $A$ . Now, how to reduce  $C$ ? How we can reduce  $C$ ? We can reduce  $C$  by reducing  $A$  which is for planar

technology not possible because in that case the interconnect resistance will be very high we know that  $R$  proportional to  $R$  equals to  $\rho$  into  $l$  by  $A$ .

So, if we reduce  $A$ , if we reduce  $A$  then the interconnect resistance will increase. So, that is not possible. If you decrease  $d$ , if you increase  $d$ , if you increase  $d$  or decrease  $A$  because we want to decrease  $C$ ; if you increase  $d$  then what will happen? Gap filling will be very very difficult. So, this  $d$  cannot be made to have any value, we cannot take  $d$  as any value and also  $A$  has the binding of the fact that interconnect resistance will increase if you reduce  $A$ .

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**To reduce RC time constant, interconnection materials with low resistivity and interlayer films with low capacitance are required.**

$$C = \frac{k\epsilon_0}{d} A$$

**A: area, d: thickness, k: dielectric constant,  
 $\epsilon_0$ : free space permittivity**

**How to reduce C?**

**By increasing d (gap filling will be difficult)  
& reducing A (interconnect resistance will increase**



**Material with low-k is the solution**

So, we have no other option, but to decrease  $k$ . This  $k$  is the low- $k$  to reduce  $C$ . So, material with low- $k$  is the solution that we find from this capacitance expression or if you consider the capacitance per unit area then the area terms goes and  $d$  you cannot make very very high because in this case the gap filling will be difficult and  $\epsilon_0$  is the free space permittivity which is constant. So, you have no other option, but to decrease the value of  $k$ .

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**Criteria:**

**Low dielectric constant, low residual stress, high planarization capability, high capability of gap filling, low deposition temperature, simplicity of process, ease of integration**



Now, what are the criteria? The criteria is that it must have low dielectric constant, low residual stress, high planarization capability, high capability of gap filling, low deposition temperature, simplicity of process and ease of integration.

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Low-k dielectrics: properties

Electrical	Mechanical	Thermal	Chemical	General
$k < 3$ and isotropic	good adhesion to metal or other dielectrics	low thermal expansion/shrinkage	no material change when exposed to standard chemistries	environmentally safe
high breakdown voltage	stability (low brittleness, crack resistance)	high thermal stability	no metal corrosion	commercially available
low leakage current	uniform thickness	high thermal conductivity	<1% moisture absorption	low cost
high reliability			low solubility in water	
			low defect density	



Now, if we look into the properties in detail, we can see that  $k$  less than 3 the electrical property of the dielectrics must be that such that if the, if the value of the dielectric constant must be less than 3 and it must be isotropic. So, far as the mechanical properties are concerned good adhesion to metal or other dielectrics. It must be stability that means

it must be stable. So, far as the stability is concerned it will have low brittleness and it must have crack resistance.

Also, the thermal property low thermal expansion or shrinkage, otherwise during processing if we increase or decrease the temperature there will be expansion or contraction. So, obviously there there will be crack or shrinkage and the device will not be a stable one and high thermal stability. Then so far as the chemical properties are concerned no material change when exposed to standard chemistries. No metal corrosion should be there.

It must be low solubility in water, low defect density etcetera. Apart from the general issues like it must be commercially available, it must have low cost, it must have environmental safety etcetera. And if we go back again to the electrical properties of low, low-k dielectric material apart from the value of the dielectric constant which must be less than 3 it must have high breakdown voltage, low leakage current and high reliability.

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Low-K.

$C = \frac{K \epsilon_0}{d}$

RC

low  $\uparrow$  low-K.

low  $\downarrow$  low-K.

RESP.  $\frac{1}{A}$ .


Because we know that when we use this expression  $C$  equals to  $k \epsilon_0 \frac{A}{d}$  this  $d$  you cannot take any value. If you increase  $d$  obviously there will be problem with the gap filling, otherwise you must have some optimization because very very low  $d$ , then the capacitance will increase at the same time the leakage current will increase and there will be breakdown also of the device. So, any value of  $d$  you cannot choose. One

must optimize between the thickness, the area and then one must come across the solution with the high low-k value of the dielectric.

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**Low-k materials**

Process	Materials	Dielectric constant
Vapour phase deposition polymers	Fluorosilicate glass (FSG)	3.5 – 4.0
	Parylene N	2.6
	Parylene F	2.4 – 2.5
	Black diamond (C-doped oxide)	2.7 – 3.0
	Fluorinated hydrocarbon	2.0 – 2.4
	Teflon – AF	1.93
Spin-on polymers	HSQ/MSQ	2.8 – 3.0
	Polymide	2.7 – 2.9
	SiLK (aromatic hydrocarbon polymer)	2.7
	PAE [poly(arylene ethers)]	2.6
	Fluorinated amorphous carbon	2.1
	Xerogels (porous silica)	1.1 – 2.0

 P. M. Sze, Semiconductor Devices: Physics & Technology, 2<sup>nd</sup> edition (Wiley)

In this view graph we have shown a large number of dielectric materials with low-k and value you see that apart from FSG it is 3.5 to 4 and other values are almost less than 3 and it has two types of processes one can have determinants, one can have spin-on dielectrics SOD or SOP spin-on polymers because these are the polymeric materials or one can have vapour phase deposition polymers like say parylene N, parylene F, black diamond it is the carbon doped oxide, fluorinated hydrocarbon, teflon etcetera. These are not spin-on polymers, these are vapour phase deposition, CVD must be used or VPE must be used or in case of say spin-on polymers one can have HSQ, MSQ, polymide. Then S i L K aromatic hydrocarbon polymer, poly arylene ethers those are from the dow chemicals etcetera, then xerogels, fluorinated amorphous carbon.

So, different types of materials are obtained and this is spin-on polymers that means using spin coating one can have this material all deposited on the surface. So, till now what we have discussed let us conclude for today's session. One thing is that though thermally oxide S i O 2 which is grown by thermal oxidation process has many edges so far as the electrical and other properties are concerned, it is very very superior, but apart from this thermally grown oxide one can have CVD to obtain S i O 2 of comparatively higher thickness.

And number two is that silicon nitride that can be grown by two methods one is plasma assisted CVD another is low pressure CVD and in plasma assisted CVD we have seen that the quality of the grown film are inferior to those obtained by LPCVD and at the same time though the quality wise it is inferior the plasma assisted CVD films, silicon nitride films. However, it can be used as a coating for scratch resistance or as barriers for moisture and sodium. Then we have started with the dielectric films. These dielectric films can be of low-k and high-k. Today, we have justified the low-k with different kinds of materials. Why, one need low-k for interconnection etcetera. In the next class we shall consider in detail the high-k dielectrics.

Thank you.