Processing of Semiconducting Materials
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Lecture - 36
Oxidation – II

In the previous class we have discussed about the effect of time on the oxide thickness. So, we have deduced two types of individual cases; one is the thickness as a function of temperature and we see that with time, what we find that when time is very small for small time of oxidation we find that there is a thickness which is depending on the time itself that means it is linear with time. The thickness which is growing is linear with time.

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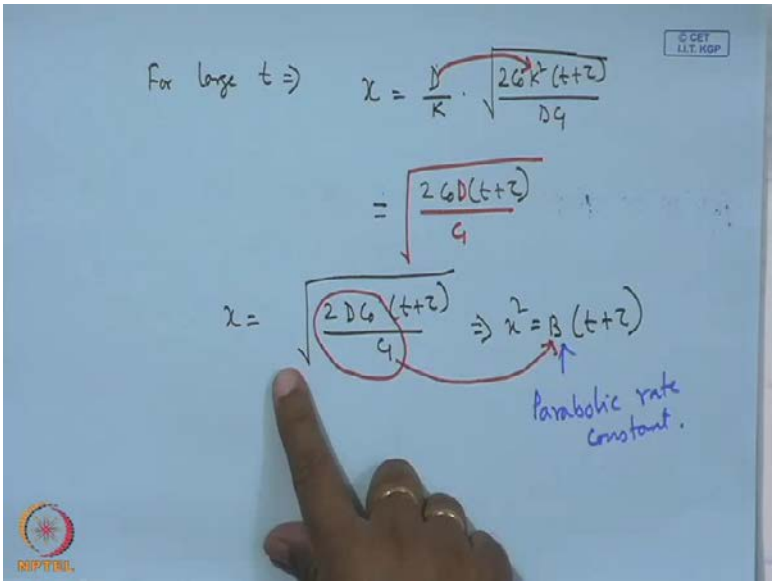

Now, when time is increased that means when we increase t for large t, what we have seen that x equals to this expression and which boils down to x square equals to b into t plus tau that mean it is the parabolic rate constant. Why we shall say it is a parabolic rate constant, because of the nature of this relation of the thickness with time.

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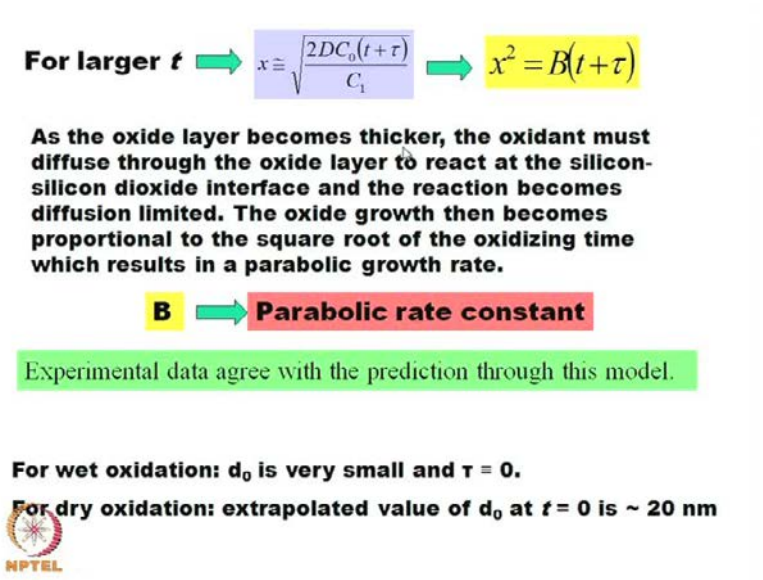

As the oxide layer becomes thicker, the oxidant must diffuse through the oxide layer to react at the silicon silicon dioxide interface and the reaction becomes diffusion limited. This thing, we have basically used here that when the there will be an diffusion of oxygen and this oxides, so there will be the diffusion of the oxygen with the oxides and when it passes through the diffusion passes through the silicon dioxide layer, there will be the diffusion.

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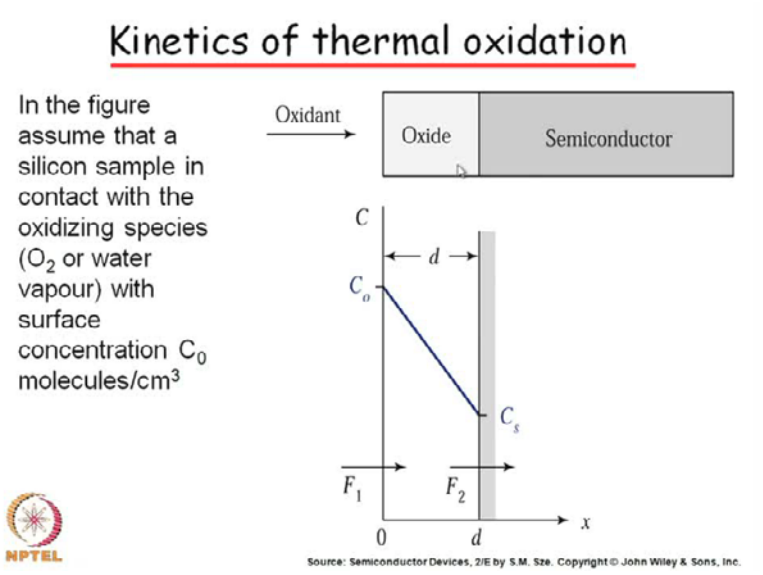

So, this is the diffusion path through which the oxidizing species will move through to the semiconductor surface because the reaction will take place at the semiconductor surface itself reaction between in this case silicon and oxygen or silicon with the oxygen in the water vapour or steam. So, when some layer is grown after initial formation of the oxide layer there will be diffusion and that so the reaction here will be the diffusion limited. The oxide growth then becomes proportional to the square root of the oxidizing time which results in a parabolic growth rate and as mentioned earlier that b is the parabolic rate constant.

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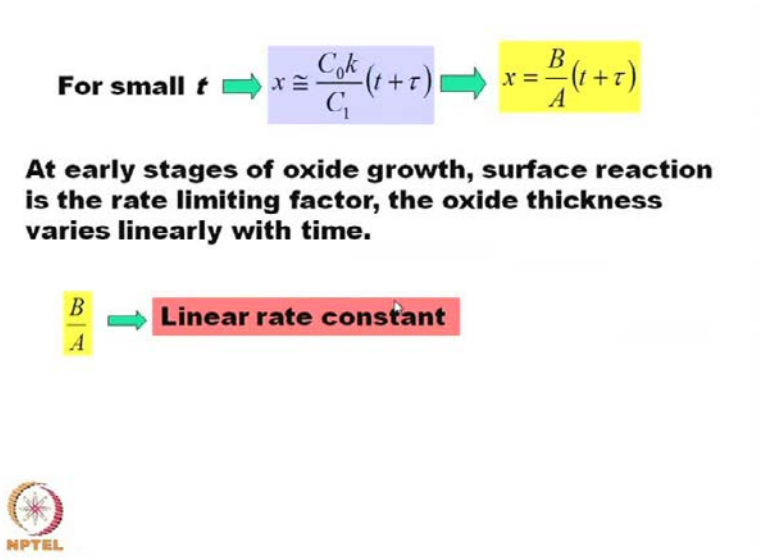

However, this parabolic rate constant or the linear rate constant B by A for small t those are basically agree with the prediction through this model. So with this model we came across two types of rate constant for small t, it is linear B by A for large t it is B, which is parabolic in nature. For wet oxidation this d 0 is very small for wet oxidation this d 0 is very small, you can consider it is almost 0.

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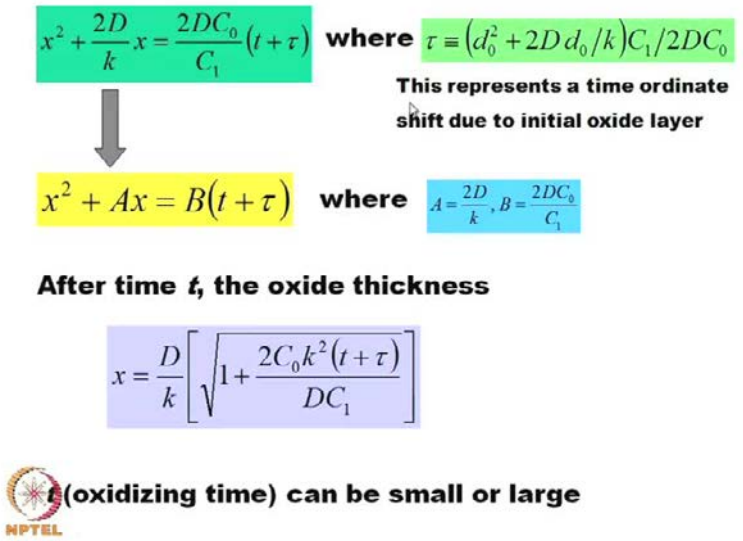

However, for dry oxidation extrapolated value of d 0 at t equals to 0 is almost 20 nanometres it is quite high.

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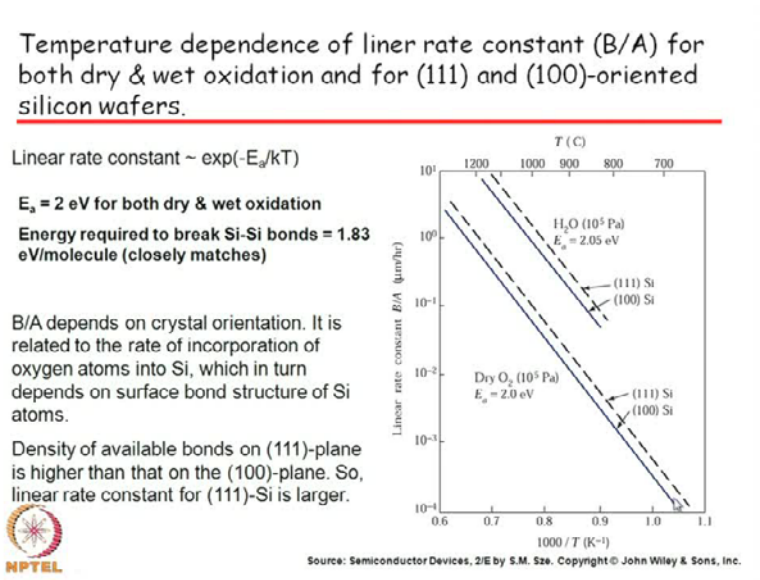

And you see that in this graph we have shown the linear rate constant that means B by A as a function of the temperature, it is basically thousand by t the unit is Kelvin inverse in this case it is micrometre per hour. The linear rate constant Bb by A, you see that the variation it is basically the temperature variation of the linear rate constant the variation is straight line.

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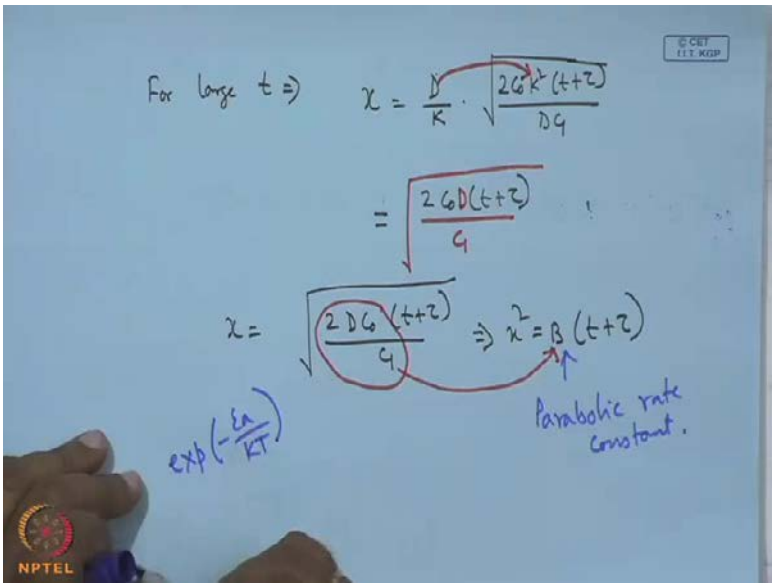

So, that means it follows the relation exponential minus E a by K T and this is Arrhenius type of relation and this E a is the activation energy, this e a is the activation energy. It follows in all the cases here the two cases have been shown in the blue lines, it is silicon 1 0 0 plane, on the dashed lines it is silicon 1 1 1 plane, so from this view graph we shall be able to understand why there will be a difference between the crystalline plane when silicon is 1 0 0, the value is low the linear rate constant value is low.

However when we take a piece of silicon having 1 1 1 plane, so at that plane 1 1 1 plane you see that the value of the linear rate constant is higher, in both the cases. And in the lower graphs it is basically the source material is the dry oxygen and it is 10 to the power 5 pascal pressure is applied. Whereas, in the upper two you see that water vapour is used having 10 to the power 5 pascal, the same pressure is used.

The activation energy calculated isit is at in both the cases 2 electron volt, in for dry oxygen source in both the 1 0 0 silicon or 1 1 1 silicon you see that the activation energy is 2 electron volt. Whereas, the activation energy for 1 0 0 or 1 1 1 silicon with the source as the water vapour or steam is 2.05 electron volt. So, we can conclude that the activation energy is 2 electron volt for both dry and wet oxidation. Now if we consider that the what is the energy required to break a silicon silicon bond?

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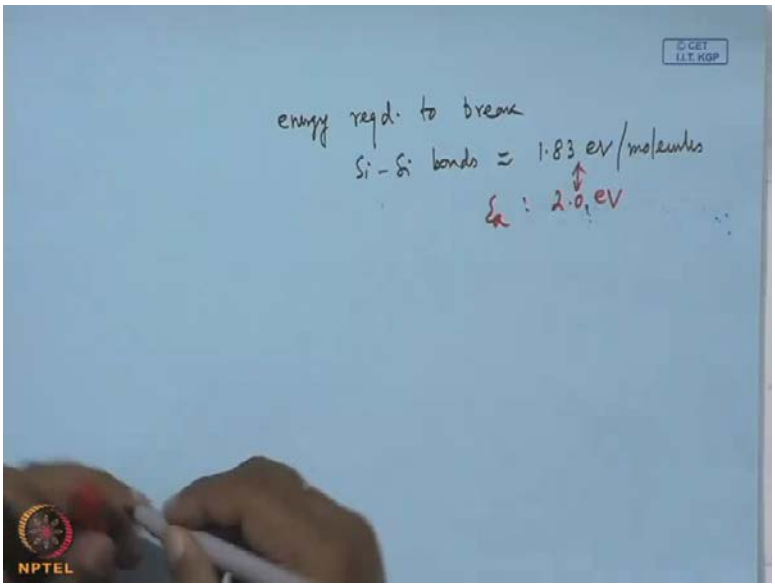

If you want to break a silicon silicon bond, the energy energy required to break silicon silicon bonds, it is almost 1.83 electron volt per molecules and what we are getting activation energy, we are getting 2 electron volt. So, they are basically closely matching. So, so they are basically closely matching that energy required to break the silicon silicon bonds and the activation energy for dry and wet oxidation. So, linear rate constant is basically the breaking of the silicon silicon bonds for reacting with the oxygen.

Now, B by A the linear rate constant it also depends on crystal orientation. It also depends on crystal orientation, it is related to rate of incorporation of oxygen atoms into silicon, which it which in turn depends on surface bond structure of silicon atoms. So, in this case we see that the value of the linear rate constant is higher whether it is dry or wet oxidation. The rate is higher for 1 1 1 silicon in both the cases. Why it is so? Because the density of available bonds on 1 1 1 silicon plane is higher than that on the 1 0 0 silicon plane. So, the linear rate constant for 1 1 1 silicon is larger. Obviously with this value there is a close matching between the experimental and this is the experimental curve and the theoretically obtained value of the silicon silicon bond, breaking energy and so it is consistent. So, this proves the efficacy of the model, which is which is able to describe the kinetics of oxidation in S i S i O 2.

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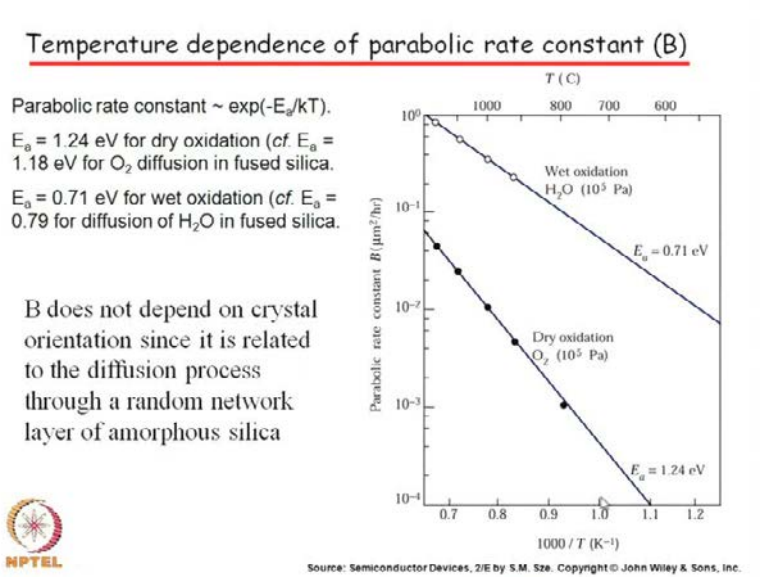

Now the same thing here it is the linear rate constant as a function of temperature, here we have plotted the parabolic rate constant as a function of temperature.

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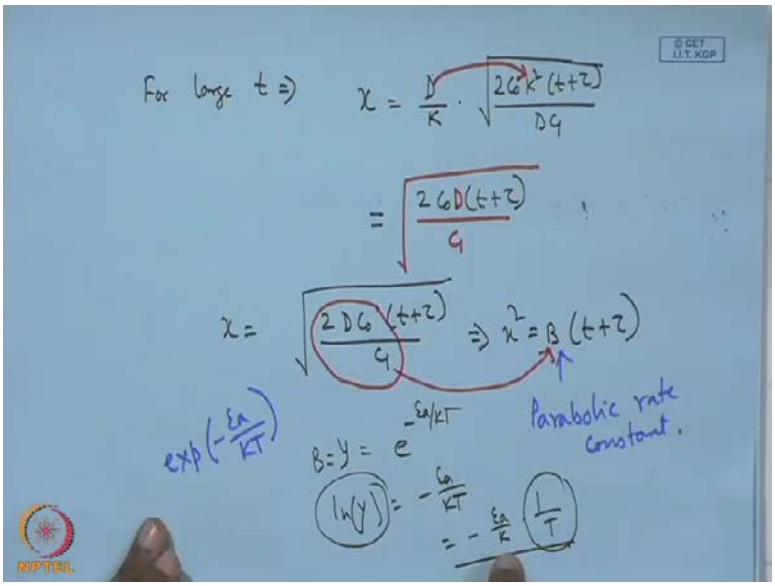

Here also we see that the variation is like the Arrhenius type exponential minus E a by K T because you see that in this case only it can be shown using a straight line plot like say something say y equals to E to that power minus E a by K T. So, you take log y it is equals to minus E a by K T. So, that means the activation energy E by k multiplied by 1

by T. So, if you plot 1 by T versus l n y, so it it is a log scale, if you it is basically they the parabolic rate constant that means y is nothing but B.

So, l n B it is the B value parabolic rate constant it is the log is taken and it is basically the with 1 by T it will be a straight line, so it is a straight line. The slope of this line minus E a by K. K is a constant and here you see that this E a value in this case that means the activation energy for dry oxidation is 1.24 electron volt. Whereas whereas, for wet oxidation the value is 0.71 electron volt.

So, if you compare with this thing here in both the cases, 2 electron volt here it is different. So, we shall explain the difference also when 1.24 electron volt is the activation energy for the dry oxidation that is the parabolic rate constant is constant and theoretically available value of oxygen diffusion in fused silica. It is 1.18 electron volt.

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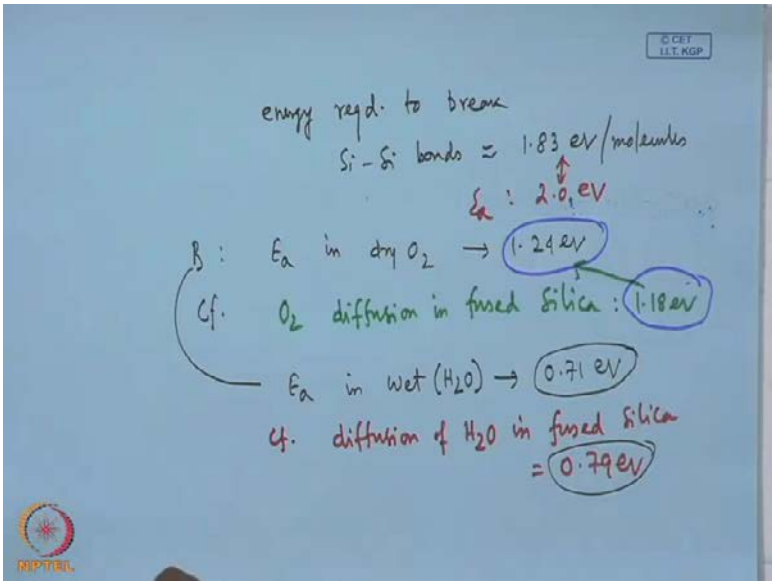

So, if you compare these two value that means for parabolic rate constant B the value of activation energy in dry oxygen it is 1.24 electron volt. You can compare this value with the value of the oxygen diffusion in fused silica that is 1.18 electron volt. So, we find that this is basically the diffusion of oxygen through fused silica as discussed earlier. In relation with the parabolic rate constant. Similarly, for B parabolic rate constant here the activation energy in wet oxidation that means if you use water vapour or steam it is basically you see that it is 0.71 electron volt.

So, it is 0.71 electron volt and you can compare this value with the diffusion of water vapour infused silica, what is its value? Its value is 0.79 electron volt, so this value is consistent with this value. Similarly, this value is consistent with this value, so it can account for the diffusion of either oxygen or water molecule through the S i O 2 layer to the S i surface. Now, you see that in this case B does not depend on crystal orientation, since it is related to the diffusion process through a random network layer of amorphous silica. Okay?.

So, in this case it depends on the crystal orientation but B does not depend on crystal orientation. Why because it is a diffusion process, it is a diffusion process and diffusion is always random through a amorphous silica and it also a random network layer through a random network layer of amorphous silica. So, obviously you can see that there should not be any dependence on the crystal orientation, so far as the parabolic rate constant is concerned.

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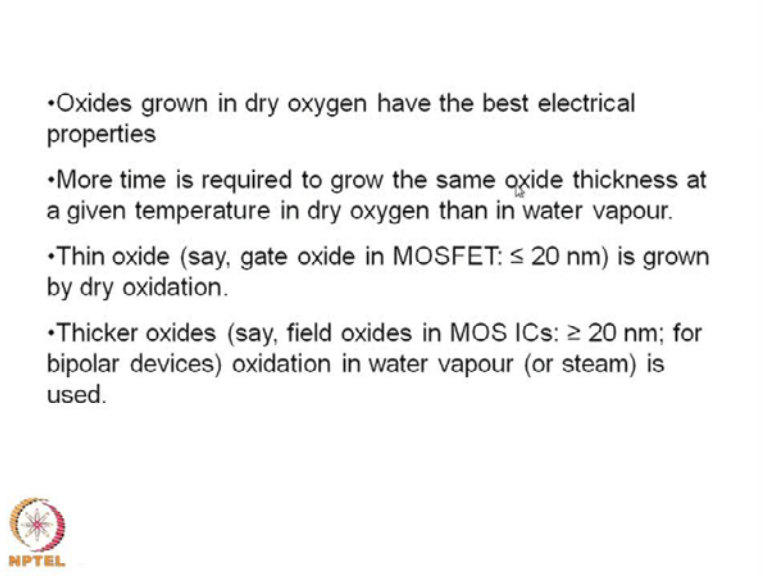

Now, oxides grown in dry oxygen have the best electrical properties. It has been experimentally observed that oxides grown in dry oxygen have the best electrical properties, more time is required to grow the same oxide thickness at a given temperature in dry oxygen than in water vapour. And thin oxide say gate oxide in MOSFET is generally less than 20 nanometre is grown by dry oxidation, because oxides grown in dry oxygen have the best electrical properties. And in a MOSFET, so far as the gate oxide is

concerned, we want that there must be very, very efficient electrical properties free form any kind of porosity etcetera, why because otherwise there will be leakage current enhancement, as well as the dielectric breakdown.

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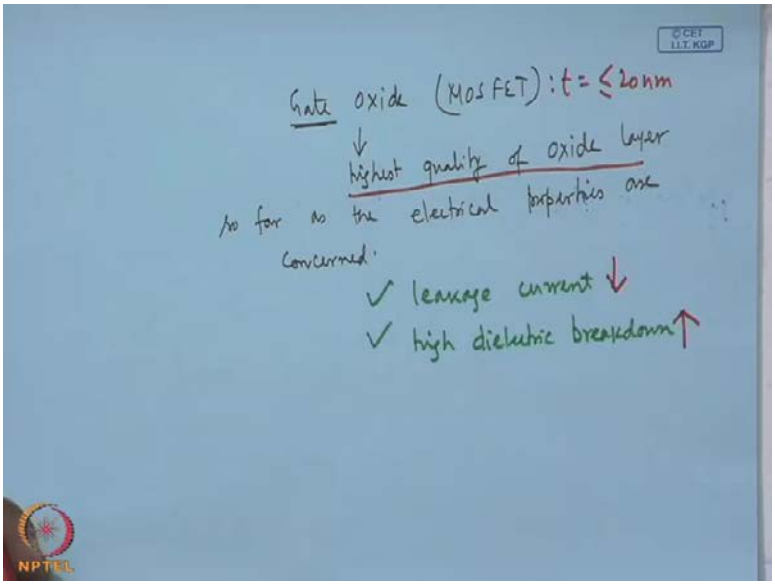

So, the property that we need for the gate oxide this gate oxide in a mos device so this gate oxide have the highest quality of oxide layer so far as the as the electrical properties are concerned. Why because in a mos device you can realise that one important thing is the leakage current, you have to reduce you have to reduce it you have to reduce it and another thing is there should not be dielectric breakdown. So, high dielectric breakdown high dielectric breakdown, so the dielectric breakdown will be high and this two can be achieved.

If we have some highest quality of oxide layer and that is the reason that oxides grown in dry oxygen is always used because this gate oxide thickness, if you consider the thickness t it is less than equals to 20 nanometre, very thin. However, for thicker oxides where the thicker oxides are used say field oxides in MOS IC's it is greater than twenty nanometre for bipolar devices and you can use the oxidation in water vapour or steam, because if we if we go back to the first slide from where we have started that in this case you see that this field oxide can be a thick oxide filed oxide can be thick oxide, because it is use for isolation with the adjacent device.

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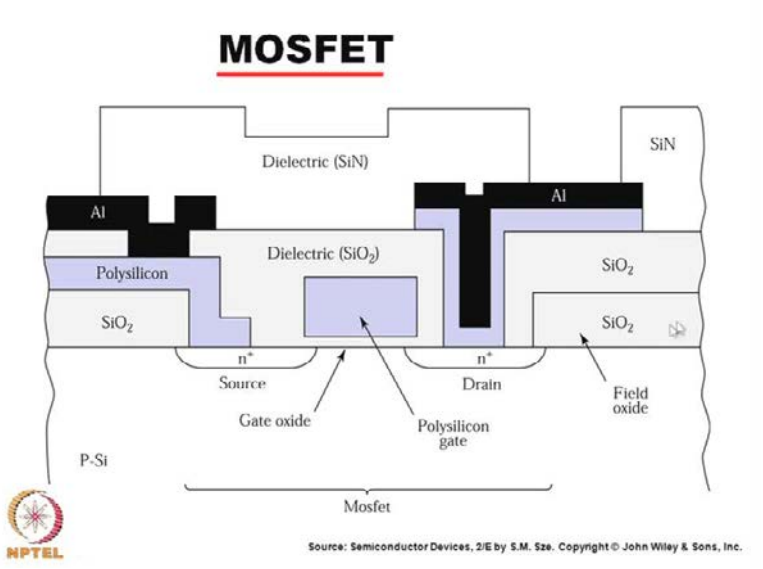

So, this is a device, consider this is device one and on both the sides there is device say this i device n. So, it can be device n plus 1, it is device n minus 1. So, there must be isolation between n minus 1 and n as well as n and n plus 1, so on both the sides there must be field oxide, which will give us the which will give us the value of the isolation reasonable. And you see that in this case, thicker oxides oxidation in water vapour or steam we can use because thicker oxides is there. So, first you can use say oxide grown in dry oxygen and then over dry oxygen you can grow water vapour, oxidation with water vapour for thick.

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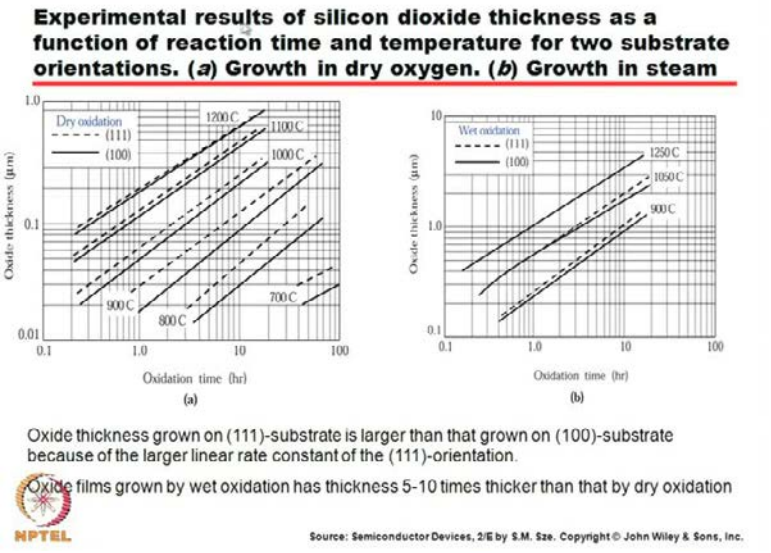

Now, in this figure you see that this is the experimental results of silicon dioxide thickness as a function of reaction time. So, on the x axis we have oxidation time and on the x axis we have oxide thickness in micron in both the graphs. The left one represents this is in dry oxidation and the right one is the wet oxidation and in both the cases both 1 0 0 and 1 1 1 plane of silicons were used.

So, in this case in the dry oxidation you see that the solid line and the dashed line it is basically there is a variation. So, it is 800 degree centigrade, it is 700 degree centigrade, it is 1200 degree centigrade. So, as the temperature of oxidation increases as the temperature of oxidation is oxidation increases, we see that the growth is more. So, at a particular time, say if we consider that at 10 hour, after 10 hour, this is 10 hour. If you grow at 800 degree centigrade, it is basically 0.3 0.1, 0.2, 0.3. However, at 10 hour for say 1200 degree centigrade it is very high almost 0.8 or 0.7 micron.

So, it is 0.2 micron, whereas, for the same time, but the temperature is different as the temperature increases the oxide thickness also increases and also you you can find that oxide thickness grown on 1 1 1, 1 1 1 means the dashed lines is 1 1 substrate is larger than that grown on 1 0 0 substrate because of the larger linear rate constant of one 1 1 1 orientation. We have seen that the rate constant linear rate constant in 1 1 1 is higher in case of, yes you see that here 1 1 1 and 1 0 0 plane, we have considered this is the linear rate constant and the linear rate constant is distinctively higher. It is distinctively higher and so since the linear rate constant is higher for 1 1 1 plane.

So, obviously here in 1 1 1 orientation the thickness of oxide grown on 1 1 1 is larger. However, in this case for wet oxidation you see that oxides films grown by wet oxidation has thickness 5 to 10 times thicker than that by dry oxidation. You consider any value say for 900 degree centigrade. So, 900 degree centigrade 1 hour, 900 degree centigrade 1 hour is basically 0.1 then 0.2 it is 0.3, so somewhere between 0.3 and 0.3 and 900 degree centigrade 1 hour. Here you see that this is 900 degree centigrade at 1 hour it is almost 0.02 or if you consider the 1 1 plane it is 0.3. So, several orders of magnitude at at least 5 to 10 times thicker than that by dry oxidation is obtained. If you grow by wet oxidation, so these are two important conclusion of the oxidation 1 by dry and another by wet.

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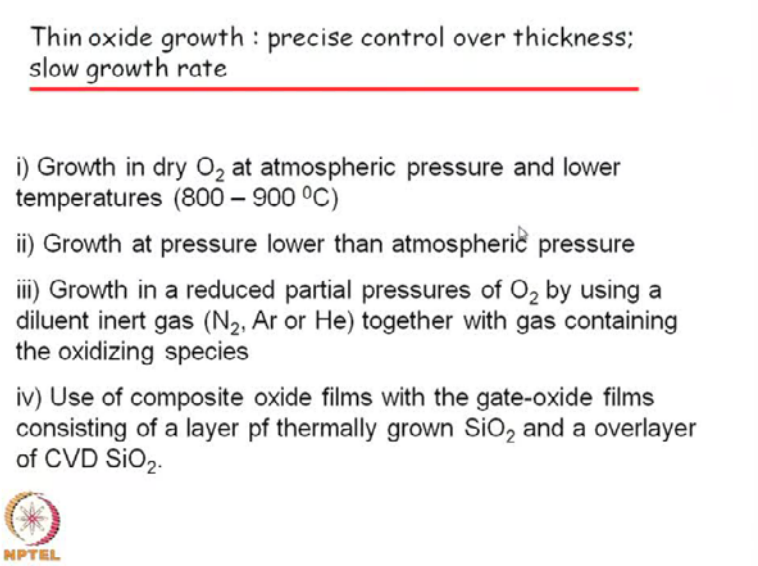

That wet oxidation thickness of the oxide planes grown by wet oxidation is always thicker than that the than that grown by dry oxidation and also since the diffusion through a random network of say amorphous sides in in S i O 2 layer is basically random in nature. So, we can say that the there is no bearing of the crystal orientation, so far as the B is concerned or the parabolic rate constant is concerned. Now, thin oxide growth precise control over thickness because the thickness is very important as we have seen that for our gallium arsenide, MOS devices it is basically if you use the gate oxide it is basically less than equals to 20 nanometre, so you must have very control.

So, so the growth rate must have some nanometre per second or say few nanometre per minute, so that precise control is possible. So, always slow growth rate is there, always you can have very slow growth rate. The general ambient or the general conditions optimum conditions that are used for the thin oxide growth is the growth in dry oxygen at atmospheric pressure and lower temperature because we have seen that the lower temperature the growth rate is small. However, for higher temperature the growth rate is very, very large. So, you cannot control at higher temperature, if you need say 2 nanometre, 5 nanometre, 3 nanometre of oxide thickness with this temperature you cannot be able to control always.

So, rather you use 800 to 900 degree centigrade and to use dry oxygen because in wet oxygen what happens wet oxidation thickness is 5 to 10 times thicker. So, do not go for

that and growth at pressure lower than atmospheric pressure because if you grow in a low atmospheric pressure condition or reduced atmospheric pressure condition there the growth rate will be further lowered. So, you use the moderate temperature as well as the lower atmospheric pressure, then the growth rate will be sufficiently low and you can control the growth rate another point is the growth in a reduced partial pressure of oxygen by using a diluent inert gas.

So, you can use helium or argon or nitrogen together with gas containing the oxidizing species. So, that means you reduce the partial pressure because the growth rate is directly proportional to the partial pressure. So, if you can reduce the partial pressure by diluting it, then obviously the growth rate will be quite low and use of composite oxide films with the gate oxide films consisting of a layer of thermally grown S i O 2 and a over layer of CVD S i O 2.

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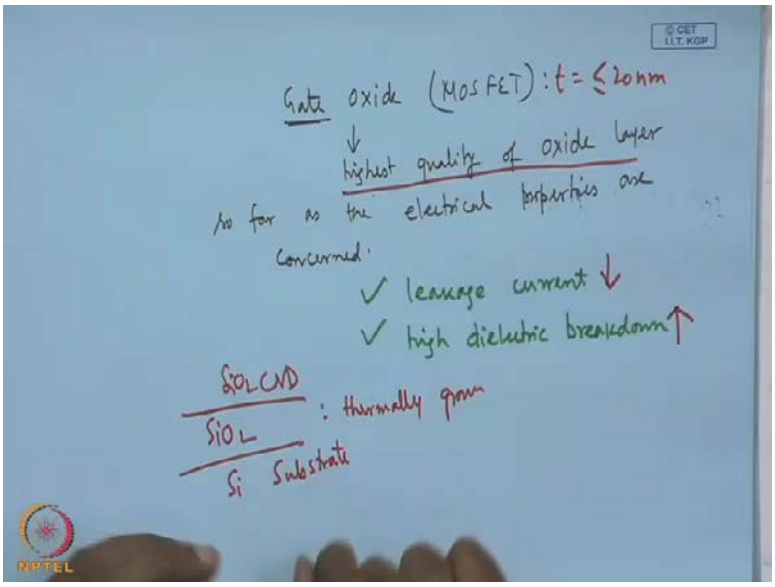

So, that means you can have gate oxide films consisting of a layer of thermally grown S i O 2, so first you use a thermally grown S i O 2 layer this is your silicon substrate, so this S i O 2 is thermally grown. Then above S i O 2 thermally grown you can use CVD is also S i O 2, but it is not by thermally grown it is by CVD. So, these are the techniques that one can use for making the silicon oxide film which can have very controlled growth because in all the cases we have seen that we get very, very small.

And this age of in, this age of miniaturization we have say 2 nanometre or 3 nanometre or 5 nanometre growth, so precise control one is the temperature you reduce, number two is the you dilute the oxygen by say argon or helium or nitrogen or you say the you take the growth pressure lower than the atmospheric pressure. That means you grow at reduced pressure or you grow if you need a thick oxide layer, then you use the thermally grown S i O 2 and then over there CVD grown S i O 2.

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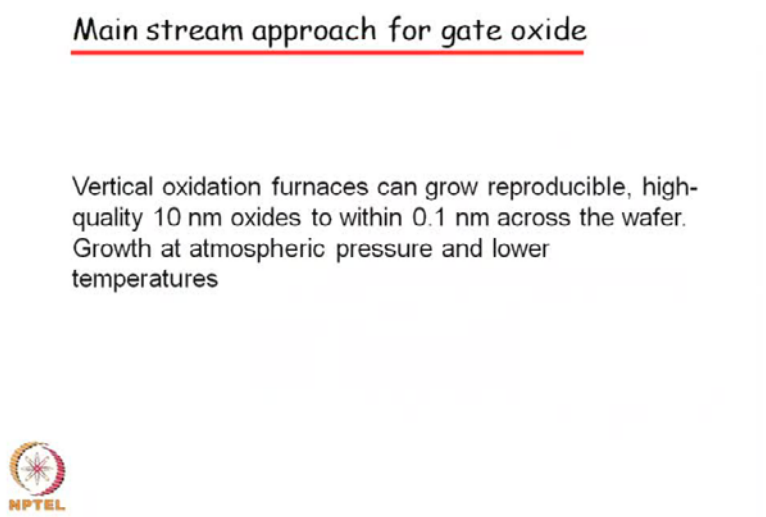

So, these are the approach that one can have say gate oxide very thin and very controlled growth and the main stream approach for gate oxide is that what is the main stream approach for gate oxide? The main stream approach for gate oxide is vertical oxidation furnace can grow reproducible high quality ten nanometre oxides to within point 1 nanometre across the wafer growth at atmospheric pressure and lower temperatures. So, this is the main stream approach for gate oxide ten nanometre, it is possible reproducible that is very important, because batch processing is done and all the you see that all the computer chips are made of S i where S i O 2 is is extensively used and in one wafer you can have this kind of of a wafer the wafer diameter can be 2 inch to say 8 inch.

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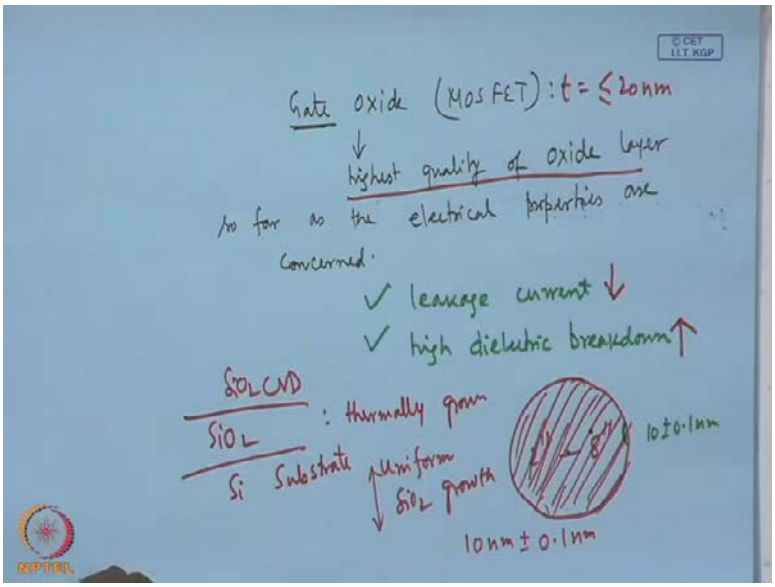

So, in an 8 inch diameter you must have uniform growth of S i O 2 uniform growth throughout the length and breadth throughout the surface and all the areas it must be a uniform growth nd this uniform growth is essential uniform. S i O 2 growth it is essential and you see that in this uniform S i O 2 growth what you can do? That 10 nanometre is possible plus minus 0.1 nanometre.

That is very important plus minus 1 nanometre across the wafer that means here say it is 10 nanometre, here it is 10 nanometre or at this side it can be 10 plus minus 0.1 nanometre. So, very, very controllable growth is possible so that is the mainstream approach later on we shall see that this SiO 2can be grown by other methods also as well like a CVD and different kinds of precursors we can use that we can and consider in the later stages.

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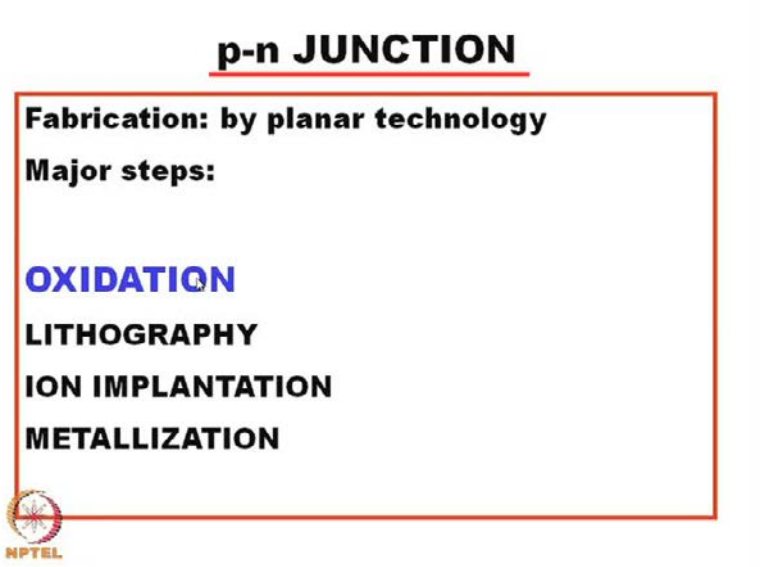

Then what happen? That here we have considered that we have some oxidation and this oxidation and have different type of approaches because in a MOSFET there are different kinds of layers also.

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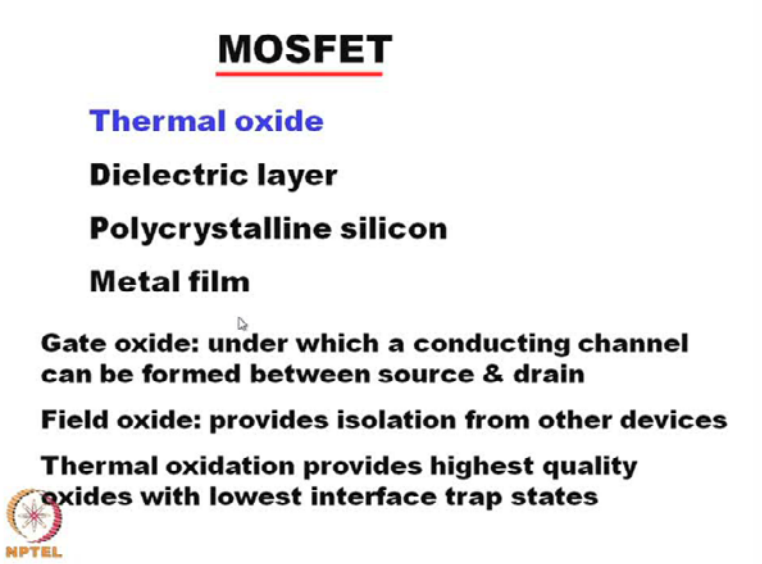

Let us discuss something about this dielectric layer, which is essential for device fabrication as well.

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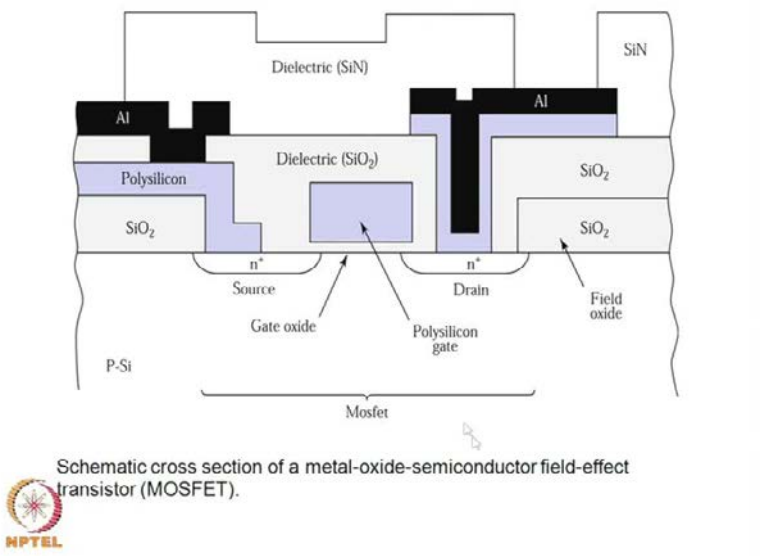

Schematic cross section of a metal-oxide-semiconductor field-effect transistor (MOSFET).

Because in a in a dielectric layer, what happens that silicon nitrite is obviously generally used, and this silicon nitrides can be have different types of growth and also we can have thick oxide layer like S i O 2.

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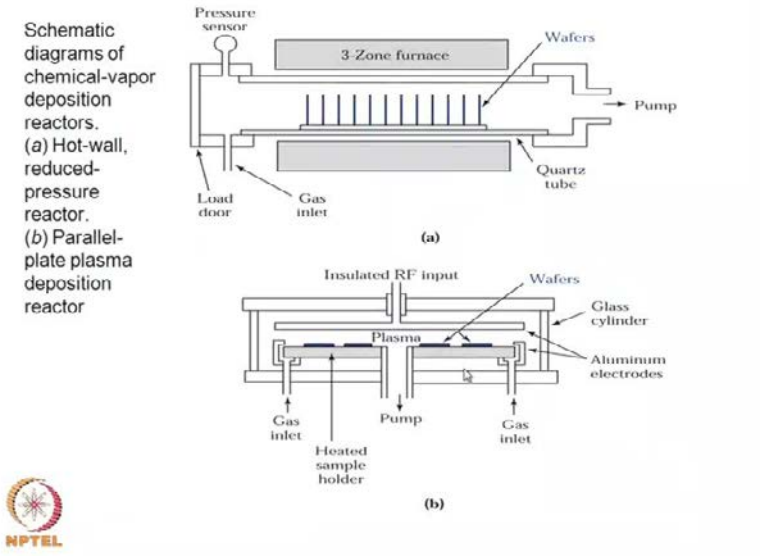

Say you can use that hot wall reduced pressure reactor because this is a CVD approach and parallel plate plasma deposition reactor also. We have, so that the lower portion we see that there are aluminium electrodes and in between the aluminium electrodes the wafers are placed where there is the gas inlet pumping system etcetera. This blue are the

wafers where you can put several wafers at a same time and r f source is there because in r f source what happens there is a chance to form the plasma because the the because in this case that will be very very uniform growth of S i O 2 and there can be say glass cylinders etcetera. Inside that there are the wafer circuit and the plasma is formed by the insulated r f input and pumping is required because you have to reduce the pressure inside the air atmosphere. You have to take out and if you need say plasma of say argon or anything and then you have or hydrogen then we have to use that kind of a gas inlet for making this plasma.

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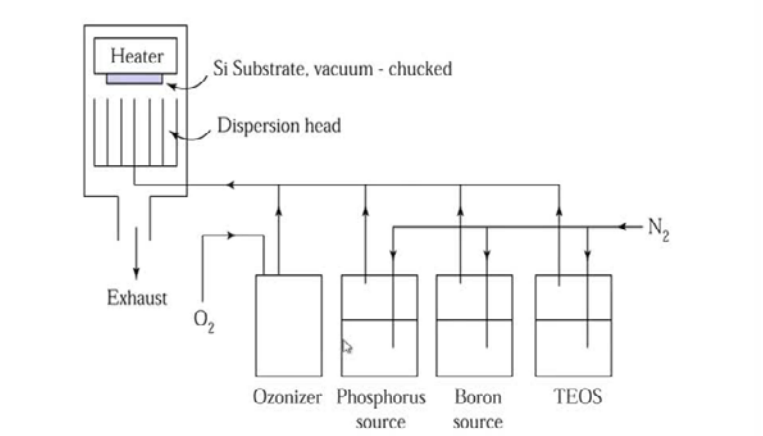

Experimental apparatus for the O_3-TEOS chemical-vapor deposition (CVD) system.

Now, one experimental apparatus for the O 3 TEOS chemical vapour deposition system, in this TEOS chemical vapour deposition, we see that there are ozonizer, then there can be phosphorous or boron source because you can dope S i O 2 you can dope S i O 2 and TEOS is one of the precursors. Here you see that the nitrogen vapour is used for making the transporting the gases. So, phosphorus source it can be say phosphine, boron source it is it can be boron hydride and then ozonizers is also there where the input is oxygen.

So, what are the things that we we sent one is that you see that oxygen, number two is TEOS and if you need p type or n type doping, then what to use as the boron or phosphorous respectively. Because boron gives you the p type doping and phosphorous the n type doping and there will be sufficient accumulation of the vapour pressure and that vapour pressure will be transported by the nitrogen as the carrier gas to the reactor

side here. There will be some silicon substrate vacuum chucked is used heater is also used to heat and dispersion head for the uniform dispersion of all the chemicals.

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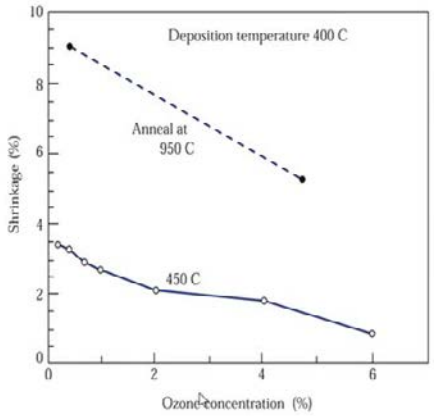

Dependence of the shrinkage of the O_3-TEOS CVD film on ozone concentration using annealing. (Courtesy of SAMCO Company, Japan.)

There will be growth of the TEOS made TEOS used CVD S i O 2. Then if you have some ozone concentration with shrinkage, you see that there is a ozone concentration with the shrinkage and dependence of the shrinkage of O 3 TEOS CVD film on ozone concentration using annealing. So, two annealing temperature are used; one annealed at 950 degree centigrade another is 450 degree centigrade and the deposition was took place at 400 degree centigrade.

The heater is there, so the deposition took place as 400 degree centigrade and at that temperature you see that there is a shrinkage when the annealing temperature is almost double. So, the shrinkage is more when the annealing temperature is more because from 450 degree centigrade to 950 degree centigrade. You see that the shrinkage is quite high from almost 3.8 to 8.6 or 8.8 at a particular ozone concentration. However, when the ozone concentration is reduced when the ozone concentration is reduced the shrinkage is also reduced.

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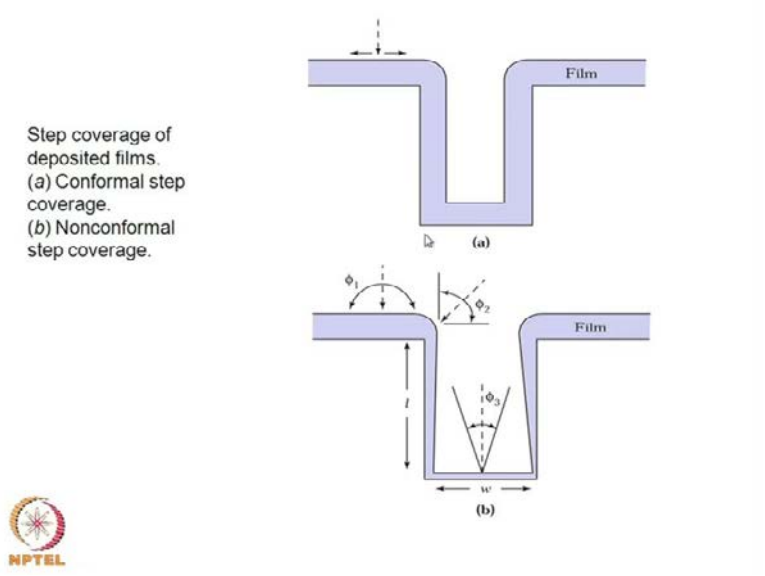

So, that is one important aspect of the film, and the if you consider the step coverage that you see that it is the conformal step coverage in conformal step coverage.

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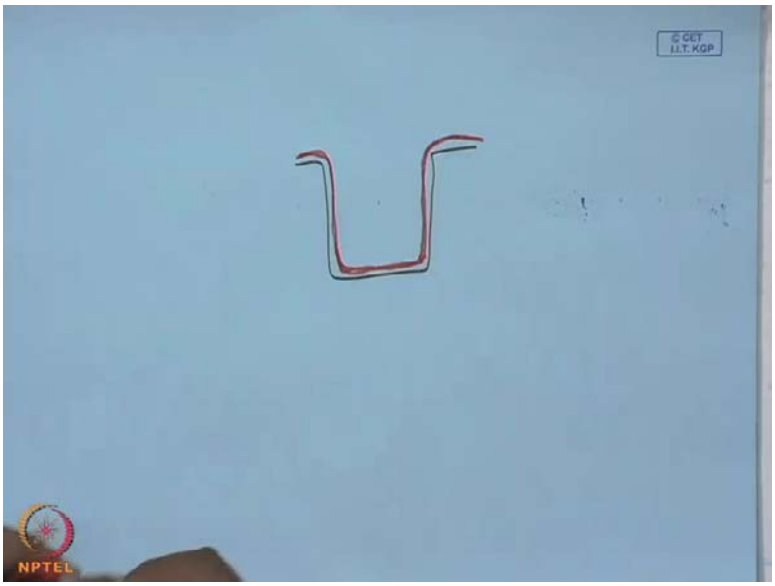

What happens that in a conformal type of coverage the all the regions, all the regions all the sides will be conformally deposited. The material will deposit uniformly on all the sides etcetera in the corners region everywhere. There will be uniform deposition, so that is known as the conformal here you see that in all the directions the thickness is same thickness of the deposited film is same.

But in this case you see that it is not conformal it is non conformal, in the sense that in some of the regions, the thickness is poor and in some of the region's the thickness is uniform. When they are making an angle phi 1, so it is uniform, but when they are making an angle phi 2, so there is some reduction in the thickness or in phi 3 that means the precursor molecules are coming at at an angle, let us say with phi 3 then it is still a reduced so depending on the angle of the deposition, so the thickness of the films will be different.

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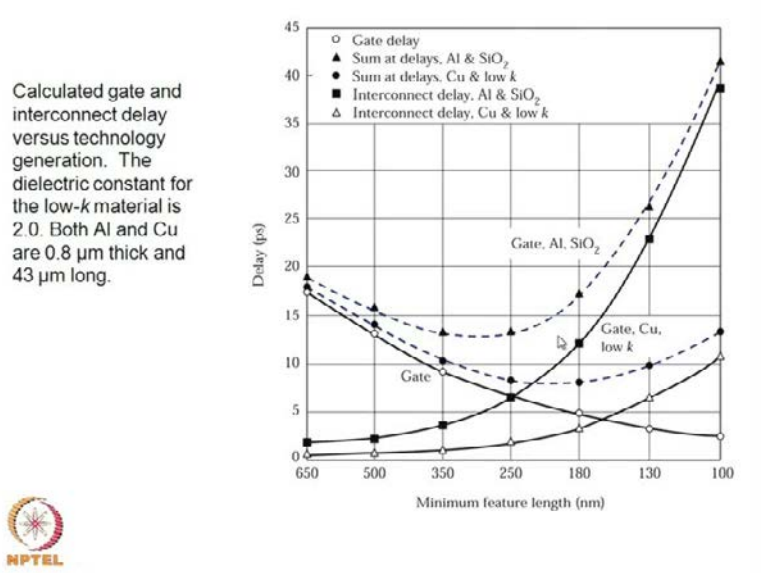

Now, it is basically the a calculated gate and interconnect delay versus technology generation and different kinds of technology have been used and the dielectric constant for low k material is 2, a low k material and both aluminium and copper are 0.8 micron thick and 43 micron long, both aluminium and copper. They are 0.8 micron thick and 43 micron long.

So, there are some you see that some at delays gate delays is this, this word is a gate delay, so gate delay is reducing as the minimum feature length is reduced. So, from 650 nanometre to 100 nanometre you see that there is a reduction of the feature size and at the same time the delay in pico second is also reduced, from say 17.5 to 2.5 at 100 nanometre. However, interconnect delay copper and a low k you see that this is the interconnect delay. Interconnect delay is basically very high, if you consider the

minimum feature length, it is gate with aluminium and S i O 2. S i S i O 2 aluminium is the metal gate.

Then interconnect delay, you see that interconnect delay is aluminium and S i O 2 this interconnect delay is also increasing. So, both the interconnect delay and the interconnect delay with copper, this is the copper and interconnect delay with a aluminium. This is this triangles are the copper and this rectangular are the aluminium. So, both are increasing aluminium increasing, the increase in aluminium is is very high, it steeps rather compared to the copper.

However, if you sum at the delay, so if you take the sum so these two are the summation of delays, the blue one. However, the gate delay is low, so you see that the interconnect delay and gate delay versus the technology generation. So, one has to make some optimization, so that the delay will be small because with the gate delay it is reducing, but the interconnect delay is increasing and the sum is obviously the increasing.

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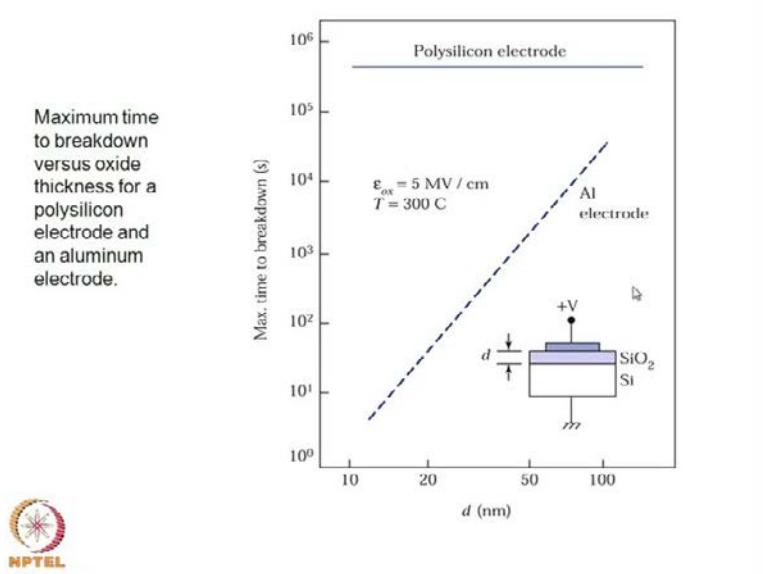

Here you see that it is basically the when there is a polysilicon electrode maximum time to breakdown versus, maximum time to breakdown versus thickness for a polysilicon electrode, that polysilicon electrode is as mentioned earlier that it is basically the polycrystalline silicon and with aluminium electrode you see that as the d increases, d increases obviously the thickness basically it is a thickness oxide thickness is d and

maximum time to breakdown it is second, so maximum time to breakdown also increases but it must be thick enough.

Even if you take a say 20 nanometre or say 50 nanometre gate, 50 nanometre or 20 nanometre aluminium electrode, you see that maximum time to breakdown is is very small, 10 second compared to 100 nanometre where it is 10 to the power 4 second. Here the oxide thickness dielectric constant dielectric is breakdown voltage is 5 mega volt per centimetre, obviously very high and temperature is 300 degree centigrade a very high temperature also.

Now, if you consider the polysilicon electrode you see that this is the polysilicon electrode, here whatever be the thickness of the oxide layer whatever be the thickness of S i O 2, if you use this as a polysilicon this blue 1 is polysilicon, so then the breakdown is very high, it is above 10 to the power 5 second and but it is uniform throughout the thickness so it has no bearing on the value of the thickness of the oxide layer.

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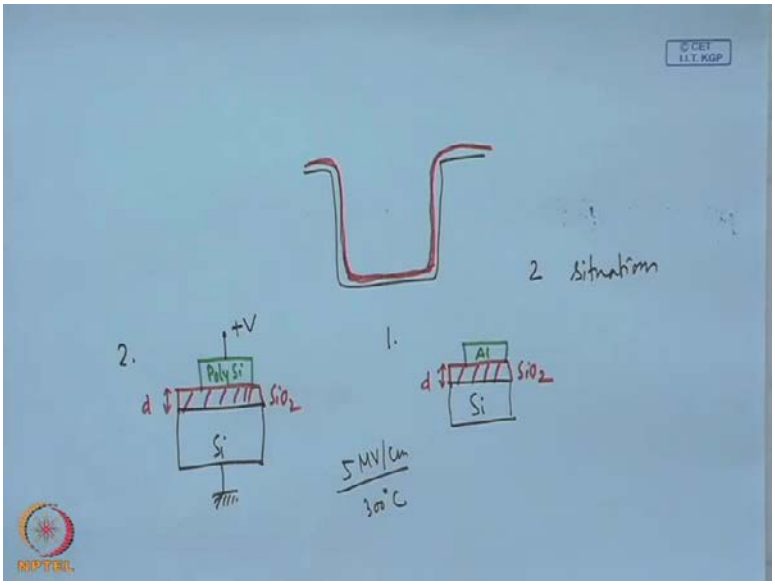

So, that means we can have two types of situation, two situations; one is this S i substrate on which we have S i O 2 and over which we have this is d thickness over which we have aluminium. This is aluminium, so this is one situation another situation is number two situation is you have silicon over which we haves i O 2 of the same thickness. The d S i O 2 the thickness is d, this thickness is d, this thickness is d and above which we have polysilicon. So, these two situations are there and if we if we put a voltage the

breakdown voltage will be here given and at 5 mega volt per centimetre has been, suppose you use at 300 degree centigrade.

So, under this situation, we are considering two cases; if you use this polysilicon gate you see if you use this polysilicon gate. So, if you use this polysilicon gate it is almost constant, this is almost constant and if you use this aluminium gate and with this aluminium gate you see that it is a function of the thickness. So, it is not a function of the thickness, however this is the function of the thickness, so polysilicon gate is always better than this silicon aluminium gate. So, people have been using this polysilicon gate for quite a long time and you can dope the polysilicon as well at n type or p type depending on your different kind of applications.

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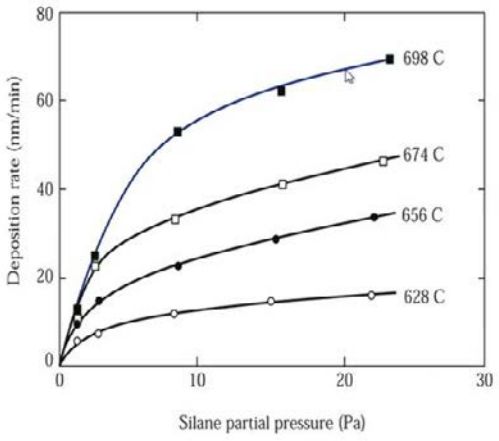

Effect of silane concentration on the polysilicon deposition rate.

Now, how the deposition rate of polysilicon depends on the silane partial pressure, the effect of silane concentration on the polysilicon deposition rate you see that for different temperatures are used 628 degree centigrade, 656 degree centigrade, 674 degree centigrade, 698degree centigrade, so four temperatures are used and with that temperature you see that the deposition rate is linear for lower silicon silane pressure soup to say 2 pascal 3 pascal partial pressure, it is almost linear.

Then above which it is going to be saturated, so if you use very high temperature say almost 700 degree centigrade. So, it is linear up to say 3 pascal, then above there is an increase, but it is going to be slowly it is the deposition rate is limited by the higher

silicon partial pressure. So, if you put silane with very high partial pressure so the deposition rate will be smaller.

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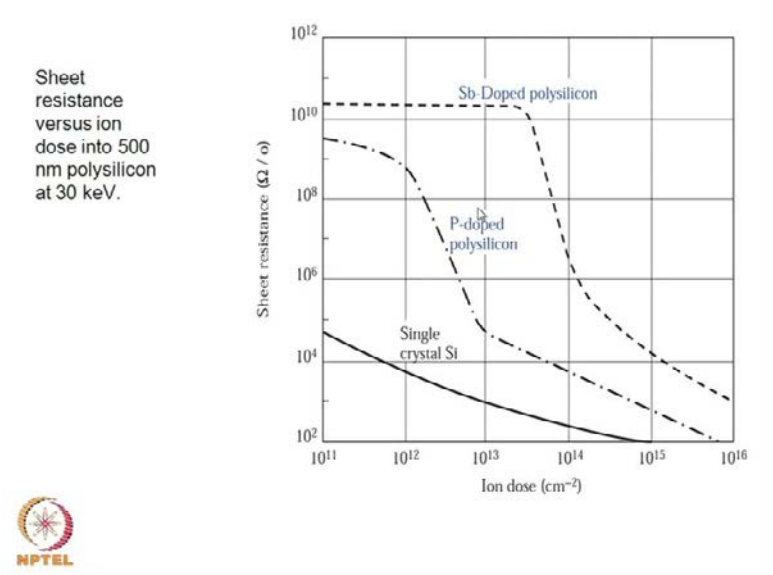

If you consider the sheet resistance versus the ion dose into 500 nanometre poly silicon at 330 kilo electron volt 30 k e V, you see that for single crystal the sheet resistance is very low. But this sheet resistance increases when you dope phosphorous in poly silicon or if you dope antimony in poly silicon. It is it is basically up to say 10 to the power 5 into 10 to the power 13 ion ion dose. It is almost the sheet resistance is almost constant independent of the ion dose, then it reduces. The sheet resistance reduces. Similarly, for phosphorous doped polysilicon it is basically a reducing and further reduction after 10 to the power 13 to 10 to the power 16 ion dose per centimetre square.

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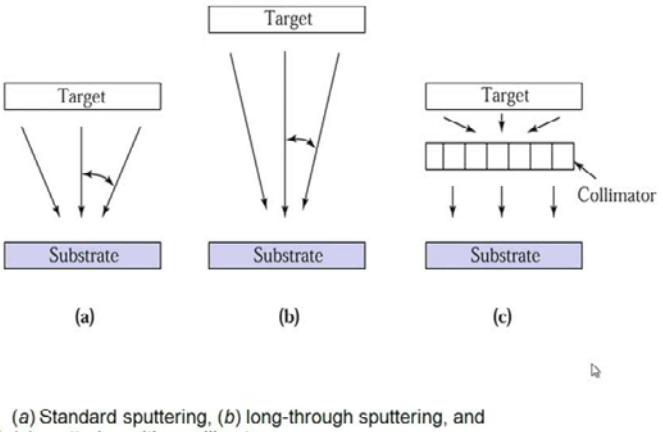

(*a*) Standard sputtering, (*b*) long-through sputtering, and (*c*) sputtering with a collimator.

Then if you have some say sputtering target here you can have substrate and the target, so depending on the target position you can have different kinds of growth of the deposited film this is the standard sputtering this is standard sputtering, what we use in our daily laboratories. This is basically the target when the long through sputtering is used and it is sputtering with a collimator. So, in collimator is basically you see that the angles are reduced because of the collimator.

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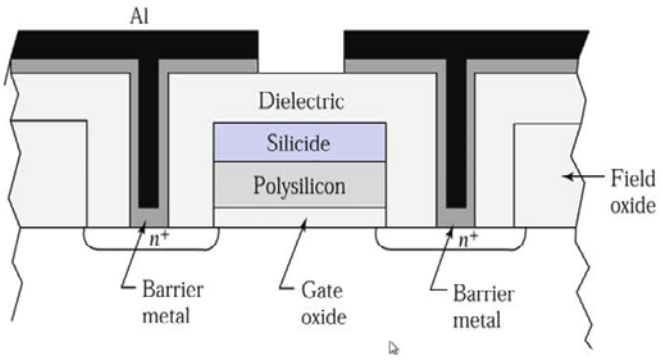

Cross-sectional view of a MOSFET with a barrier metal between the aluminum and silicon and a composite gate electrode of silicide and polysilicon.

Now, with this one important thing is that this if you see the cross sectional view of a MOSFET with a barrier metal between aluminium and silicon and composite gate electrode of silicide and polysilicon, the details of which we shall discuss that in this case the aluminium spiking will not be there because of this barrier meta land also. We have used some silicides for making the dielectric breakdown very high. Now, let us consider the earlier diagram where we have used this oxidation.

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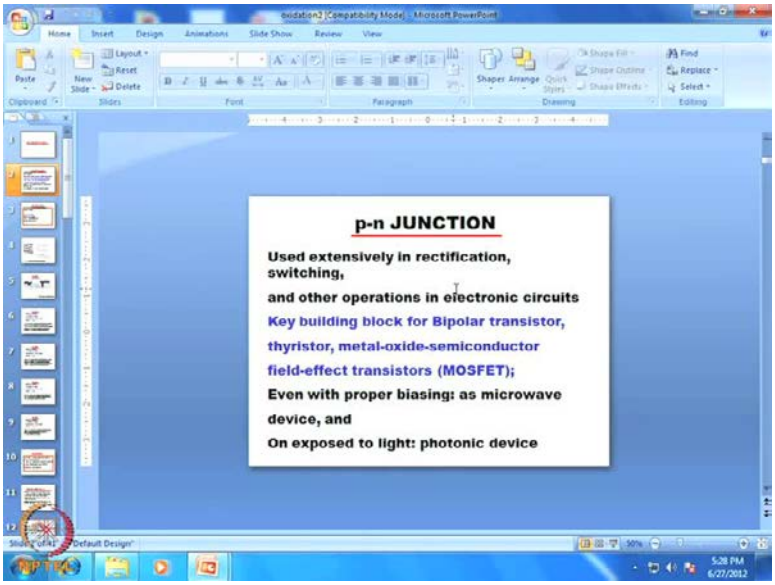

That in this process technology that where this we have used extensively in in making the p n junction, the it is very important.

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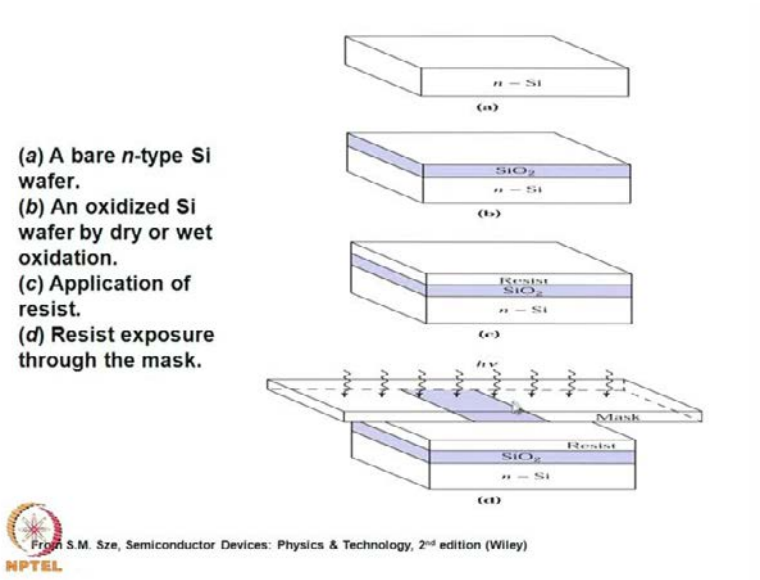

And in this case you see that what are the steps that we use here this is a bare n type silicon wafer we start with and then we oxidise silicon wafer by dry or wet oxidation. The details of which are are already discussed. And finally, we apply a resist mask for for some pattern transfer and resist exposure through the mask to obtain the different kind of pattern on the, so to obtain the different kind of pattern on the silicon dioxide resist. Finally, the h nu that means the ultraviolet irradiation is done with this ultraviolet irradiation. Generally there can be say positive photo resist or negative photo resist depending on the positive or negative different kind of of developer solution is used to etch out. Finally, the device is obtained.

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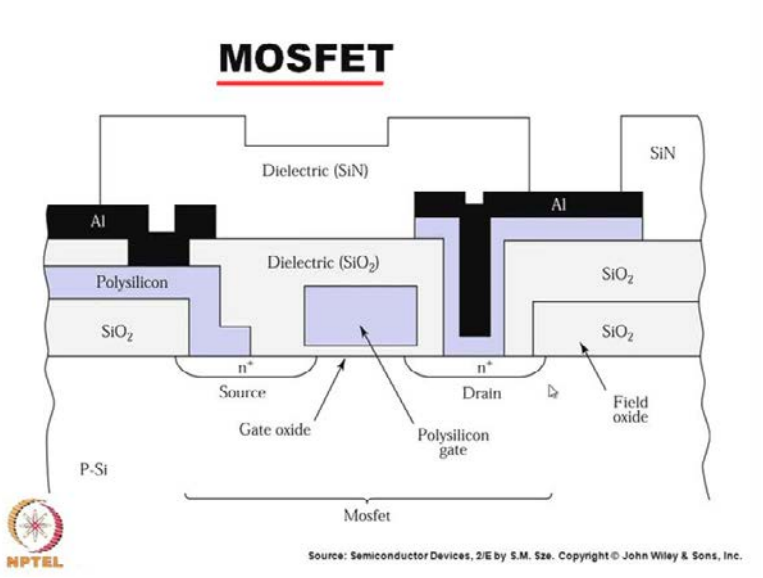

So, here you see that when is when there when we use a gate oxide or a field oxide for the isolation or gate oxide under which they a channel is made from the source to the drain apart. From this we can have say poly silicon, which is deposited on S i O 2 and on poly silicon we we can use aluminium for metallization here. Also you see that this is this is the source contact, this is the source contact, so directly we do not deposit aluminium on source or on on the source or we directly we do not deposit aluminium on the drain rather since it is a S i S i O 2 MOS.

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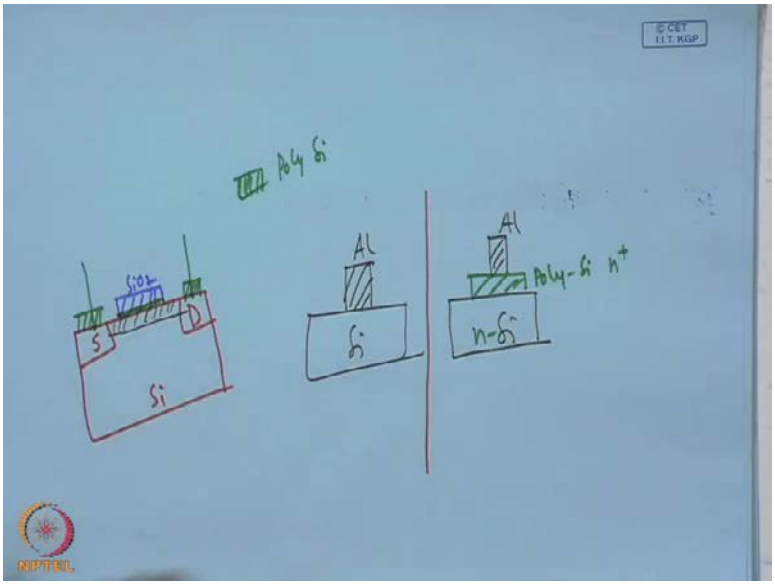

So, always we prefer that always we prefer that on silicon direct deposition of aluminium is also possible, but better if we use a silicon and then some poly silicon and finally say aluminium. So, as discussed earlier that this is this two types of possibilities are there; one is the direct deposition of aluminium on silicon or one is the deposition of the aluminium on silicon through poly silicon and it can be doped. Suppose, if it is n type silicon, so you can dope poly silicon n plus type. So, that it it is almost a monolithic type of resistance path is there, very small resistance.

The will be very, very small and it is basically a metal path type of concept can be created here, because of the heavy doping of the poly silicon on n type of silicon before making the aluminium contact. So, here you see that we have used that poly silicon as a layer between the metal and the source and drain. So, this is the source contact this is the drain contact. So, if you consider that a silicon MOS, so this is S i so you have to make the source and the drain and this source and the drain are connected by say poly silicon.

So, this is poly silicon, this is poly silicon and here you use, here you use the gate oxide S i O 2, so that a channel will be formed between source and drain below this S i O 2 gate. So, this is this general structure of a silicon MOS device where source and drain are used at the same time and S i O 2 is the gate. Obviously here also we can use a poly silicon gate above S i O 2, so before making the S i O 2 here we can use another poly silicon gate, this green patches are the poly silicon gate, poly silicon.

But consider that at the top layer we have used the dielectric S i N and S i N this silicon nitride dielectrics as discussed earlier that this is for the passivation of the surface. That is the protective coating that is the protective coating and you see that in this protective coating. We have silicon nitride because it protects from the moisture is protect from the dust and also is protect from the scratches such kind of dielectric layers have huge implications. In case of or applications rather in case of the solar cell devices not only in MOSFET in solar cell, you see that in solar cell what happens?

The panels are formed and the panels are kept at the roof tops or at the top of the trees etcetera in the forest areas or in different kinds of buildings at different places. So, there is a chance that you can have moisture or dust particle or scratch over that, so that will reduce the device like, so dielectric deposition are made at the top of the surface. So, in

essence 4 type of layers we generally use; one is the oxide layer, which is basically the gate oxide or the field oxide.

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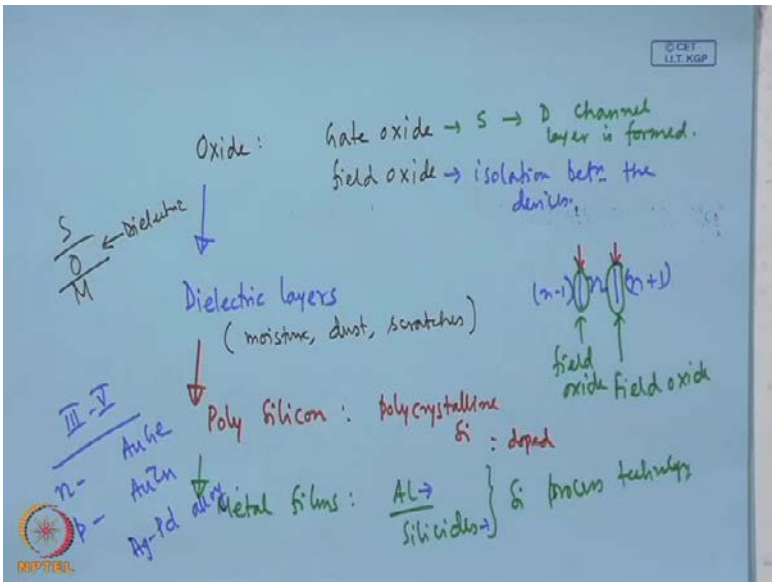

Let us summarize in this sense in this way that we can have oxide layer which can be gate oxide or field oxide. Remember that gate oxide is basically that thing below which source to drain channel layer is formed channel layer is formed. So, this is very crucial in device operation another thing is the field oxide. It is basically the isolation between the devices from one device to one another device.

Say, you you can have n number of device here it is N, this is N plus 1, this is N minus 1, so you can make this isolation here and this isolation here. So, between these two layers of the devices, you use the field oxide or here you use the field oxide. So, oxide deposition has very important and today we have just discussed about the thermal oxidation in a, at at at length and the different kinds of model the growth kinetics that we have obtained, that we have considered. Then up after oxide layer, we have seen that different kinds of dielectric layers are important dielectric layers are there and those dielectric layers are basically the layers, which protect from moisture from dust and scratches also.

These dielectric layers have is used for isolation as well as the dielectric layers are used for making the gate dielectrics like say MOS devices metal oxide semiconductor here also. This is basically nothing but a dielectric, so in later stages we we shall find that

different kinds of dielectrics are used say titanium oxide zirconium oxide tantalum oxide hafnium oxide different types of oxides are used those are basically dielectrics of very high value and they have specific application in high k areas. In the next class, we shall see that both type of dielectrics be it high k or low k is required for device applications.

So, dielectric layers cab be grown number three is the poly silicon. This is nothing but the polycrystalline silicon layer. It can be doped and we have seen that the breakdown on poly silicon basically does not depend on the thickness of the poly silicon. The breakdown is very high, at very high voltage or if the breakdown time. In terms of seconds is 10 to the power 6 10 to the power 7 second. We have seen that this poly silicon or the polycrystalline silicon, particularly you can doped for making poly silicon gate for making poly silicon source and drain between you put poly silicon between the metal and the silicon.

Your contact will be better with very low contact resistance and the last one is the metal films. Generally two types of metal concept we used; one is the aluminium or it can be say silicides. These are very much important in case of silicon process technology, but we shall see that in case of other type of compounds like say 3 5 semiconductors. If you consider the 3 5 semiconductors not silicon, then aluminium never used silicides, are also not used in this case. If it is n type, then we use gold, germanium or alloy or if it is p type, we use gold, zinc, alloys.

So, these are basically the alloys gold zinc, gold germanium, silver palladium, so different kinds of alloys are used for making the metal films. The metal can be used for interconnections, it can be used for making the ohmic contact, it can be used for metal semiconductor Schottky barrier or rectifying barrier. And we shall see that they they have some advantages disadvantages like aluminium spiking electro migration, those things we can we shall discuss in the next lectures.

Thank you.