

Processing of Semiconducting Materials
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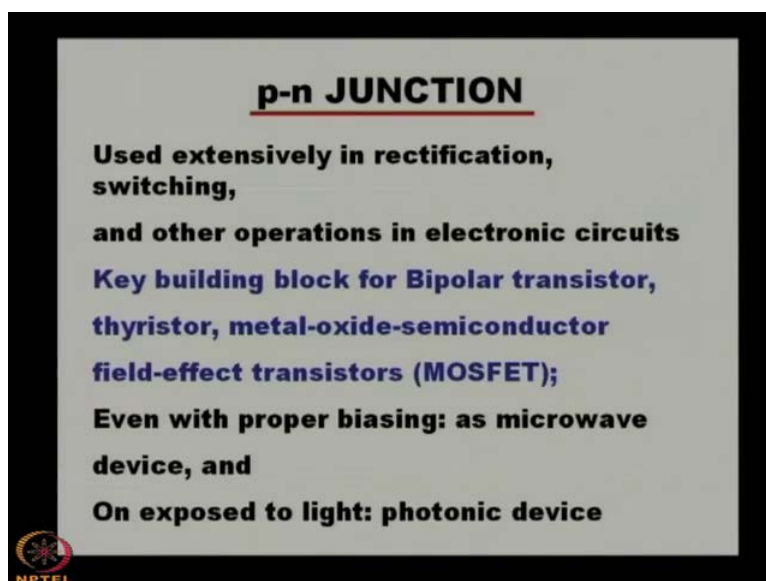
Lecture - 32
Oxidation - I

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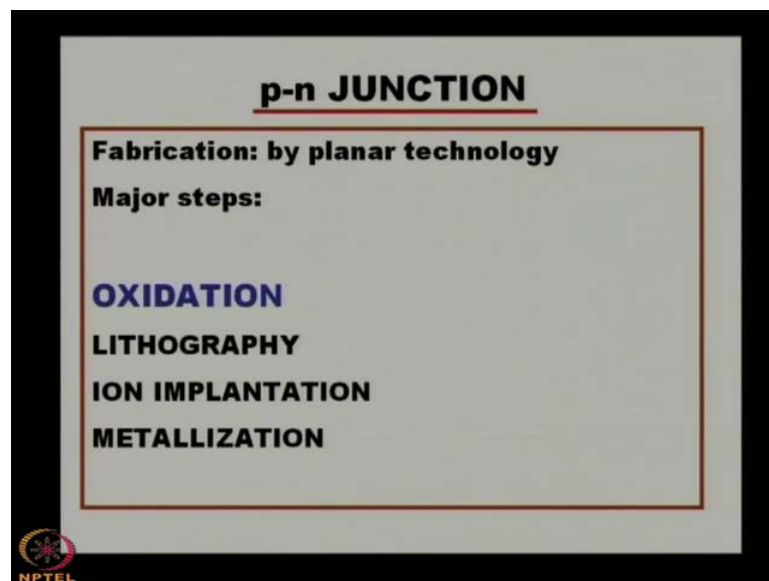
From today onwards, we shall start discussing the process technology.

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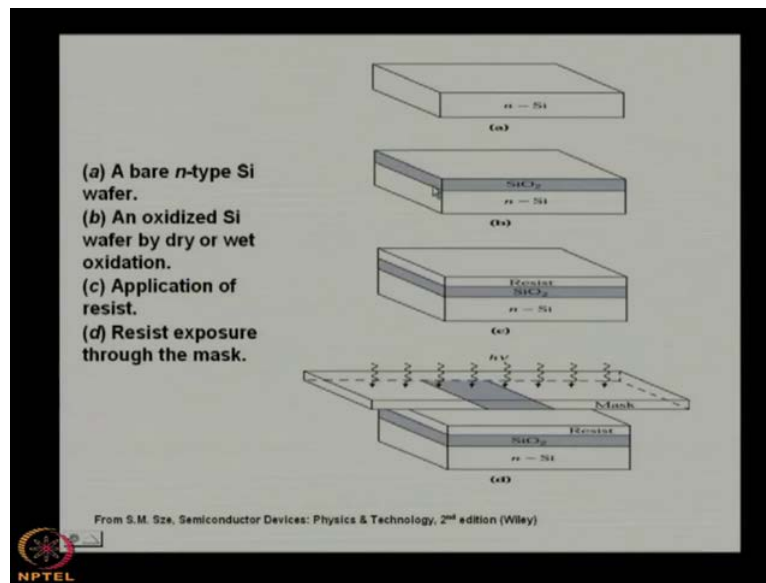
As you find that this is very important for any kind of material processing be it p n junction or any kind of device and it may be mentioned here that if you talk about the p n junction. You see that it is used extensively in rectification, switching and other operations in electronic circuits and this p n junction is the key building block for bipolar transistor, thyristor, metal oxide semiconductor field effect transistors that means MOSFET. Even with proper biasing, it can be used as microwave device and on exposed to light it can be used as a photonic device.

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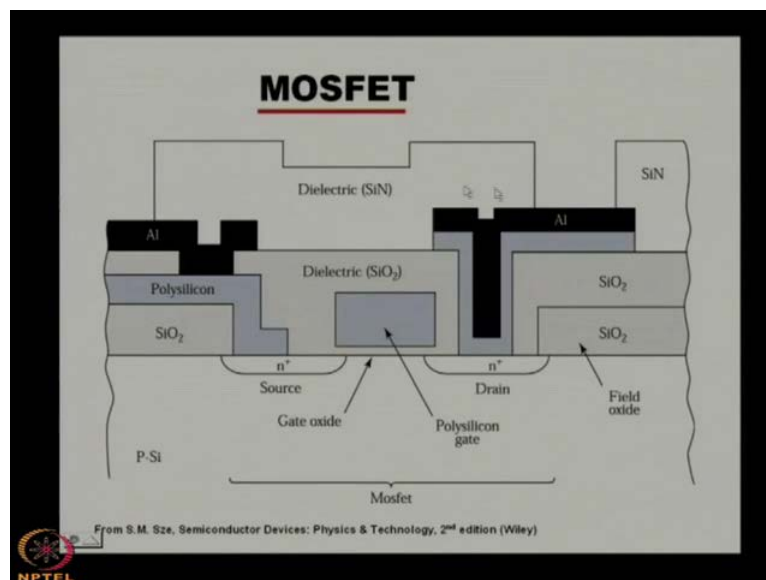
Now, for this process technology you know that if we talk about this p n junction, one important aspect of this p n junction is the oxidation. As you find that there are many steps for the process technology, one is oxidation on which we shall concentrate today. Others are the lithography, ion implantation, metallization and in our earlier discussion we have talked about the ion implantation in details and today's p n junction is nothing but the fabrication by planar technology and this is the backbone of all IC technology.

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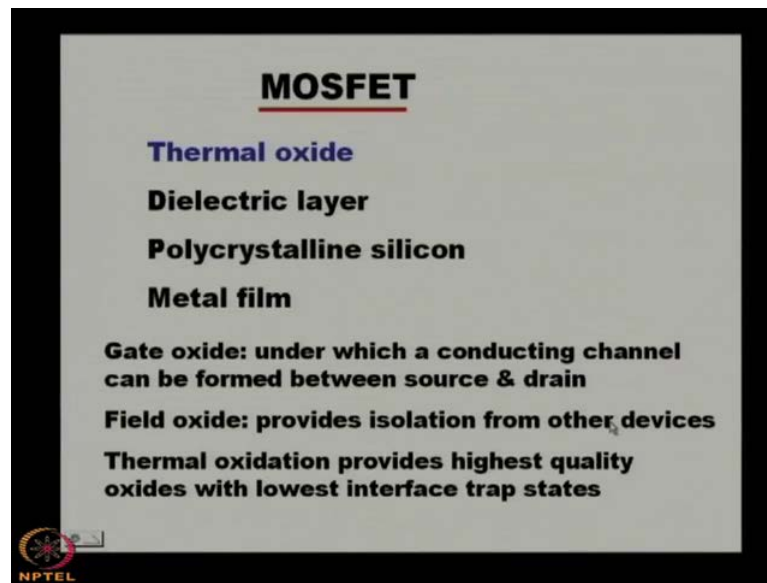
Then, if you find that for the formation of a p n junction, you see that if we start from an n type silicon wafer. First is to grow a layer of silicon dioxide on it, so this is the first step which defines the p n junction, so oxidation is very important step for this processing.

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If you take another example of the MOSFET, you will find that this in MOSFET there are many kinds of dielectric poly silicon and oxide films like this gate oxide poly silicon gate field oxide dielectric like silicon nitride then SiO_2 .

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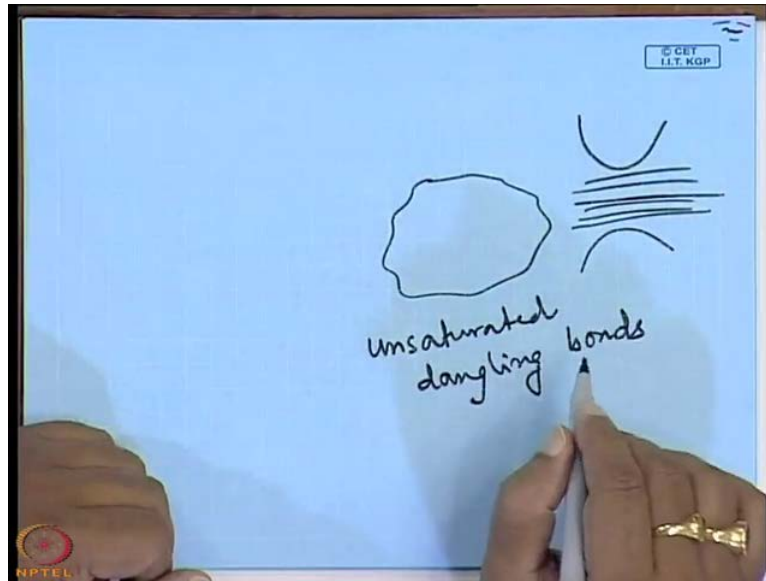


Now, there are many types of thin films which are used for the processing of MOSFET and important of those are the dielectrics like SiO_2 etcetera. Now, if we sub divide into a large number of a into if we sub divide the process technology related to MOSFET, we will find that there are four types of processing that need to be made. One is the thermal oxidation, another is the dielectric layer, third one is the polycrystalline silicon and fourth one is the metal film. You see that this is the metal film, like this is the aluminum, this black region this black region are the aluminum then poly silicon gate is the bluish region and one is the gate oxide another is the field oxide.

Now, if we start from the thermal oxide in MOSFET we will find that this is basically a conducting channel under which a conducting channel can be formed between source and drain. You see that this is the source and this is the drain and this dielectric SiO_2 under this the conducting channel is formed. Now, this gate oxide is nothing but the SiO_2 then field oxide is another oxide which provides isolation from other devices.

You see that in this case, this is the field oxide which isolates this MOSFET from the other devices that means there may be another MOSFET here which is grown by planar technology and this SiO_2 isolates that one. So, we find that this gate oxide field oxide which are important oxides for the fabrication of MOSFET. Thermal oxide oxidation provides highest quality oxides with lowest interface trap states, now what are interface trap states you see that if we talk about a silicon wafer.

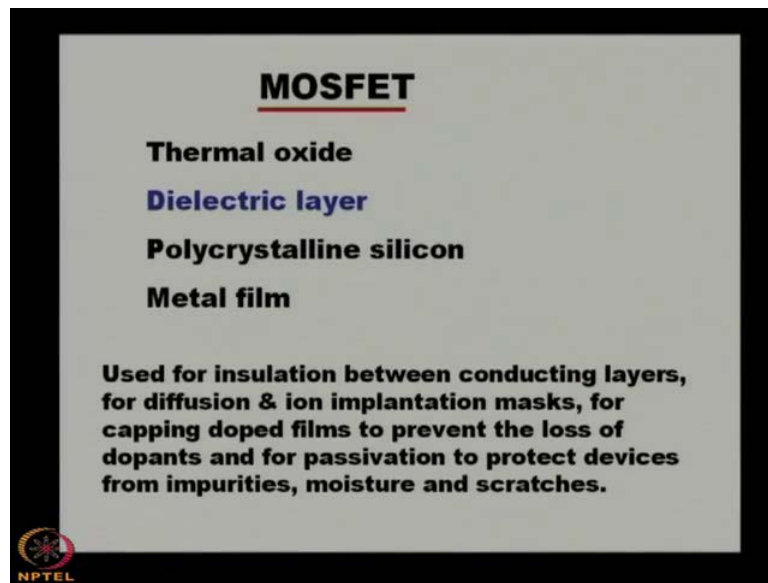
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Then, this is there is a discontinuity of the crystals because of the cutting or a slice of the crystals have been taken out as a wafer. When we start from the silicon wafer, there are unsaturated dangling bonds, there are unsaturated dangling bonds which are there at the surface because of the discontinuity of the crystalline state. Now, this discontinuity of the crystalline state is originated from the cutting of the crystal from the whole wafer from the whole crystalline whole bulk crystal. This is a bulk crystal and we take a piece of it we slice of it so there is a discontinuity and it is very easy from the quantum mechanical treatment to establish that this discontinuity in the crystalline states gives rise to the interface states.

That means between the conduction band and valence band we will find a large number of states which are known as the interface states. The origin of this interface state is the unsaturated covalent bonds due to the cutting of and a slice of the wafer from the original bulk crystal. Now, this thermal oxidation as we see that it provides highest quality oxides with lowest interface trap states. Now, we can assume that this oxidation is very important step so far as the silicon planar technology is concerned.

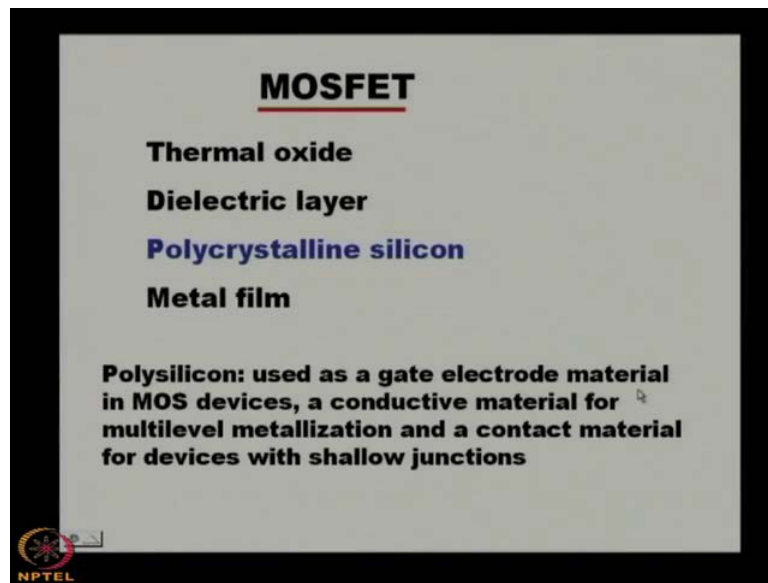
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Now, this is another important aspect of this technology is you see that this is the dielectric layer. We can use this for different types of application like the insulation between conducting layers for diffusion and ion implantation mask for capping doped films. This prevents the loss of dopants and for passivation to protect devices from impurities moisture and scratches. So, these are the application of the dielectric layer and you can find that this is the dielectric layer and this is silicon nitride which is used and other types of dielectrics are also used like SiO_2 . That is the transparent conducting oxide and then ZnO which is another transparent conducting oxide.

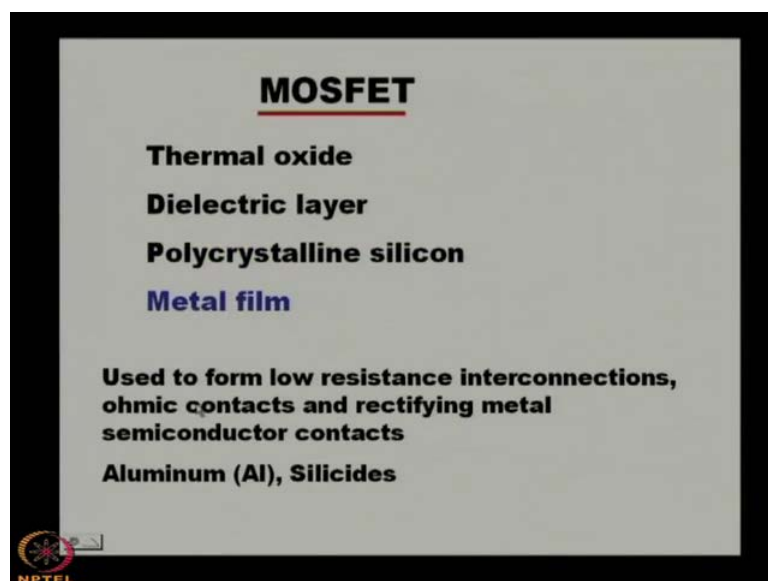
This type of conducting oxides is used particularly for the fabrication of the optoelectronic device like TiO_2 and SiO_2 , TiO_2 is a transparent oxide conducting oxide, and ZnO is another transparent oxide. Those are used for the fabrication of the optoelectronic device solar cells etcetera, the antireflection coating. So, that means you see that this dielectric layer is another important layer which can be a fabricated using this process technology third one is the polycrystalline silicon.

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You see that in polycrystalline silicon it is which is referred to as the poly silicon in general. This is used as a gate electrode material in MOS devices a conductive material for multilevel metallization and a contact material for devices with shallow junctions. So, this is another important process technology which we which we shall deal you see that this is the poly silicon gate. This is another poly silicon gate this is another poly silicon gate, so this is the contact layer and these are one of the important process technology which we shall deal with and the last one is the metal film.

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In metal film, it is used to form low resistance interconnections Ohmic contacts and rectifying metal semiconductor contacts and aluminum is widely used in silicon technology. There is lot of research on aluminum and also the silicide like your iron silicide or titanium silicide or aluminum silicide a large number of silicide is also used for the metal film.

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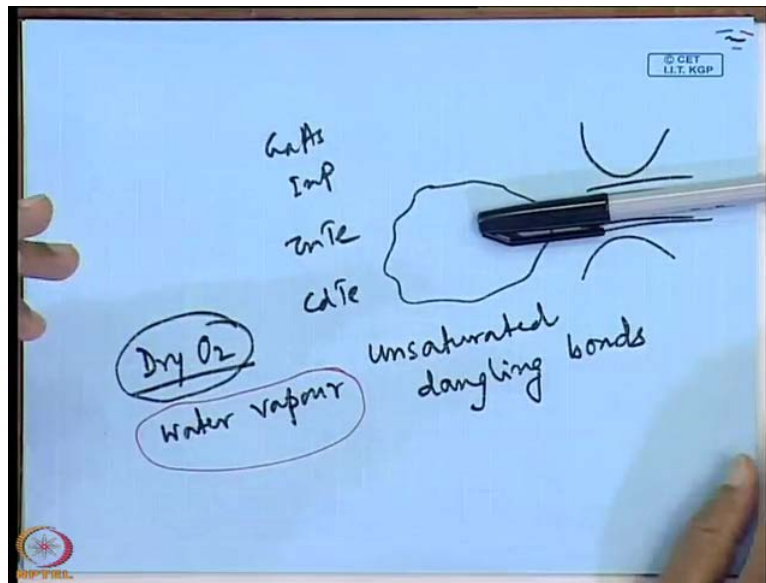


OXIDATION

High quality native oxide on silicon (Si)
SiO₂ (Silicon dioxide)
It acts as insulator, as a barrier to diffusion & ion implantation, in p-n junction it defines the junction area.
Oxidation: DRY and WET

So, from our discussion it is apparent that the oxidation is very important process technology and you see that the high quality native oxide on silicon. The term is very important here is the native oxide which is not, which is not available in except for the silicon in whole semiconductor family.

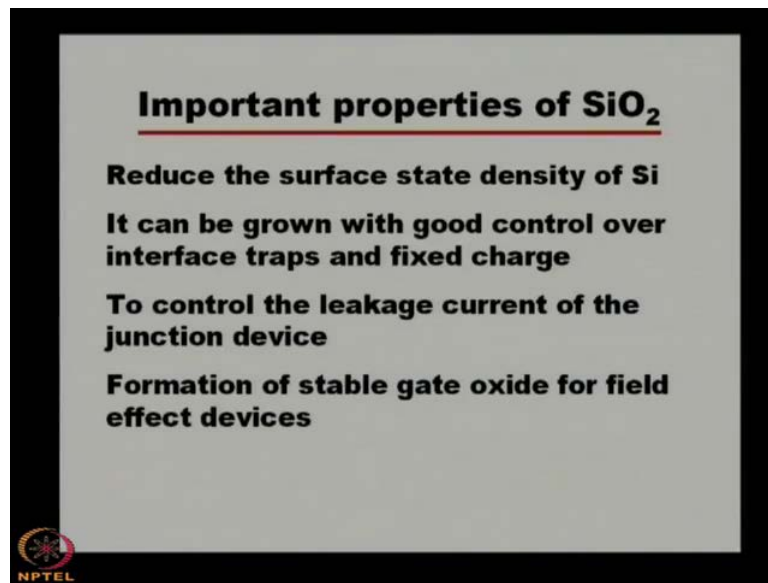
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Suppose, if we talk about the gallium arsenide or say indium phosphide or zinc telluride cadmium telluride a large number of materials consisting of the semiconductor family and you see that this high quality native oxides are not available other than silicon. It acts as insulator as a barrier to diffusion and ion implantation in p n junction it defines the junction area etcetera. These are the application of the oxidation and the oxidation can be dry and wet and depending on which kind of oxygen I shall use for the fabrication of the oxidation.

I use dry oxygen, I use dry oxygen, then it is known as the dry oxidation and if we use the high purity water vapor for the oxidation processing, then it is known as the wet oxidation it is water vapor. So, for dry oxidation, dry oxygen is used and for the wet oxidation water vapor is used obviously both the oxidizing species must be pure and you see that other important properties of Si O₂.

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It reduce the surface states density of silicon as we have mentioned earlier that basically the surface state density originating from the unsaturated covalent bonds or the dangling bonds because of the cut of the slice from the mother ingot. That we have discussed earlier that the whole crystal is obtained as the bulk crystal which is say 4 inch, 6 inch, 10 inch or even more than 20 inch diameter.

Length is some few feet and from where we cut the slice to use as a wafer or the substrate for the epitaxial growth or for the other kind of IC processing. The surface state density of silicon reduces, it can be grown with good control over interface traps and fixed charge to control the leakage current of the junction device. Formation of stable gate oxide for field effect devices, so these are the important properties of silicon dioxide.

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OXIDATION

Various methods for oxidation

- Thermal oxidation**
- Electrochemical anodization**
- Plasma reaction**

What happens for GaAs?

Non-stoichiometric films, poor electrical insulation & semiconductor surface protection

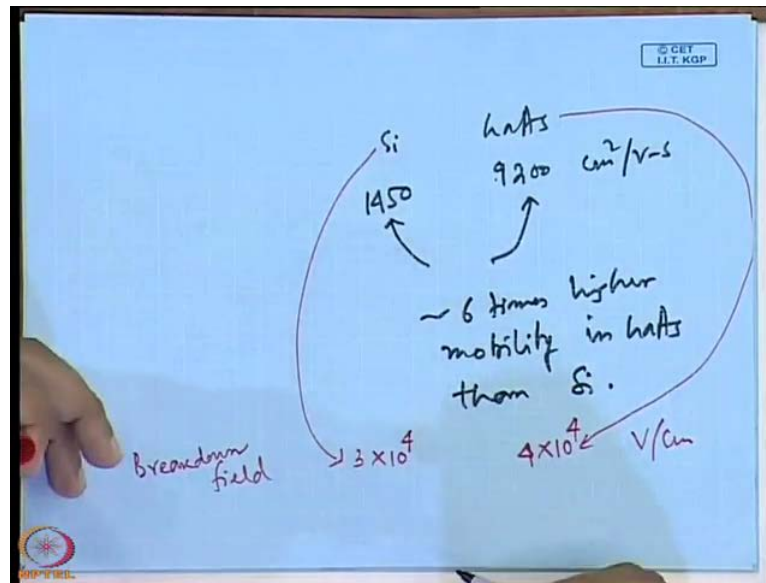


Now, there are many methods which we use for the oxidation one is the thermal oxidation, another is the electrochemical anodization, third one is the plasma reaction. Out of these, generally in semiconductor planar technology, we use the thermal oxidation the other two oxidations are not generally used. Now, what happens for gallium arsenide now because we are talking about the silicon and so far as the gallium arsenide is concerned you see that for gallium arsenide? If we try to oxidize gallium arsenide what happens it will be arsenic oxide it will be gallium oxide as well as the arsine.

So, it is obviously it will be non stoichiometric and so the films if we try to process oxidation out of gallium arsenide surface or on gallium arsenide surface. We will find that there will be non stoichiometric films and because of the non stoichiometric poor electrical insulation is there. So, the very spirit of the oxidation layer because it is used as the insulation and between the devices or between the gates or between the gate oxide and the metal.

So, it will be defeated and also the semiconductor surface protection will be very poor because of the non stoichiometrics. So, you see that though gallium is very important material, because you know that for a gallium arsenide what happens.

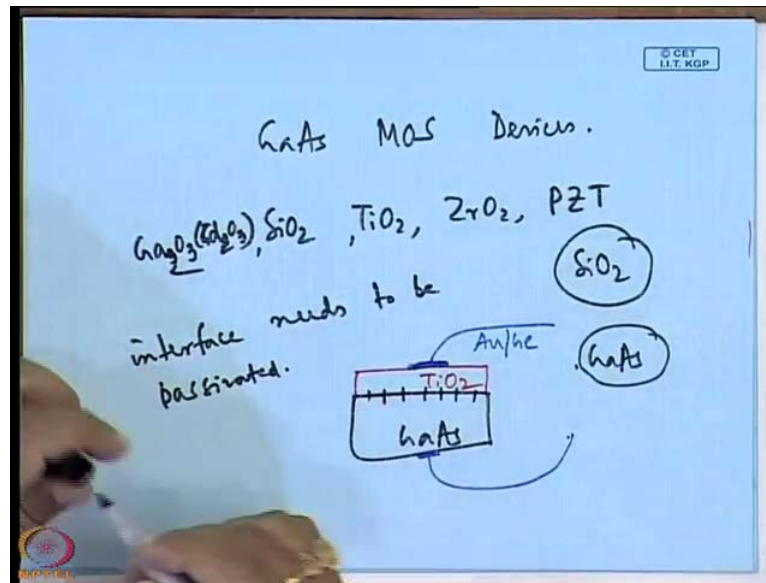
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The mobility for gallium arsenide is 9,200 centimeter square per volt second if we compare with silicon which is 1450. So, if we compare this 1450 with 9200, we will find that it is almost 6 times higher mobility in gallium arsenide than silicon. So, the mobility is very high and also the breakdown field which is in case of silicon is 3×10^4 in comparison to 4×10^4 volt per centimeter.

This is for silicon and this is for gallium arsenide, we see that the breakdown field is higher in case of gallium arsenide. So, these are the advantages of gallium arsenide over silicon and the mobility is 6 times higher the breakdown field is higher or so. The gallium arsenide device or MOS devices can be used for very faster response for power electronics etcetera. Unfortunately, because of the lack of proper oxidation on gallium arsenide like silicon because no native oxide is obtained in case of gallium arsenide. So, it is not used that means the oxidation of gallium arsenide is not used like the oxidation of silicon oxide.

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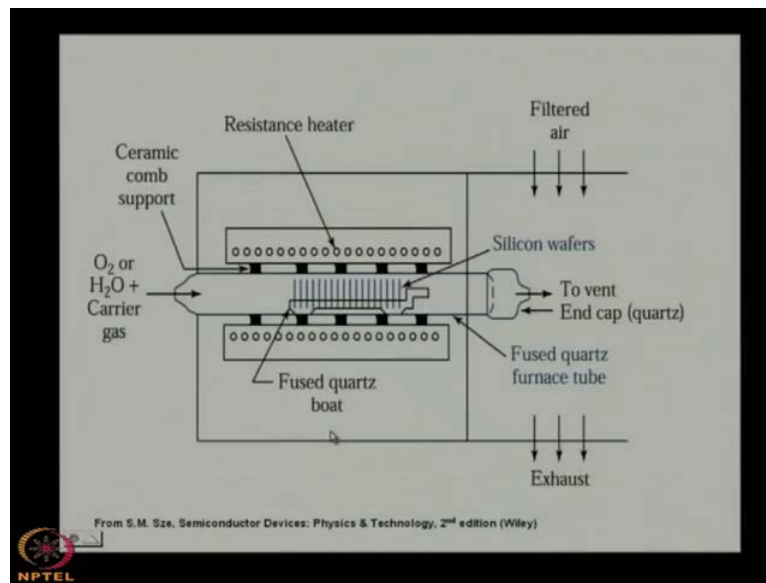


Now, the obvious reason is obviously the non stoichiometry and another important thing is that people have tried to form gallium arsenide MOS devices gallium arsenide MOS devices metal oxide semiconductor devices with the help of titanium oxide. Then, zirconium oxide then PZT also people used Si O 2 then gallium oxide gadolinium oxide Gd 2 O 3. So, this type of various oxides or the insulators were used for the fabrication of gallium arsenide MOS. The basic structure can be like this say we start with a gallium arsenide substrate suppose it is a p type substrate on which we form a oxide layer say Ti O 2 and then there is a metal gate say aluminum over it or gold germanium over it.

So, if we take the contact between the two, it acts as a parallel plate MOS capacitor and with the Ti O 2 as the dielectric between the two plates. One plate is this, another plate is this gallium arsenide and if the problem is here is that which we encounter is that this interface between the Ti O 2 and gallium arsenide needs to be passivated.

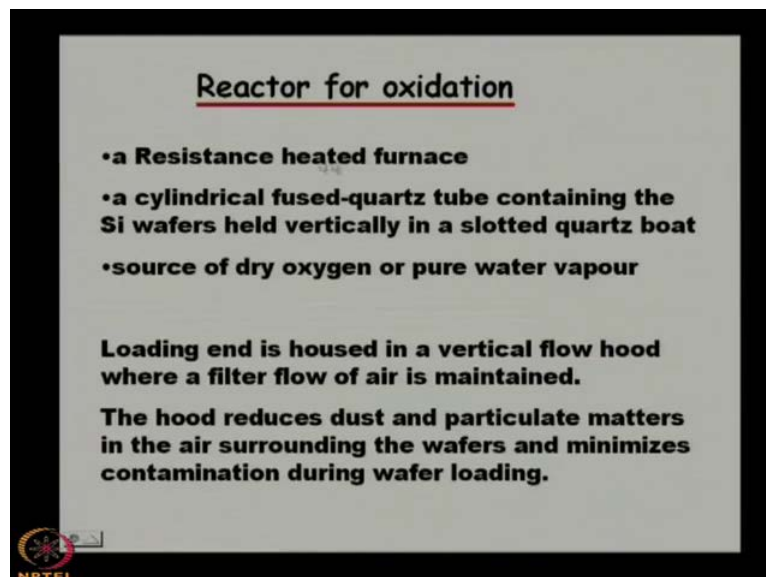
That means the interface states or the unwanted energy levels in the band gap that must be passivated using some chemicals and in this case generally people used hydrogen plasma or sulphur passivation or Si O 2 passivation. So, this type of passivation layer is required for the gallium arsenide MOS devices and so that is the advantage of silicon MOS over gallium arsenide. In silicon devices, the silicon oxide is the native oxide for gallium arsenide such kind of native oxide is not available, so for gallium arsenide even if it has many kinds of advantages over silicon because of the non stoichiometric films, it is not used now.

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For the oxidation process, we need a reactor and in this view graph you see that this is the oxidation reactor and which consist of these are the parts of the reactor. It consist of a resistance heated furnace this is the resistance heated furnace and this furnace can be resistance heated it can be inductance heated it can be lamp heating like quartz lamp etcetera.

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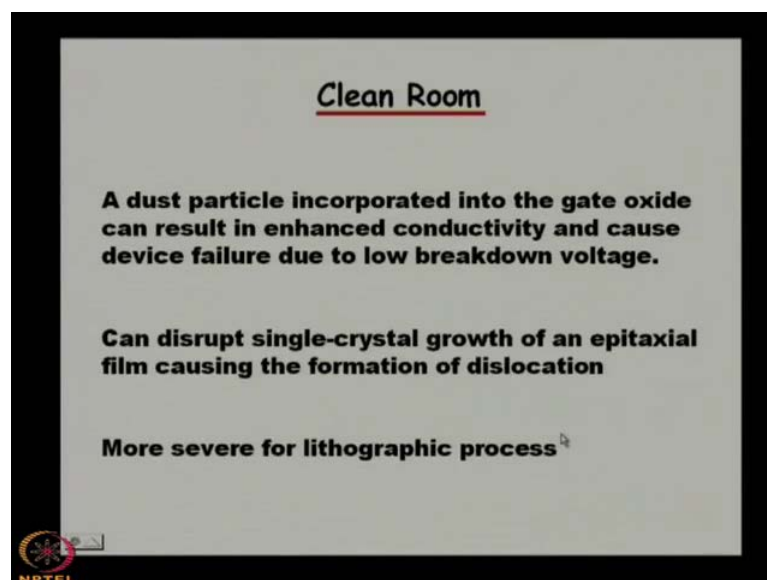


So, this is the figure, it is the resistance heated furnace, then a cylindrical fused quartz tube containing the silicon wafers held vertically in a slotted quartz boat. So, a cylindrical fused quartz, this is the cylindrical fused quartz and this is the slotted quartz boat on which the

silicon wafers are placed. You see there are large number of silicon wafers are placed on the quartz boat inside the quartz tube and this source of dry oxygen or pure water vapor is required in this case. This is the pure oxygen or pure water vapor which is carried by some carrier gas like the argon or nitrogen inside the reactor chamber.

So far, as the loading front is concerned that means the loading end is housed in a vertical flow hood where a filter flow of air is maintained. You see the direction of the air the filtered air is coming from the top and it is going to exhaust. So, there will be laminar flow at the loading end and that means through which the silicon wafers are put inside the quartz boat and the hood reduces dust and particulate matters in the air surrounding the wafers and minimizes contamination during wafer loading.

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Now, what is the implication of the reduction of dust and particulate matters and you would you see that so far as the possessing of the semiconductor materials is concerned it is always done in a clean room. Not only that, there will be a hood type of thing which we have described earlier in connection with the oxidation chamber the whole process unit must be housed in a clean room. This description of the clean room which I can show you is that there can be different type of clean room.

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How to define a Clean Room


Two systems: ENGLISH, METRIC

English System: Maximum allowable number of particles $0.5\ \mu\text{m}$ and larger per cubic foot.

Class 100: dust count of 100 particles/ft³ with particles diameter of $0.5\ \mu\text{m}$ and larger.

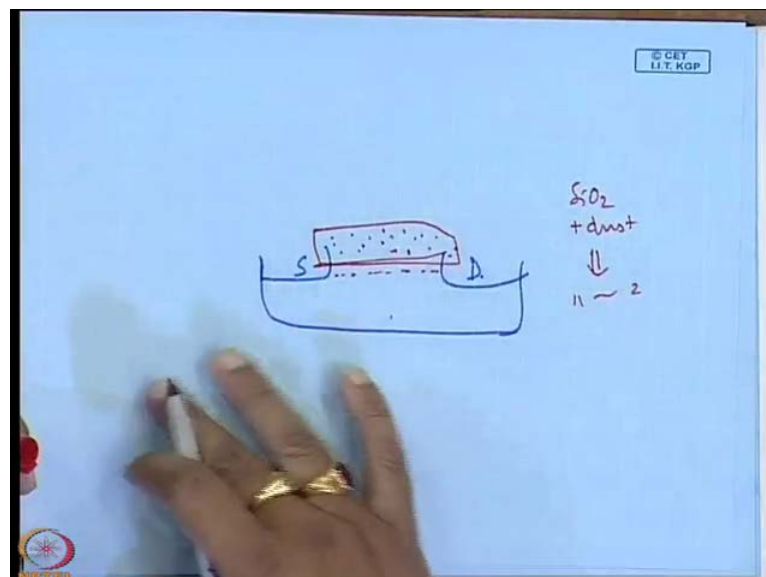
Metric System: Logarithm (base 10) of the maximum allowable number of particles $0.5\ \mu\text{m}$ and larger per cubic meter.

Class M 3.5: $10^{3.5} \approx 3500$ particles/m³



It can be class 100, it can be class m 3.5, it can be class 10, it can be class 1000 and we shall discuss those thing. Practically, a dust particle incorporated into the gate oxide can result in enhanced conductivity and cause device failure due to low breakdown voltage suppose we want to make a MOS device.

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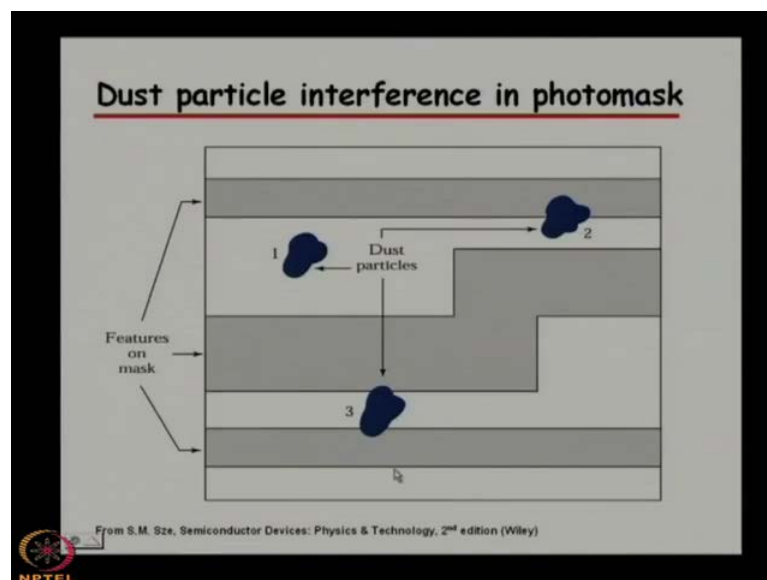


We have gate oxide, this is the substrate then this is the source then this is the drain and this is the gate this gate a channel must be formed just below the gate oxide and this gate oxide must be an insulating one. Now, if there is a particulate or some dust inside the oxide inside the

insulating material, then what will happen? Suppose SiO_2 we would like to grow it is insulator and almost 11 is the dielectric constant and if we add some dust with it may be that 11 will reduce to 2 or 3.

That means it will be conducting in nature and since it will be conducting in nature, so the breakdown will be held will be will occurred before the actual operation of the device. So, it can disrupt the single crystal growth of an epitaxial film causing the formation of dislocation and this problem of incorporation of dust or the particulate matter is very severe for lithographic process and for lithographic process.

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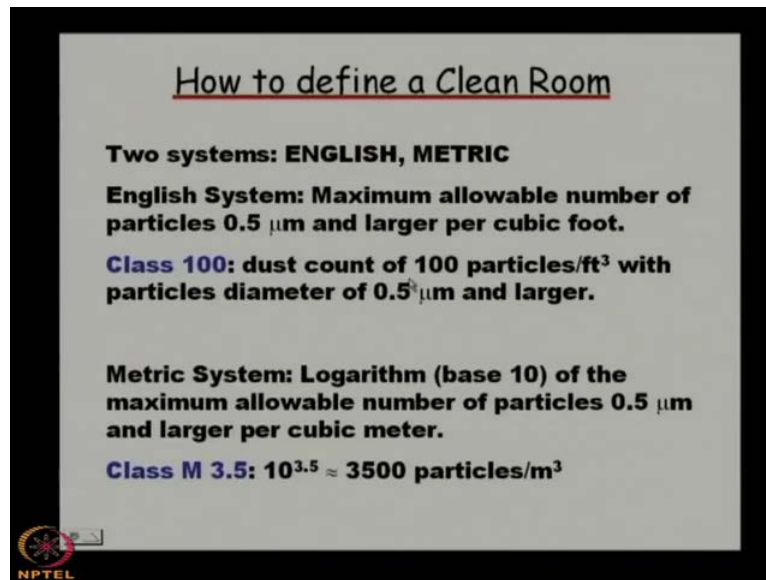


You see that suppose we want to transfer this pattern and if there is a dust particle so what will happen that it will be opaque to some photo mask. When it will be exposed, then there will be a connection between this connection between this feature and this feature. So, there will be a short circuit type of network between these two pattern, now between these two patterns since there will be a short circuit type of network. So, obviously there will be device failure or suppose you want to make the thickness of this open space is x and because of the dust particle x reduces to x by 4 or x by 3.

So, there will be device failure, so because of this type of problem associated with the incorporation of dust particle into the gate oxide or into the lithographic process. We need a clean room type of thing where there will be which will be free from any dust particle and particulate matter another important aspect of these incorporation is that. Suppose, we are

growing to we are growing an epitaxial field and there is a dust particle on the substrate. So, what will happen, there will be dislocation and so that epitaxial layer will not be used for the growth of the device or the fabrication of the device, now because of this difficulty associated with the incorporation of dust particle

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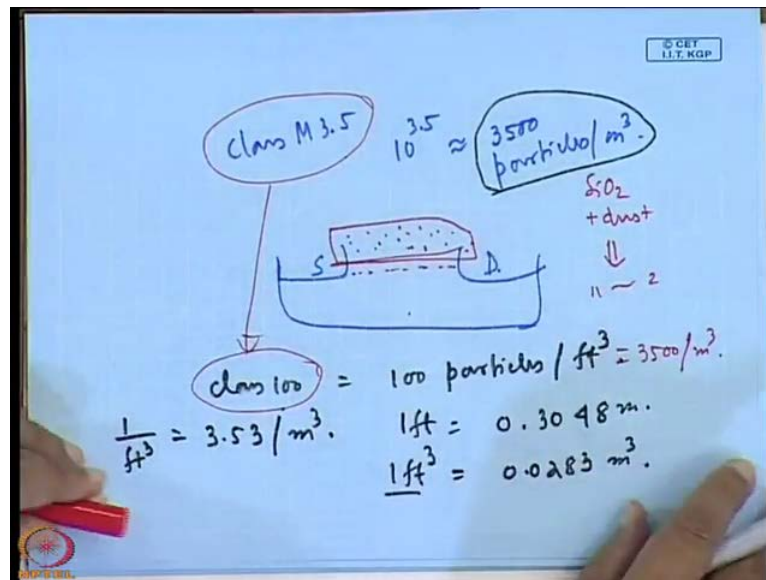
We need a clean room and so far as the clean room is concerned how to define a clean room there are two systems using which the clean room can be defined one is the matrix system another is the English system. In English system, generally class is used class 10 class 10,000 class 1,000 this type of method of nomenclature is given and for matrix systems class m 3.5 class m 6.5 class m 9. Those are used in English system maximum allowable number of particles of size 0.5 micron and larger per cubic.

That means if we take one cubic foot of the volume then within that volume of one cubic foot there should not be 100 particles of size 0.5 micron and larger when we talk about 0.5 micron or larger that means it is the diameter of the particle. It is the size of the particle means the diameter of the particle, so it must be very precise. Suppose, in this room first you calculate the number, first you calculate the volume of this room and then how many dust particles of that size means 0.5 micron and larger can be accommodated at the maximum within that limit.

Otherwise, we have to reduce the dust particles to make it a clean room and obviously these are not clean room and in class 100 clean room the dust count must be 100 particles per cubic

feet with that size means 0.5 micron and larger. Now, in metric system, it is taken as the logarithm base 10 of the maximum allowable number of particles of the same size. The size is constant 0.5 micron and larger in both the cases in class 100 that means in English system it is cubic feet is taken as the volume in metric system cubic meter is taken as the volume.

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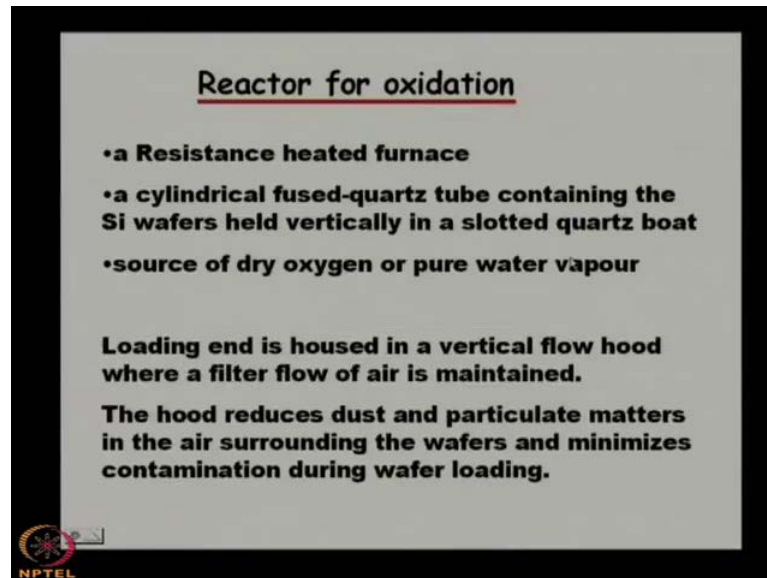
Suppose, we have the class m 3.5, so what is the value of class m 3.5 say class m 3.5 means ten to the power 3.5 and approximately it becomes 3,500 particles per cubic meter approximately the value is say 3 2 0 0 or such. Let us take as 3500 into 10 to the power 3.5, these particles per meter cube, now class 100 it is basically 100 particles per cubic feet. Now, we know that one foot is equals to 0.3048 meter, now if you take one foot cube then it becomes 0.0283 meter cube.

Then, if you take the reciprocal of 1 feet cube, then it will be 1 by 1 feet cube is equals to one by 0.0283 and it will give you 3.53 per meter cube. So, now if you compare with this class 10, class 100 and class m 3.5 what you find that in class m 3.5 you have 3500 particles per meter cube class 100, 100 particles per feet cube. If you convert this feet into meter you will find that it is nothing but 3500 particles per feet meter cube, so that means in English system class 100 is equivalence to class m 3.5 in metric system.

So, in this manner one can one can convert the relative number of dust particles per feet cube or meter cube in a clean room for semiconductor processing technology. Generally, class 100 class 1,000 clean room is absolutely required in some cases like say lithographic process even

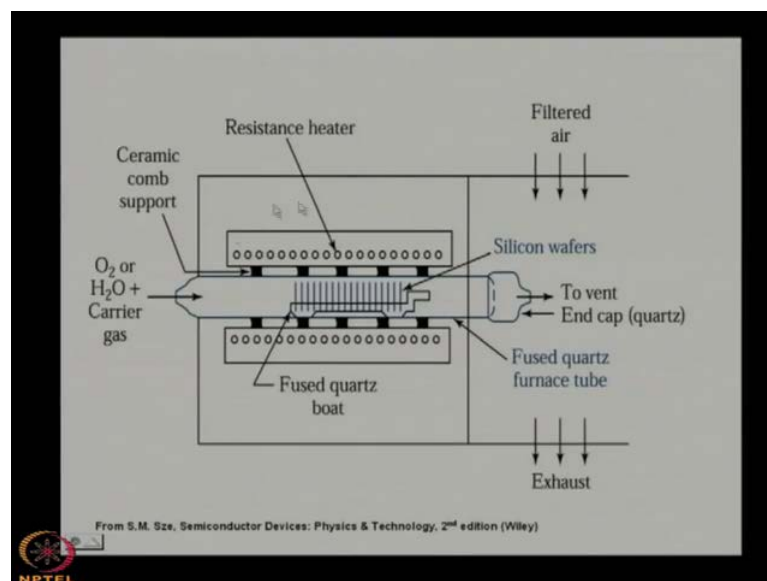
class 10 clean room is advisable. Otherwise, you will find that there will be network of connections or that can be other type of damages or pattern which is nothing but the opaque in a light system in a photo mask and that will be very detrimental to the device fabrication.

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Now, another important concept consideration of this oxidation chamber is that you see that whole thing is controlled by the microprocessor.

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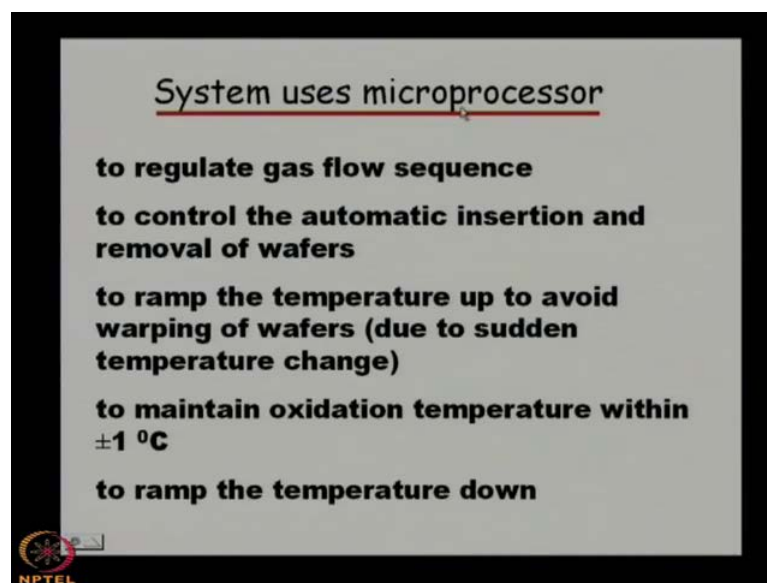


The whole thing means the first thing is that we have to load the silicon wafers inside the oxidation chamber another important thing is the enhancement of the temperature raising the

temperature from the room temperature to the oxidation temperature. Obviously, the temperature cannot be raised very arbitrarily and suddenly, then there will be warping of the damage of the silicon wafers due to sudden increase in the change sudden increase in the temperature. So, there will be a heat shock to the wafers, so obviously this temperature must be increased very linearly which is nothing but the ramping.

So, ramp heating must be associated with this, so one thing is the loading of the silicon wafers another thing is the increase of the temperature from the room temperature to the oxidation temperature linearly. That means by the method or ramping and then it must be stable for quite some time suppose during the process of oxidation the temperature of the oxidation furnace must be stable and what the temperature oxidation furnace is. The general temperature which is required for the oxidation of silicon is 900 to 1200 degree centigrade generally 900 to 1,200 degree centigrade temperature is required for the oxidation of silicon.

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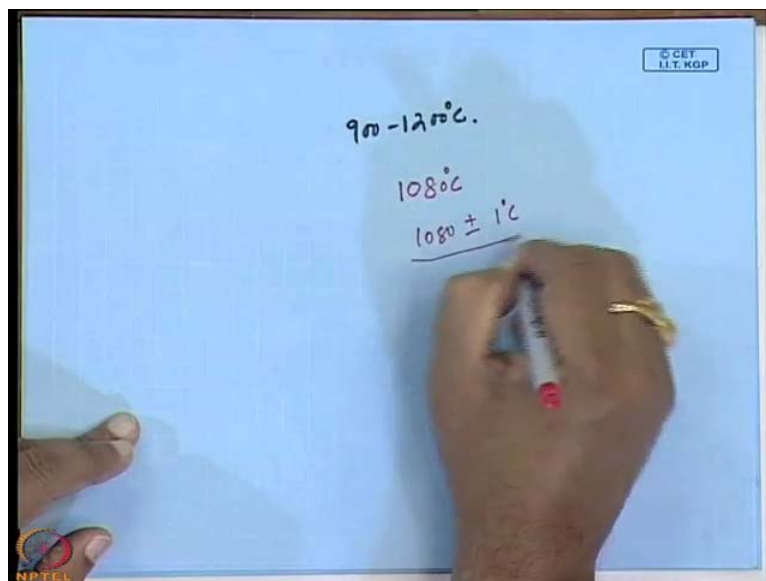


This whole thing is done by the microprocessor that means it is not done by manually microprocessor control system is available to regulate gas flow sequence gas flow. Sequence means first we have to flow the purging gas say nitrogen gas and then oxygen must be transported by some carrier gas say again by argon or nitrogen gas. Generally, argon gas is not used because the purity of argon is not very high compared to nitrogen ideally hydrogen gas can be used, but in this case hydrogen is not used and so the gas sequence.

That means first you purge the reactor with nitrogen, then you send oxygen by some carrier gas, then you stop oxygen, but you flow the carrier gas you meant to flow the carrier gas and then you switch off the carrier gas. So, that the process is completed and this is nothing but the flow sequence which is regulated by the microprocessor system associated in such kind of an oxidation chamber to control the automatic insertion or removal of wafers.

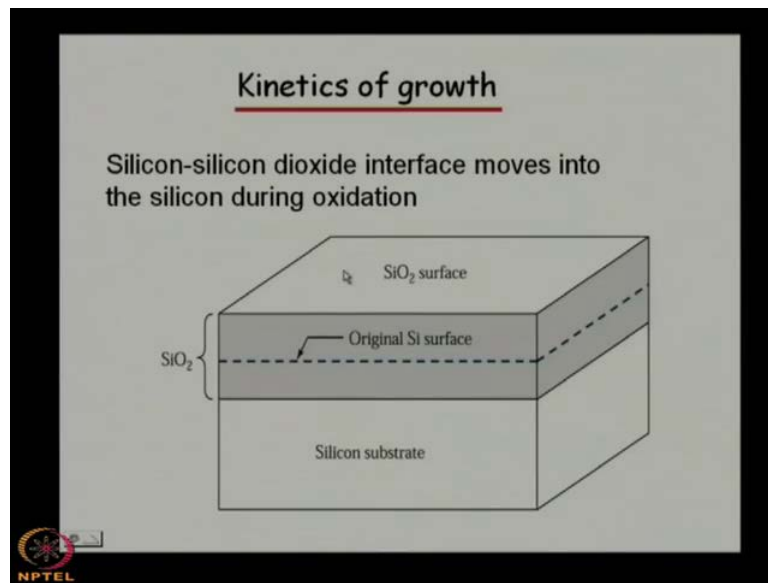
That means we have to load the wafers inside the chamber and at the same time you have to remove the wafer from the chamber. That means after the oxidation is over the temperature is come down from say 1,000 degree temperature to room temperature and then it can be removed. Then, the wafers are oxidized obviously to ramp the temperature up to the temperature of oxidation to avoid warping of wafers due to sudden temperature change to maintain oxidation temperature within plus minus 1 degree centigrade.

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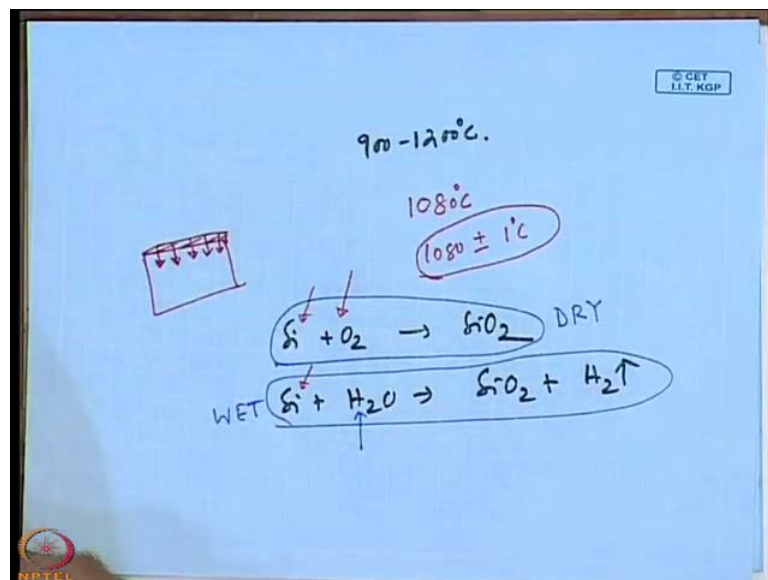
This is very important aspect because you see that when the temperature is 900 to 1,200 degree centigrade. Suppose, I need 1,080 degree centigrade for oxidation and it must be 1080 plus minus 1 degree centigrade that means very precise control of the oxidation temperature is absolutely required. So, that the temperature remains stable for quite sometimes till the operation is completed that means still the all the wafers are oxidized and then to ramp the temperature down again from the say 1,080 to room temperature. So, these are the sequence of events which can be done by a fully microprocessor control system

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Now, when we talk about the growth of the of oxide layers, so let us talk about the kinetics of growth what is kinetics of growth how the oxidation takes place though oxidation takes place.

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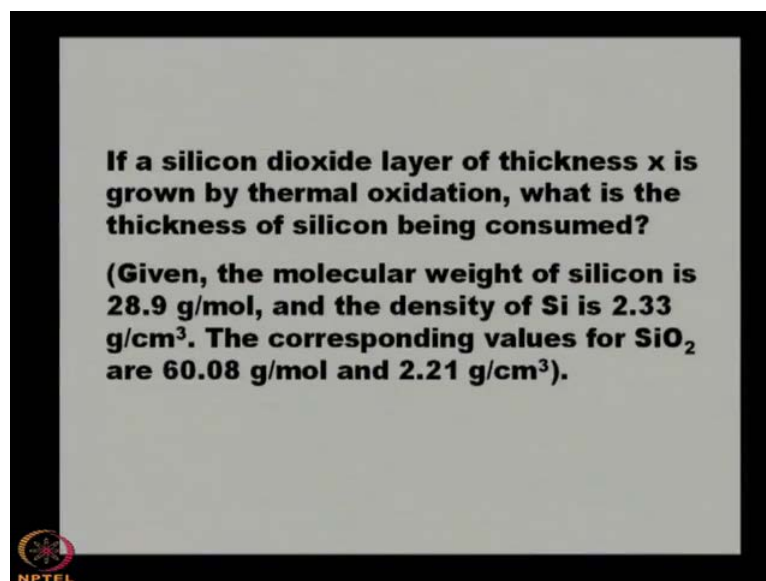


By the chemical reaction, suppose there are silicon and oxygen it will be Si O 2 and if we use the water vapor then obviously there will be Si O 2 plus hydrogen. So, these are the reactions the first one is due to the dry oxidation and the second one is due to the wet oxidation where the water vapor is required now this is the kinetics of growth or the reaction is like this. You

see that silicon dioxide interface moves into the silicon during oxidation that means say this is the dotted line of the original silicon surface and this grey area.

That means this is the oxide layers which is moving inside the silicon during oxidation that means oxidation should take place with the reaction of the silicon and the oxygen or the water vapor and in the process silicon is consumed. I shall show you that 44 percent silicon is consumed for the preparation of SiO_2 out of silicon. So, that means suppose you start from an oxidation this is your silicon first the silicon dioxide is formed at the surface layer then this silicon dioxide layer moves inside the silicon wafer from the surface inside its to its bulk. So, that means some silicon is consumed because that is the condition of the reaction that you need silicon you need silicon, now let us talk about the quantification of the silicon dioxide formed.

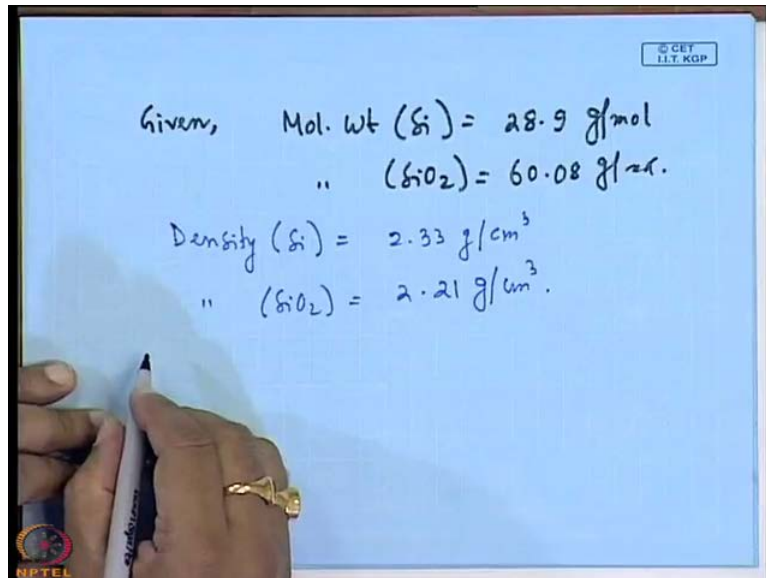
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Let us solve a very small numerical to forward this point if a silicon dioxide layer of thickness x is grown by thermal oxidation what is the thickness of silicon being consumed. If a silicon dioxide layer of thickness x is grown by thermal oxidation, suppose I want a silicon oxide layer of 100 nanometers. So, if I want 100 nanometers, then what is the thickness of silicon being consumed because I have a wafer of says 300 micron or 400 micron or 200 micron thick and I want 100 nanometer of the silicon dioxide layer on the surface if the silicon wafer.

Then, how much silicon wafer is consumed and the values are given that the molecular weight of silicon is 28.9 gram per mole and the density of silicon is 2.33 gram per centimeter cube. It is given and the corresponding value that means the molecular weight of silicon dioxide is 60.08 gram per mole and the density of silicon dioxide is 2.21 gram per centimeter cube.

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So let us try to solve this numerical first thing is that given molecular weight of silicon molecular weight of silicon it is 28.9 gram per mole and molecular weight of silicon dioxide. It is also given it is 60.08 gram per mole and another parameter is given that is the density of silicon is given it is 2.33 gram per centimeter cube and that of density of SiO_2 it is 2.21 gram per centimeter cube. So, these four values are given and we shall try to calculate how much silicon is consumed for the growth of x thickness of SiO_2 or say 100 nanometer of SiO_2 . Now, what is the process, the process is very simple let us try to calculate the volume one.

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Vol. of 1 mol of Si

$$\frac{\text{Molecular wt. of Si}}{\text{Density of Si}} = \frac{28.9 \text{ g/mol}}{2.33 \text{ g/cm}^3}$$
$$= 12.06 \text{ cm}^3/\text{mol.}$$

Vol. of 1 mol of SiO₂

$$\frac{\text{Molecular wt. of SiO}_2}{\text{Density of SiO}_2} = \frac{60.08 \text{ g/mol}}{2.21 \text{ g/cm}^3}$$
$$= 27.18 \text{ cm}^3/\text{mol.}$$

The volume of one mole of silicon first we shall calculate the volume of one mole of silicon and then we shall calculate the volume of one mole of silicon dioxide. Now, how this is calculated it is calculated by very simple relation it is the molecular weight of silicon by density of silicon what is the molecular weight of silicon. It is 28.9 gram per mole it is given and density of silicon it is 2.33 gram per centimeter cube, it is also given and if we simplify it will be 12.06 centimeter cube per mole, so this is the volume of one mole of silicon.

Now, let us calculate the volume of one mole of silicon dioxide then volume of one mole of silicon dioxide Si O 2. We shall use the same formula only in place of silicon we shall use the values for Si O 2 that means molecular weight of Si O 2 by density of Si O 2 what is the molecular of Si O 2 it is given as 60.08 gram per mole and the density of Si O 2 is 2.21 gram per centimeter cube. So, with simplification it becomes 27.18 centimeter cube by mole, so then the next question is how we shall proceed one mole of silicon is converted to one mole of Si O 2.

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1 mol. of Si is converted to
1 mol of SiO₂.

$$\frac{\text{Thickness of Si} \times \text{area}}{\text{Thickness of SiO}_2 \times \text{area}} = \frac{\text{Vol. of 1 mol. of Si}}{\text{Vol. of 1 mol. of SiO}_2}$$
$$\frac{\text{Thickness of Si}}{x} = \frac{12.06}{27.18} = 0.44$$

Thickness of Si = 0.44 x (Thickness of SiO₂)

44 nm. 100 nm

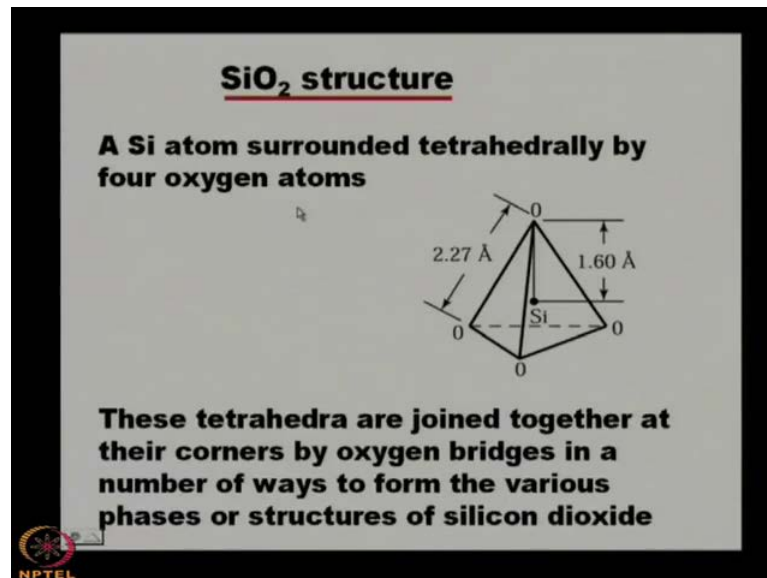
So, that means thickness of Si into area by thickness of Si O₂ into area this is equals to volume of one mole of silicon by volume of one mole of Si O₂. Then, suppose the thickness of silicon is x suppose the thickness of silicon is x and the thickness of Si O₂ suppose the thickness of Si O₂ is x because that is given and the thickness of silicon we would like to calculate. So, this is thickness of silicon this is equals to volume of one mole of silicon we have calculated it is 12.06 by volume of one mole of Si O₂. It is 27.18 and it becomes 0.44 that means we can write thickness of silicon is equals to 0.44 x that means thickness of Si O₂. Now, if we want to grow 100 nanometer of Si O₂ the thickness of silicon becomes 44 nanometer, 44 nanometer.

So, that means 44 percent of the silicon is consumed in the process of SiO_2 , so first what will happen some silicon will react with the oxygen or the water vapor to form SiO_2 layer. That will be governed by the surface reaction and as the silicon dioxide is formed. It will try to penetrate or diffuse because otherwise the oxidation oxidizing species will not be able to react with silicon because silicon is there underneath the SiO_2 layer.

So, the oxidizing species must be diffused through the SiO₂ layer to react with a Si, so that means some part of the Si will be consumed and the SiO₂ layer will be moving towards the bulk of the Si. That means this is moving bulk see this is the dotted line and it is the boundary of the silicon substrate before oxidation starts. After the oxidation is over, you see that the SiO₂ layer which is this grey layer it is going down the dotted line towards

the bulk. That means it is the moving, so that is why I have written that silicon dioxide interface moves into the silicon during oxidation.

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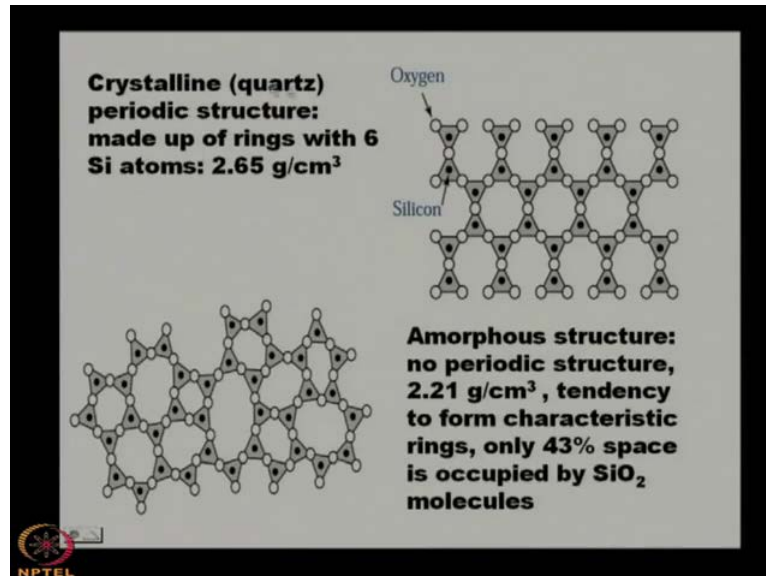
So, that means we have seen that 44 percent of the silicon is consumed in the process, now what is the structure of Si O 2 what is the structure of Si O 2. You see that the structure is very important because not necessarily that Si O 2 will be always crystalline or always amorphous normally the thermal oxidation Si O 2 grown by thermal oxidation is amorphous in nature. Apart from the apart from the crystalline amorphous nature there are crystalline structures which are known as the quartz because Si O 2 you know that it is known as the silica in some cases and quartz is a form of silica which is crystalline in nature.

Now, let us talk about the Si O 2 structure a silicon atom you see that surrounded tetrahedral by four oxygen atoms. So, this is silicon atom and four oxygen atoms are surrounded tetrahedral and this is a tetrahedron structure. The inter nuclear distance between oxygen and silicon is 1.6 angstrom while the inter nucleus distance between oxygen and oxygen is 2.27 angstrom here also it is 2.27 angstrom.

So, this is the tetrahedron structure of a silicon atom surrounded by four oxygen atom it is one unit this tetrahedral are joined together at their corners by oxygen bridges in a number of ways to form the various phases of or structures of silicon dioxide. These tetrahedral are joined together at their corners by oxygen bridges in a number of ways to form the various phases or structures of silicon dioxide. Now, depending on the structure that means the

oxygen bridges and it can be amorphous it can be crystalline in nature and two types of structures.

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I shall show you one is the crystalline or the quartz another is the amorphous structure and in this crystalline structure you see that these are the rings. This is the one thing is that it is a long molecular structure periodic structure and made up of rings with six silicon atoms you see 1, 2, 3, 4, 5, 6. Here, you see 1, 2, 3, 4, 5, 6 silicon atoms are there and they form a ring one ring second ring third ring fourth ring and so on. There will be a large number of rings and all the rings you see that made up of rings with six silicon atoms and the density is 2.65 grams per centimeter cube. Now, if you compare this structure with this amorphous one you see that almost there is no periodicity in this structure if you compare this two structures and the density is 2.21 gram per centimeter cube.

So, obviously the crystalline structure is more dense or denser than the amorphous structure so it means that the amorphous structure there must be some porosity and you see that only 43 percent space is occupied by SiO_2 molecules. That means there are empty spaces and only 43 percent of the space is occupied by SiO_2 molecule. So, that means there are a large number of pores inside the structure and so the diffusion of the impurity is possible and another thing is that there is a tendency to form characteristic ring, but not with the six silicon atom.


Here, the black dots are the silicon atom, so 1, 2, 3, 4, 5, 6 here you see 1, 2, 3, 4, 5, 6, but here you see 1, 2, 3, 4, 5, 6, 7 8 here you see one 2, 3, 4, 5. Here, you see 1, 2, 3, 4, 5, 6, 7, so though there is a tendency to form characteristics ring, but this is very haphazard in manner and so it is amorphous in nature. So, basically the building block is the tetrahedron where the silicon is at the center with four oxygen atoms tetrahedrally. This is one unit which is repeated here because of the bridging by oxygen and depending on the formation of the rings one is crystalline which is one form of crystalline and another is amorphous nature and in our discussion. Since we are growing Si O 2 with thermal oxidation that thermal oxidation gives you the amorphous nature and that is why it there is a tendency that diffusion or impurity can penetrate through Si O 2 layer in this case.

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Oxide thickness after an oxidizing time t

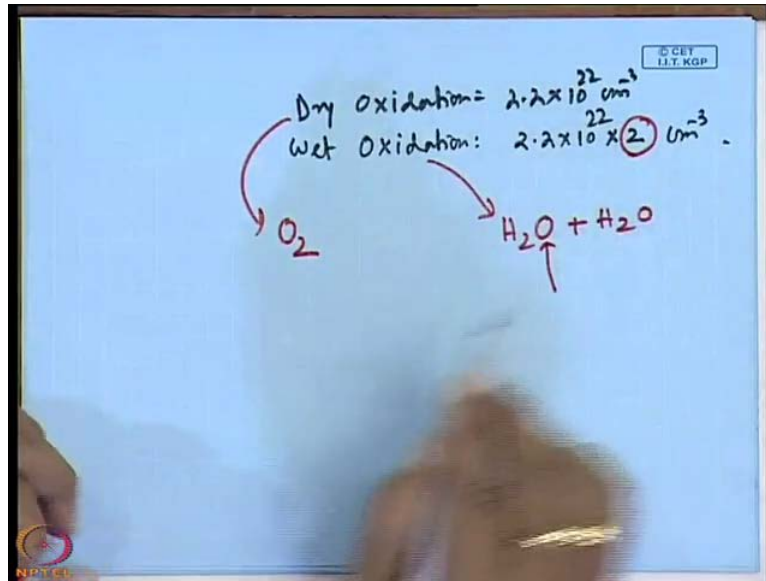
$$x = \frac{D}{k} \left[\sqrt{1 + \frac{2C_0 k^2 (t + \tau)}{DC_1}} - 1 \right]$$

D: diffusion coefficient of the oxidizing species; k: surface reaction rate constant; C₀: surface concentration of oxidizing species, C₁: 2.2 × 10²² cm⁻³ for dry oxygen, and τ represents a time coordinate shift to account for the initial oxide layer.



Now, if we consider the growth model you see that oxide thickness after oxidizing time t is given by this relation. So, this is available from any standard textbook you find and the constants there are some constants d is the diffusion coefficient of the oxidizing species k is the surface reaction rate constant. Then, c 0 is the surface concentration of oxidizing species and tau is represents a time coordinate shift to account for the initial oxide layer. This c 1, c 1 is another surface concentration of oxidizing species its value is 2.2 into 10 to the power 22 for dry oxygen and if you use the wet oxidation.

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For wet oxidation, its value will be 2.2 into 10 to the power 22 multiplied by 2 centimeter cube inverse why for dry oxidation it is 2.2 into ten to the power 22 why there is a factor of 2 to be multiplied with this one. It is because you see that for dry oxidation oxygen molecule is used whether two atoms of oxygen for wet oxidation water vapor is used where there is only one oxygen. So, there must be two water vapors to complete the reaction, so that means it must be multiplied by 2 so the value of c_1 will be different for different methods of oxidation be dry or wet.

You see that with this thickness with this thickness of the oxide layer there are two terms which I shall define. One is the parabolic rate constant another is the linear rate constant this is the reaction gives you the oxide thickness of x equal to something and for small t .

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For small t

$$x = \left(\frac{2Dk}{q} \right)^{1/2} (t + \tau)$$

For large t

$$x = \sqrt{\frac{2Dq}{c} (t + \tau)}$$

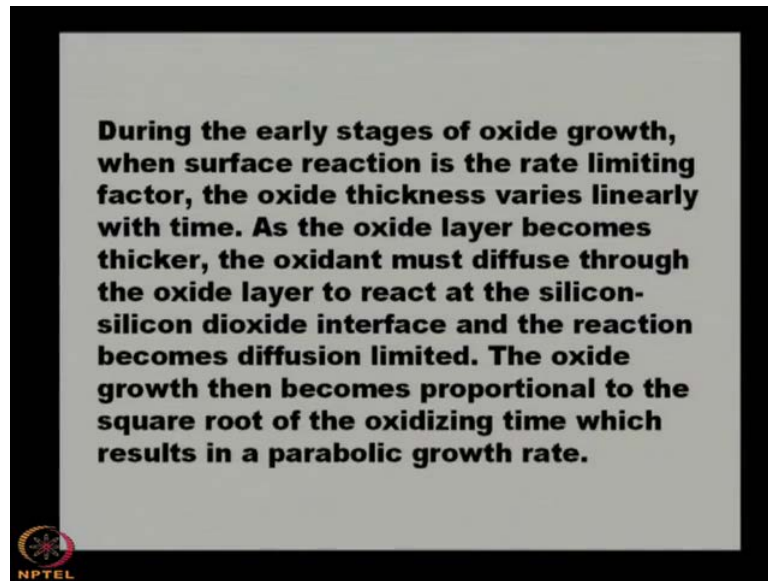
$$x = \frac{B}{A} (t + \tau), \quad \frac{B}{A} = \frac{kq}{c}$$

$$B = \frac{2Dq}{c}$$

For small t , you see that x will be equals to twice, sorry x will be equals to $C_0 k C_1 t$ plus τ that is for small t and for large t for large t x will be root over of twice $D C_0$ by $C_1 t$ plus τ . So, this is nothing but the simplification of this thickness oxide thickness for larger t and smaller t for smaller t . You see that it is the that can that expression can be simplified to this one for larger t that expression can be simplified to this thing and from here x can be written as this x can be written as B by A t plus τ where B by A is given by $k C_0$ by C_1 .

That means this is B by A , so this can be simplified to x equals to B by A t plus τ and for larger t . This expression can be simplified to x equals to sorry x square equals to B t plus τ where B is given by where B is given by twice $D C_0$ by C_1 this is B and this is B by A . So, what we see that here it is the linear thing and here it is the parabolic thing, so we can say that B by A is referred to as the linear rate constant and this B is known as the parabolic rate constant. This is parabolic rate constant and this is linear rate constant because this is the expression for a parabola and this is the expression for a linear variation, so we can conclude that during the early stages of oxide growth.

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When surface reaction is the rate limiting factor surface reaction that means the rate of formation of oxidation is due to the surface reaction and in that case the oxide thickness varies linearly with time that means x equals to $\frac{v}{A} t + \frac{B}{A}$ $\frac{B}{A}$ is the linear rate constant. It is due to the surface reaction, but as the oxide layer becomes thicker the oxidant must diffuse through the oxide layer to react at the silicon dioxide interface and the reaction becomes diffusion limited the oxide growth. Then, becomes proportional to the square root of the oxidizing time which results in a parabolic growth rate that is why you see that it is x^2 equals to $\frac{B}{\tau} t$ that is the parabolic growth rate.

So, with this we conclude today that the oxidation for the initial stage it is the linear variation, so $\frac{B}{A}$ is known as the linear rate constant and as the reaction starts and it continues, then it becomes parabolic in nature due to the diffusion of the oxidizing species inside the SiO_2 towards the Si surface.

Thank you.