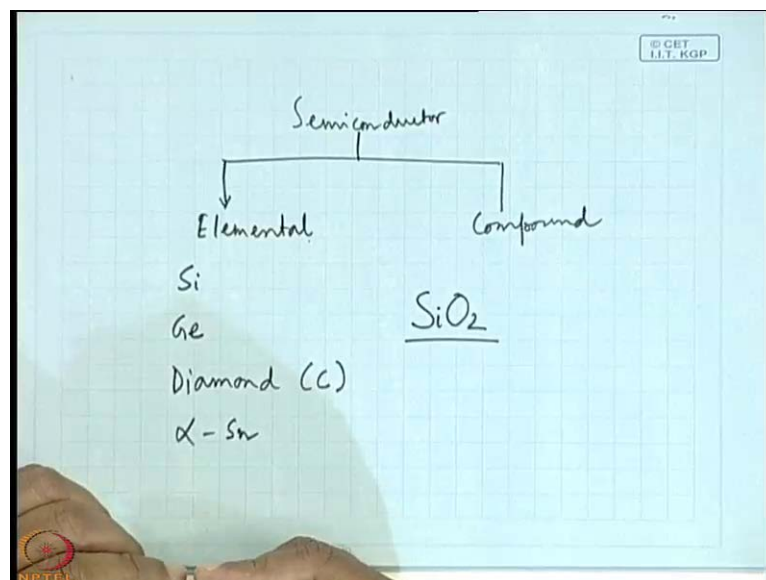


Processing of Semiconducting Materials
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Lecture - 10
Elemental Semiconductors

Today, we shall discuss about the Elemental Semiconductors. You know that the electronic materials are mostly semiconductors and it can be categorised into a large number of materials; practically it is a material family. And, broadly we can divide semiconductors into two groups; one is the elemental semiconductor, another is the compound semiconductor.

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So, one is elemental, another is compound. As the name implies that this elemental semiconductors, this is a particular element or a material and it is not a compound at all. See, if I would like to name some of the elemental semiconductors; obviously silicon, germanium, diamond. You know that diamond comes from carbon basically, then gratin which is known as alpha sn. So, these are materials, which are the elemental semiconductors. Now, among these semiconductors materials, which are elemental in nature, silicon is the most important electronic material; because of its application in the integrated circuit. Now, what are advantages of silicon? Let us first see.

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Advantages of Si

- Relative ease of passivating the surface by oxidizing it in a controlled manner.
- This stable native oxide layer, thus formed, reduces the surface recombination velocity.
- Its hardness allows large wafers to be handled safely.
- Its thermal stability allows high temperature processing related to diffusion, oxidation, annealing, etc.
- Low cost



The advantages of silicon, there are many advantages. One of the advantages is the relative ease of passivating the surface by oxidizing in a controlled manner. Now, what is the implication of this statement? Relative ease of passivating; you see that I have mentioned here, the relative ease of passivating. First term, which is coming is passivating. What is passivation? Can you tell me, what is known by the term passivation? And there is a clue; there is a clue that passivation of the surface. So, what is passivation? Making a surface (()) exactly.

And, if you tell me why this is required, because you see that; silicon or any material basically it is covalent bonding are there. And if you cut a piece from it say this is a silicon crystal and you are taking a cut of it; so, what will happen? Basically, you are cutting the bonds; you are cutting the bonds. You do not know actually, somewhere there will be bond.

So, at that top of the surface there will be unsaturated bonds, which are known as the dangling bonds. And these dangling bonds are very reactive. So, that is why if you keep a piece of particularly silicon or that type of material; within a few second, a thin oxide layer will go at the surface. It is because of, it will take the areal oxygen. And, if you if it takes the areal oxygen from the atmosphere, then with the unsaturated bonds; there will be an oxide layer of SiO_2 , very thin layer of SiO_2 .

Now, for silicon this is very advantage; this is an advantage. Why? Because SiO_2 can be made very easily. This is basically known as the oxidation. So, when you come to learn about the different steps of IC fabrication in your semiconductor technology class, you will find that oxidation is an important step for fabrication of integrated circuit; like your ion implantation, diffusion, annealing, lithography. So, oxidation is very important term or the process basically. This oxidation in silicon it can be done very easily unlike in germanium. You cannot grow germanium oxide very easily on the germanium substrate or the germanium wafer. Why? Because it is unstable in nature; you do not have any control on it. If you take another example for say gallium arsenide, indium phosphate; there are several types of semiconductors, cadmium telluride, zinc oxide.

Oxidation layer in control manner growing, growth of oxidation layer in a controlled manner is very difficult except in silicon. So, that is advantages that you can grow SiO_2 in a very controlled manner. Because that is a you know that this silicon is basically the host metrics. Silicon is the host metrics here and always there will be dangling bonds. So, by passivation what is the advantage of passivation? Why we need passivation?

Student: (())

No, one is reactivity will be reduced that he told earlier; then, what is our application point of view. So, for our application point of view, what is the advantage?

Student: (())

No, No. Not only dust or impurity, the advantage is.

Student: (())

Yes, diffusion. During diffusion or ion implantation or lithography, you know that masking is done and here SiO_2 and acts as a mask for those processing. So, that is very important thing. And, in some devices like a mosfet, you need an oxide layer MOS; Metal Oxide Semiconductor. So, for silicon it is the god gifted item that silicon oxide can be done very easily and without any difficulty and it is very stable. So, that is why MOS can be fabricated very easily using silicon. Such thing is not there for compound semiconductor like gallium arsenide, indium phosphate. It is not very easy to deposit gallium oxide; there is no such massive or technology these days.

So, that is one important thing that you can oxidize the surface to passivate the dangling bonds. And, this stable native oxide; thus, formed you see that I have mentioned that this stable native oxide this stable native oxide layer thus formed reduces the surface recombination velocity. That is another advantage for the oxide layer. Now, what is surface recombination velocity? What do we mean by surface recombination velocity? Can you tell what is surface recombination velocity? Suppose, you are you are making one photo detector you are making one photo detector, which detects light. So, for photo detector generally light falls on a substance on a surface.

So, if this is a silicon material and light falls on it, on its surface, it is incident on its surface. Then, what will happen? The light will be absorbed by the Surface only. Because of the oxide layer etcetera, it will be absorbed by the surface. Another point is that as soon as it will be absorbed in the surface, electrons and holes will be generated and those electrons and holes will recombine in the surface itself without going inside the bulk of the material. So, that means the output from the detector will be very, very less because that will be a surface phenomena, that will be a surface phenomena. But we want to exploit the hole of the bulk. If I use a 300 micron semiconductor and the surface is say 1 micron, 2 micron or 10 micron; then, what about the rest 250 to 300 micron?

So, we cannot exploit the electrons and holes in the bulk of the material. So, if you passivate the surface, then the surface recombination velocity becomes less. That means, the recombination will not be held in the surface itself, it will be held in the bulk of the material obviously, the recombination of the electrons and holes. Another important advantage of silicon is that its hardness allows large surface wafers to be handled safely. You know that this processing technology of silicon, it is basically the processing technology is silicon it is basically, 6 inch 8 inch or even 12 inch wafer is handled. That means the whole wafer is placed inside the furnace or inside the ion implanter or inside the diffusion chamber for processing. Basically, it is a planar technology.

Planar technology means say this is your substrate or the wafer; the whole wafer is processed. First there is a oxide layer all through the surface of the wafer. Then, there will be photo lithography, then there will be etching, then there will be diffusion or ion implantation, then there will be metallization. So, this whole planar technology we use generally the large wafer; that means 8 inch, 12 inch, 14 inch wafers are used. So, for the for those processing basically, you need some hard materials; otherwise, what will be

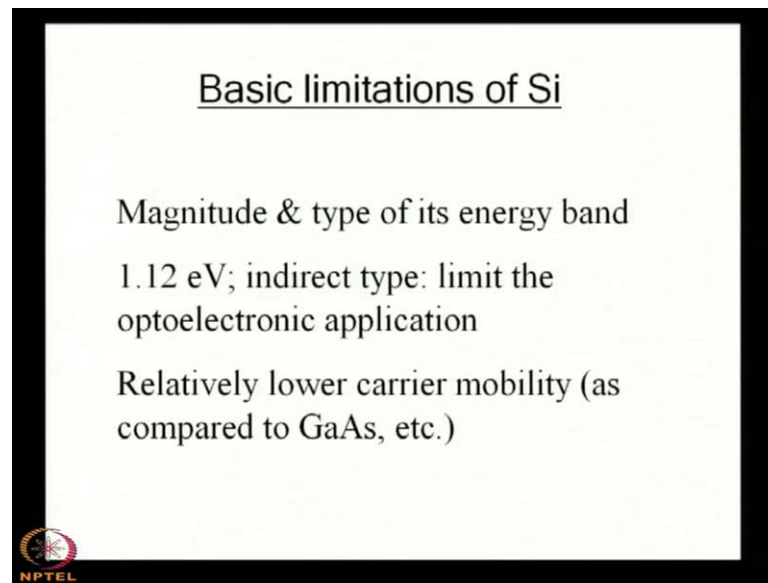
happened? If it is brittle then during processing, it will be broken. So, that is the reason that its hardness compared to indium phosphate, gallium arsenide; the compound semiconductor, the silicon is more hard compared to the other compound semiconductors or the elemental semiconductors.

Another thing is the its thermal stability, allows high temperature processing related to diffusion, oxidation, annealing etcetera. High thermal stability; thermal stability is very high. That means, processing temperature can be very high. Because we discussed in our diffusion and in implantation, that particularly for diffusion 1000 degree, 1200 degree centigrade temperature is required. For oxidation high temperature is required. After ion implantation, what we do? We subjected the material into annealing right can you remember that annealing is done rapid thermal annealing or conventional type of annealing is done.

So, all those steps all those processing, basically related to high temperature. So, that means it must withstand very high temperature otherwise there will be thermal degradation of the material. So, that is another advantage that high thermal stability, it allows and low cost; because you know that the silicon is basically freely available in nature it is abundance. So, it is the costing is very low compared to other material because other material cannot be naturally obtained. Say germanium or gallium arsenide or indium phosphate or nitrite semiconductor; naturally it is not generated. You have to use some chemical means; so, me processing technology special techniques for the growth of those materials.

But silicon is abundance in nature and during our crystal growth, I shall show you that how silicon is taken from the normal sand, it is processed, purification etcetera and then bulk silicon crystal is grown. The and a piece of those silicon crystal, which is known as the wafer of the substrate is used for IC technology. So, that is abundance in nature; that is why it is low cost. So, this is these are the advantages of silicon; the most important advantage is that the oxidation which is not available for other materials.

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Then, what are the limitations of silicon? Is there any limitation for silicon? Yes, there is limitation for silicon. One limitation is the magnitude and type of its energy band. The magnitude is 1.12 electron volt. So, this 1.12 electron volt is an energy which is associated with the emission at the 1.1 micron. What is the relation between the band gap and the emission wave length of a semiconductor? λ equals to $1.24 \text{ by } E \text{ g}$. So, if you use this 1.12; so, you will get just only one wave length. It is not suitable for visible obviously because the band gap is 1.12 eV. So, it is infrared not visible region and it is indirect type.

We know we have discussed that indirect type limitations is that, it cannot be used for optoelectronic sources because of the conservation of momentum. So, that is why it limits the optoelectronic application. So, that is the silicon is not user for particularly optoelectronic sources, you cannot make led or laser from silicon. Another important limitation for silicon is that, it is the, it has lower carrier mobility; lower carrier, what is mobility?

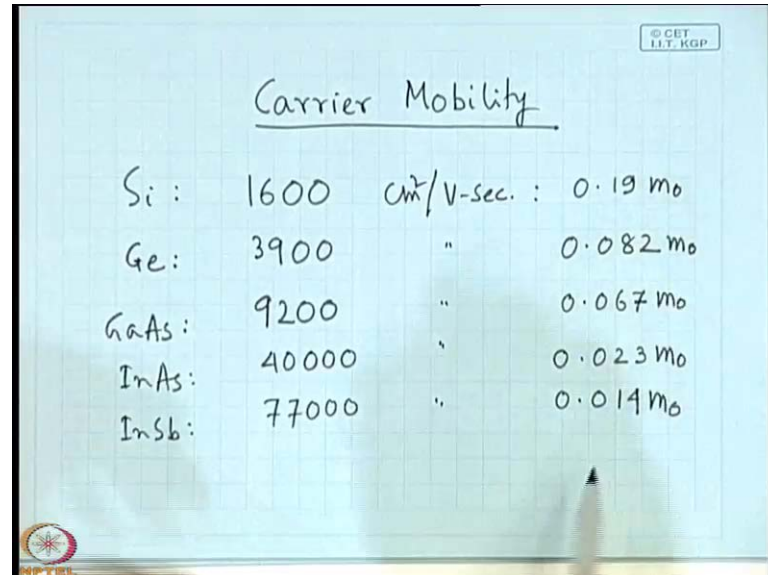
Student: (())

Drift velocity per unit electric field. So, this carrier mobility, that means mobility of electrons or holes; because when we talk about mobility in a semiconducting material there are two mobilities. One is the electron mobility electron mobility, another is the hole mobility and why the mobilities differ? Why there is a type of differ in mobilities?

Student: (()).

Yes, because of the difference in effective mass, you will get different values of the mobility.

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Si :	1600	cm ² /V-sec. :	0.19 m ₀
Ge :	3900	"	0.082 m ₀
GaAs :	9200	"	0.067 m ₀
InAs :	40000	"	0.023 m ₀
InSb :	77000	"	0.014 m ₀

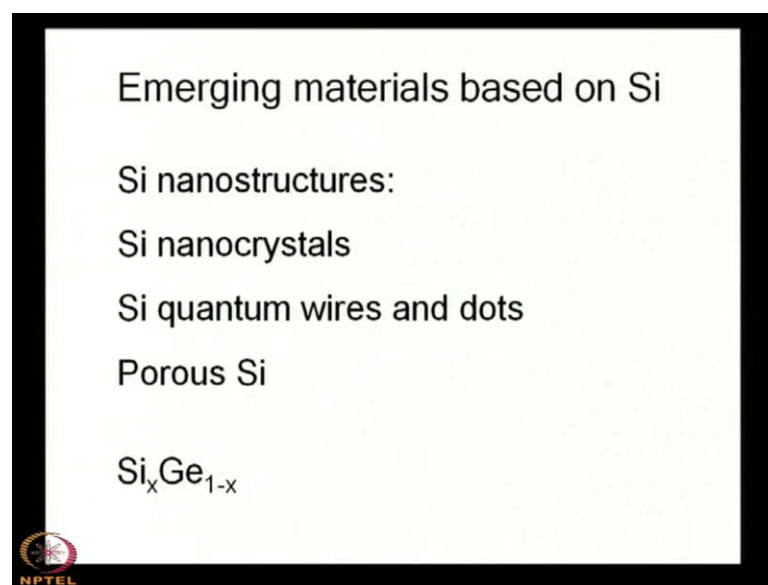
So, now carrier mobility say for silicon the mobility is 1600. Obviously, it is centimetre square per volt second in CGS unit. I am writing the electron mobility not the hole mobility, right. Then, for silicon it is 1600 centimetre square per volt second; then germanium it is 3900, but if you compare with gallium arsenide it is 9200 or say indium arsenide it is 40,000 or indium antimonite it is 77,000 very high mobility. So, these are the mobility's of different kind of semiconductors and if you compare this mobility you will see that for silicon, the mobility is very less it is 1600 only.

So, this is another limitation because if the mobility is very less; so, that means you cannot use those material for high frequency devices, high frequency devices. Because only integrated circuit is not the end; you have different types of devices. One is say laser, LED, detector, then microwave sources, impact diode, read diode, pin diode etcetera; there are different types of devises. And microbe devices is very important for particularly this communication type of thing, for modulation of signal etcetera.

So, silicon is not used because the of its bent of its mobility; the mobility is very less compared to say gallium arsenide or other materials, say indium antimonite 77,000 is

very high. And, this mobility is high because of the electron effective mass. You see that for silicon the electron effective mass is 0.19 and for germanium it is 0.082, for gallium arsenide it is 0.067, for indium arsenide it is 0.023 and it is 0.014. These are effective mass 0.19 m_0 , 0.082 m_0 , 0.067 m_0 , 0.023 m_0 and 0.014 m_0 ; what is m_0 ? m_0 is the mass which is given by 9.1×10^{-31} kg. So, you see that basically as the effective mass decreases the mobility increases. So, this mobility is an important parameter for selecting a material for a particular application and for silicon, we find that it is not suitable for many applications.

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So, what are emerging materials based on the silicon? Because silicon is very cheap, it has many advantages, it is readily available in the nature and obviously it is a the technology is very mature, because of the IC processing technology. So, can we use silicon for those applications, where there elemental silicon cannot be used? Yes, there are many types of methodologies using which you can use silicon in different kinds of applications. One is the, one is based on the silicon nanostructures. And, we have heard the name of nanostructure and what is nanostructure?

Student: (())

Within.

Student: (())

No, that is not the definition. What is basically nanostructure?

Student: (())

Exactly, exactly. Because of the structure some of the properties are changed and those are available, when you reduce the dimension of the material to what he said in the nanometre region; say 10 to the power minus 9 . So, what are the implications of nanostructures? Implication of nanostructure is that, during a fabrication of nano, the motion of the carriers is quantized. Now, what is through means of the motion of the carriers is quantized? Say you are in this room, you are in this room.

Now, in this room you can move in all the three directions x , y , z . Now, suppose if the height of the roof is reduced, if the height of the roof is reduces to say 4 feet from the floor; can you move in the z direction? You cannot move in the z direction. You have, your only option is to use the x , y plane. That means, you can move along the x , y plane; but you cannot move along the z direction. So, that means you movement is confined in the x , y plane. So, two dimensional effect will be there.

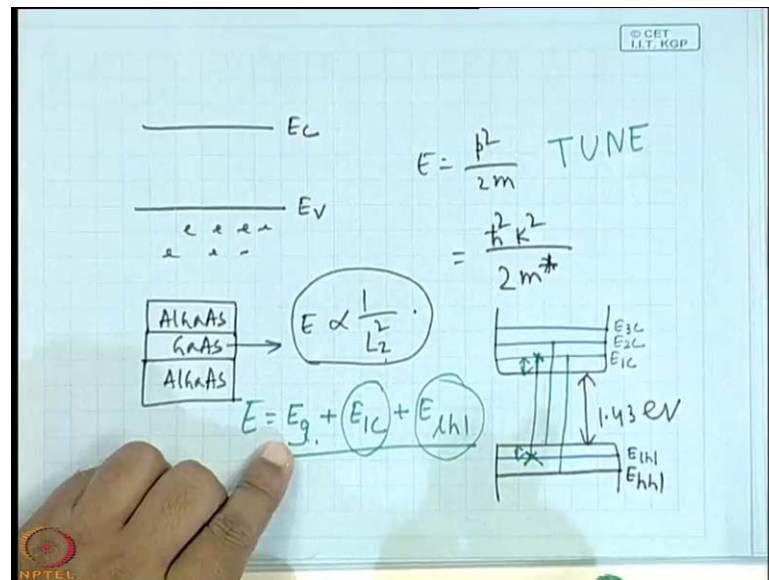
So, though you are a three dimensional material, you are a three dimensional species; even then you cannot use the z direction because of the reduction in the dimension. Similarly, suppose you are standing in this room and this two walls are made closer to each other. Then, what will happen? You can move along this z direction, but you will not be able to move around this x , y direction.

So, that means your movement is quantized now; only in one direction, your motion is allowed, right. So, there are the examples of the confinement and when we tell that it is a carrier confinement, effect carrier confinement means the confinement of the electrons and the holes. In our case, if you use a metallic film then it the electron only, because you know that the concept of hole is not there in metal or in other materials except in case of semiconductors.

So, when we talk about the confinement of something that means it is the confinement of the electrons and holes. Confinement of what? Their motion, their movement; we are restricting their movement. So, under such a circumstance because of the quantum mechanical phenomena, many new things happens; the density of states is changed. Density of state, what is density of state? Actually, per unit volume the number of

available states for a particular carrier number of available states; available states mean? Let us take the same example, that suppose there is a material and at normal temperature the hole and the electrons are there in the valence band. So, if you excite the electrons then what will happen?

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They will move to the density of state, the electrons are there in the valence band and if you excite the electrons; so, they will move to the conduction band. That will depend on the density of states in the conduction band, number of available states in the conduction band; in the conduction band that is the density of states per unit volume. That is why it is known as density. So, it will depend on the density of states. Now, during quantum mechanical treatment or if your movement is restricted; if your or movement is confined, then there density of states for bulk material it is, what is the nature of the bulk material, density of the states? It is parabolic in nature equals to $\hbar^2 k^2$ by twice m^* E equals to P^2 by $2m$.

So, E equals to p^2 by $2m$ and what is p $\hbar k$; so, $\hbar^2 k^2$ by twice m^* in our case. Because we have discussed about effective mass; because of the curvature in the bands, we do not use the normal rest mass. In our case, we use the effective mass; so, this is parabolic in nature, this density of states is parabolic in nature. But if the confinement is there and the motion is reduced, it is confined; then, this density of states will be different from the bulk density of states. It may be staircase

function and other functions are there; I am not going into details of those thing use of mathematical.

So, you can you can calculate those thing from by solving the Schrodinger wave equations. But in our case we will not go into those thing; only we can assume that because of the restriction or the confinement of the movement of the carriers, new phenomena is observed. And, that is the implication of the nanostructures and many properties; I shall show you some of the properties in our lecture, that many properties are changed. One thing is that the energy is proportional to $1/L^2$; energy becomes proportional to $1/L^2$ L means it is considered as one dimension.

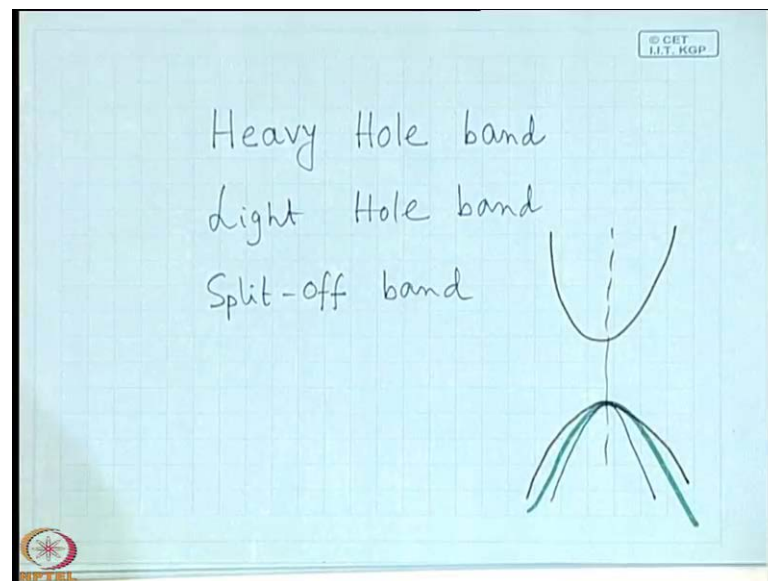
Basically, one dimension it is it is a thickness it is a thickness; if you sandwich one material say this is one material, say it is aluminium gallium arsenide. Then, you sandwich gallium arsenide between two aluminium gallium arsenide, this structure. You have sandwiched one gallium arsenide, this is the gallium arsenide layer between two aluminium gallium arsenide layers. So, if this gallium arsenide layer is very thin say of the order of say 50 angstrom, 60 angstrom, 100 angstrom. That means, 10 nanometre, 12 nanometre, then what will happen? The energy will be proportional to $1/L^2$. If L is the thickness of the gallium arsenide layer; so, it acts as a quantum well, it acts as a quantum well.

Quantum well means, there is a boundary in between, there is a well and you can solve the Schrodinger waves; all the physics students we have already solved this thing. And, you have calculated this thing also. For a infinite quantum well, it becomes E proportional to $1/L^2$ right and this. So, what we find? That just by changing the value of the thickness L , just by changing the value of the thickness L you can change the energy; you can change the energy, right. Till now what we know? We know that the band gap of gallium arsenide is 1.43 electron volt. So, the energy associated with gallium arsenide is 1.43; there is a constant thing. But now, you can change the energy of the gallium arsenide by changing the value of L .

What will happen? You see that this is 1.43; the band gap of gallium arsenide. And, the conduction band will split into a number of levels 1, 2, 3 etcetera; it will split into number of levels. Why there will be a splitting? The splitting will be due to quantum mechanical phenomena. Because of your confinement of carriers, because we have

restricted the motion of the carriers; there will be splitting of the energy level, this is E_{1C} , C means conduction band then E_{2C} , E_{3C} etcetera. Similarly, the valence band will also split. This valence band will be E_{lh1} ; lh means light hole. How many bands are there in the valence band? In a valence band, when we talk about the valence band basically there are 3 bands. One is light hole band, another is heavy hole band and third one is split of band.

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One is heavy hole, another is light hole and third one is split off heavy hole band light hole band and split off band. Generally, 3 bands are there; that means your structure will be like this. There will be 3 bands; one is heavy hole, another is light hole and 3rd one is split off. So, these valence bands will also get splitted and the splitting of the valence band will be E_{lh} . That means, light hole one say then E_{hh1} and so on. We do not know actually how it will split, but there will be the splitting of the bands both in the valence and the conduction bands.

Now, what will happen? The implication of this is that you see. First case, in gallium arsenide only transition in 1.43 is available 1.43. That means, if an electron moves from the valence band to conduction band, then how much energy is required? 1.43 electron volt. And, then if it again comes back to the original position in the valence band, there will be electron and hole recombination. And you will get the energy to be emitted in the electromagnetic wave; as the electromagnetic wave, right. What will be the measurement

of that energy? 1.43, it cannot be more than 1.43. In this case, it will be more than 1.43, how? Because you see that the transition can be from this level to that level or from this level to that level or from this level to that level.

There are many transitions possible. So, if we assume that the transition is from this level to that level; that means, energy will be band gap E_g plus E_{1C} that means this portion plus E_{h1} that means this portion. So, the final energy becomes greater than E_g . Now, you can tune the band gap by changing E_{1C} and E_{h1} , how? Because you can change the splitting; the splitting depends on the value of L_z , the splitting depends on the value of L_z . You can write a program, you can solve iteratively then you can plot energy verses thickness. Then, you choose a particular thickness to get one particular energy. But the material is same; remember, the material is gallium arsenide. And, it is applicable for any material, it is applicable for any material. So, that is the implication of the nanostructure. What happens?

First you confine the carriers to a particular dimension; then, what will happen? Its energy will split and you can expect more energy involved in the structure greater than its band gap. And, you can tune those energies, E_{1C} or E_{h1} etcetera. This depends only on the value of the thickness of the material, right. If you have any question, you can tell. This is the quantum confinement phenomena or effect and it gives you the energy, which you can tune you can tune the energy; you can tune the energy to your possible application. What is E , which one total energy total energy for this energy involved.

Now, suppose there is a recombination of electrons from this structure, then you can expect that the emission wave length will be E_g plus E_{1C} plus E_{h1} . Earlier only E_g was there in bulk material only E_g is there you cannot change the value of E_g because that is the intrinsic property of the material but in this case you can tune the energy for a particular application. So, we find that in silicon also there are emerging materials which are based on silicon those may be silicon nanostructures. The silicon nanostructures involve silicon Nano crystals silicon, quantum wires and dots, porous silicon these are three nanostructures related materials. And, in all the cases silicon is involved you see because silicon has certain advantages that we have discussed earlier.

So, because of these things that using silicon, people have been trying to obtain different kinds of properties; which are not there for in bulk silicon. Like its application in

optoelectronic materials that is not possible in bulk silicon or crystalline silicon. That is why people have been trying for silicon Nano crystals or silicon quantum wires and dots or porous silicon. And, another important this is not a nanostructure, but it is bulk material it is silicon germanium; you see that silicon x germanium one minus x. So, you can mix silicon germanium and first I can discuss these materials silicon germanium a little bit because if you see that the carrier mobility of silicon if you see that the carrier mobility of silicon it is 1600 but for germanium it is 3900. So, using silicon germanium you can increase the mobility little bit because the mobility will vary from 1600 to 3900.

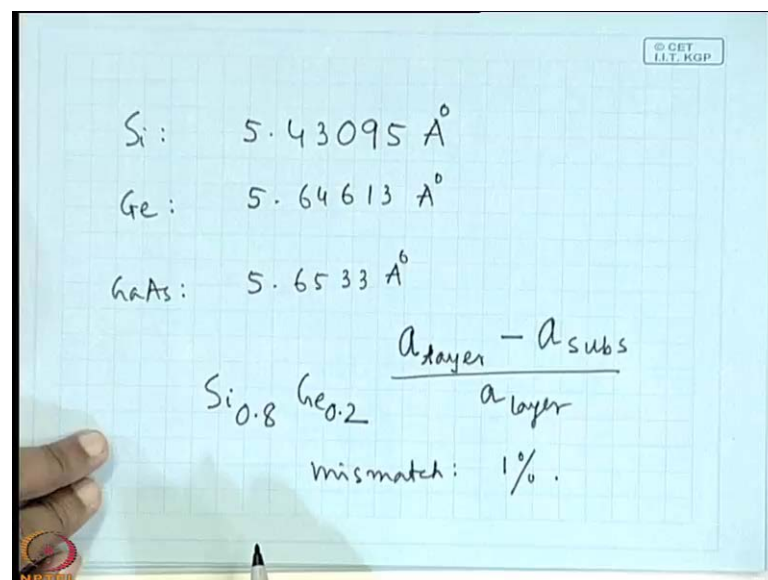
So, you can tune the mobility one part; another thing is that the band gap of silicon is 1.12 and the band gap of germanium is 0.6767. So, you can tune the band gap also from 0.67 to 1.12. Some variation you can make which otherwise is not possible using silicon. In silicon it is fixed band gap 1.12 electron volt, but here you can tune the band gap. Hence for this silicon germanium material I have one thing to add that you know that in compound semiconductors; and I shall discuss that in next class that gallium arsenide or indium phosphate. The processing technology is not very matured like silicon annealing, oxidation, implantation, diffusion, lithography there are various standard technique for silicon only.

You cannot use those processing technology or large wafer cannot be handled for compound semiconductors like a silicon where you can handle very large wafer. So, those are the advantages of silicon. And, how you can grow how you can fabricate gallium arsenide on silicon? Because normally gallium arsenide is made on gallium arsenide. Suppose this is gallium arsenide wafer; so you have to use a gallium arsenide wafer for the fabrication of gallium arsenide layers or p- n junction or MOS device. Whatever be the device you would like to do on gallium arsenide; why because of the lattice matching problem. We shall discuss those things also because we have a lattice matching problem.

A wafer has a lattice constant, a substrate has a lattice constant and on which the layer or the crystals will be grown; the crystal has a lattice constant. So, those two lattice constant must be similar in nature, must be equal in ideal case otherwise what will happen? The lattice will mismatch, and then what will happen?

At the inter phase between the substrate and the layer there will be defects at dislocation, there will be imperfections. So, when the electron will move from the layer to the substrate or from the substrate to the layer; they will be scattered or trapped inside the inter phase layers. So, that means your mobility will further reduce your mobility will further reduce or for optoelectronic device those will act as a trap centre. They will act as a killer centre the recombination will be from those trap and the electron. So, no light will be emitted the energy will be dissipated as a heat right. So that is important thing that this silicon germanium, you can use to grow gallium arsenide. Why? The lattice constant of germanium and lattice constant of gallium arsenide is same.

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Handwritten notes on a grid background showing lattice constants and a mismatch calculation. The text is as follows:

Si: $5.43095 \text{ \AA}$
 Ge: $5.64613 \text{ \AA}$
 GaAs: $5.6533 \text{ \AA}$

Below these, the formula for mismatch is written:

$$\text{Si}_{0.8}\text{Ge}_{0.2} \quad \frac{a_{\text{layer}} - a_{\text{subs}}}{a_{\text{layer}}}$$

Below the formula, the result is written:

mismatch: 1%

If I give you the value of lattice constant, you will find that lattice constant of silicon it is 5.43095 angstrom, lattice constants of germanium it is 5.64613 angstrom, lattice constant of gallium arsenide 5.6533 angstrom. So, what you find that the lattice constant of germanium and gallium arsenide is almost same almost same. So, that means mismatch is less in case of germanium on gallium arsenide or gallium arsenide on germanium.

But if you think of silicon and germanium the mismatch is comparatively high. How the mismatch is calculated? The mismatch is calculated by this formula that lattice constant a of the epitaxial layer or the layer; layer minus a of substrate by a of layer. Using this formula you can calculate the lattice lattice mismatch into 100 percent into 100 percent. So, if you take the value of say germanium and silicon; so you can find that it is almost 4

percent. If you use this 2 value germanium and silicon suppose you would like to grow germanium layer on silicon substrate, so it 5.64 minus 5.43 by 5.64.

So, it will be almost 4 percent. But you can reduce if you introduce some amount of germanium in it. That means silicon germanium compound will reduce some of the lattice mismatch. And I can give you a value that for say silicon of 0.8 and germanium 0.2. The mismatch will be the mismatch will be less than 1 percent that means, just by introducing some amount of germanium. The material is silicon almost silicon only 2 percent is 20 percent is germanium, 80 percent is silicon, 20 percent is germanium. So, if you introduce 20 percent germanium on silicon then the mismatch becomes 1 percent from 4 percent.

So, that is the implication of silicon germanium that you can and use this silicon germanium for some applications; in and the most major application of silicon germanium is in the detectors optoelectronic detectors in the infrared region; which is required for defence application right. In the defence application you need some very good detector in the infrared region; so then in that case silicon germanium is used.

Student: (())

No, that is a theoretical substance and lattice mismatch must be 0 percent, ideally, the lattice mismatch will be 0 percent. But there are other techniques that we shall discuss during our epitaxial crystal growth those issues we shall discuss. And, other materials which are based on nanostructures; you see that this nanocrystals, quantum wires and dots and porous silicon. Now, what is quantum wires and quantum dots? What is quantum wire? What is a quantum dot? If your motion is restricted to say in the x y plane then that is known as quantum well. If you movement is restricted to say only in the z direction quantum wire. It is a wire only in 1 dimension there is a growth and in other 2 dimensions the electrons cannot move. The motion of electrons is very, very restricted in 1 dimension only it cannot move in other 2 directions.

Say in this I have I have given the example that if suddenly the walls come closer and squeeze me. So, I can jump I can go up and down; up to the ceiling if ceiling and floor is the limit then I can jump, but I cannot move to the x and y sides. So, in that case that structure is known as the quantum wire and in quantum dot.

Student: (()).

Yes, the motion is restricted in all the directions. You cannot.

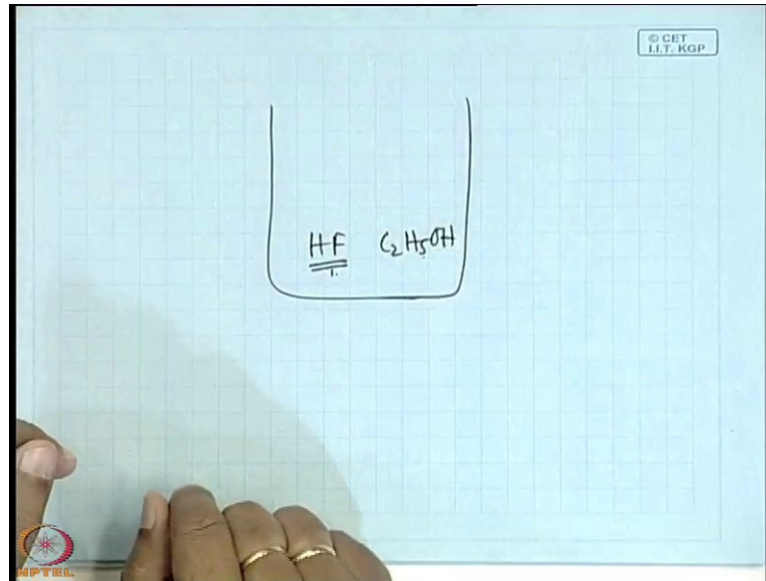
Student: Move.

Your motion is restricted in all the 3 dimensions and that is quantum dot. And, in quantum dot the advantage is that depending on the dot size depending on the dot size the energy is splitted. That I have given you the splitting of the energy levels here in this in this diagram; I have shown you that the splitting it is quantum well basically, I have drawn.

But in quantum dot also the splitting will be there. And, it will depend on inversely proportional to the square of the diameter. Here it is inversely proportional to the square of the width; there it is inversely proportional to the square of the diameter. So, if you can grow smaller and smaller the energy will be higher and higher the energy will be higher and higher. So, that is the Nano dot or quantum dot or in Nano material spherical Nano material we talk about spherical Nano material. Spherical Nano material is basically quantum dot.

And, the splitting of energy levels are there and it depends on the diameter of the dot. Another important aspect is the porous silicon and that is a technique using which you can fabricate porous silicon. You take a silicon wafer and you metalize on 1 side. Say this is a silicon wafer and you metalize say this side is fully metalized this side is fully metalized. Metalized means you can use aluminium, then you take a Teflon beaker. You know what is Teflon? Teflon is a polymeric material. You use it you take a Teflon beaker and you pour some amount of HF that means Hydrofluoric acid and ethanol C_2H_5OH .

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You take a beaker you take H F and C 2 H 5 O H. Say it is 20 percent or 40 percent H F and the rest is C 2 H 5 O H, when you put this silicon wafer inside the Teflon beaker. Now, why we have used Teflon?

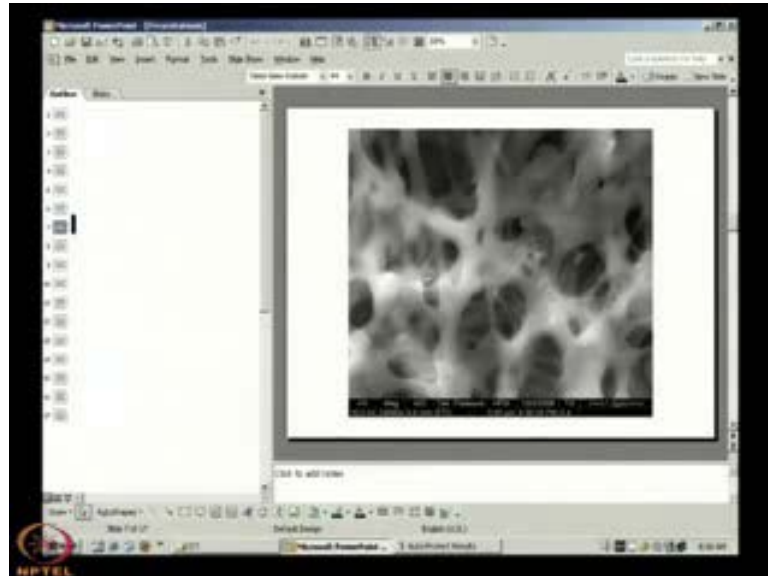
Student: (()).

Because H F is very corrosive in nature HF is very corrosion in nature. So, normal glass or other type of material it can destroy. So, that is the reason that Teflon beaker is used. And, you put the silicon wafer and you take another electrode say platinum electrode and you send a current from this is an anode. So, the silicon acts as an anode and platinum cathode between these two anode and cathode. You send current say some 20 mille ampere, 30 mille ampere, 40 milliampere. And, the electrolyte is H F and C 2 H 5 O H. Under certain circumstance you will find that the silicon surface is being etched. That means, some of the silicon is getting removed from the surface. And in that case, you will get some pores on the silicon wafer some pores in the silicon wafers.

So, the network is silicon; on the silicon there are pores. Say this is pores say the background is silicon and these are the pores and the pores dimension is in micron or Nano. Normally it is micron, but just by changing the current and this electrolyte composition you can change the dimension of the pores also. The dimension of the pores is very much dependent on the current and the electrolyte. See you can take 20 percent H

F, then you can take 40 percent H F, you can take 60 percent H F depending on that the pore size also changes the porosity differs and you will get a porous structure.

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I can show you I do not know whether this structure will be you can see no. Yes, these are the pores or the porous silicon. You see that this is the pore this is a pore and yes you see that this is pores have you seen that there are large magnification here. Yes, you can see that this is the pore this is another pore and between two pores there is this boundary. Between these two pores, there is this boundary right this is 30000 magnification S C M picture and yes these are the pores these are the pores.

Basically, there are holes on the silicon matrix. So, what happens basically in this case in porous silicon the carrier confinement occurs. That means, quantum mechanical phenomena is achieved using porous silicon because of the dimension of the pores. And, this porous silicon is used in optoelectronic application, in visible region porous silicon can be used. So, normal silicon is not used, but in porous silicon you can use this porous silicon for optoelectronic application right. So, these are the materials say silicon normally not used, but some using some techniques you can change silicon into emerging materials.

Like silicon Nano crystals, silicon Nano wires, silicon quantum dot then silicon porous silicon, silicon germanium. Now, why we are devoting so much time with silicon? Because is the material for electronic industry; till now there is no substitution for

silicon. Now, people have been trying frantically the application of silicon in optoelectronic device. So, that it can be integrated in the I C technology. Now, the in I C technology there is no scope for integration of the optical side. So, they have been trying for quite a long time right. Another important material for this elemental semiconductor is diamond. Diamond is basically, carbon it is the allotropy notification of carbon and this band gap is very high for diamond it is 5.5 electron volt wide band gap. But problem is that the processing technology is not available you can make diamond film, diamond is very hard.

So, it can be used as protective coatings in many materials; particularly for harsh environment. It is used as protective coating, because it is very transparent. You know that diamond is very transparent for a wide range of wave length and at the same time it is very hard. So, in higher harsh environment protective coating is made use in diamond. But problem is that we do not have any processing technology using which we can make diamond device, diamond device cannot make. Why? Because p n junction is required p n junction is required. Almost all wide band gap material doping is very difficult to make doping is very difficult to make 5.5 E v is very wide band gap.

So, for this wide band gap material you can see that that doping is very much difficult to make. And, for basically n type doping is not possible for diamond. P type is available, but n type is not available. So, that is one hindrance for diamond for its application in electronic device but it has other kind of device application like say protective coating, transparency etcetera you can use. Now, if you have any question you can tell me. So, till now what we have discussed basically? We has discussed silicon, some nanostructures of silicon, some new materials using silicon and some introduction about the diamond. So, these are the elemental semiconductors which are used in electronic device industry. And, in our next class immediately after this class we shall concentrate on the discussion on the compound semiconductors.