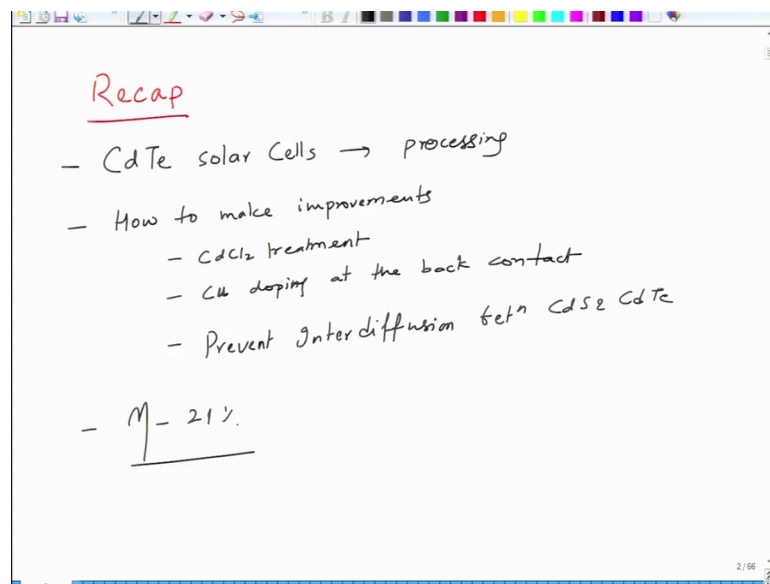


**Solar Photovoltaics: Principles, Technologies and Materials**  
**Prof. Ashish Garg**  
**Department of Materials Science & Engineering**  
**Indian Institute of Technology, Kanpur**

**Lecture - 36**  
**Generation-II Technologies: CIGS Solar Cells**

So, welcome again to the new lecture of this course Solar Photovoltaics Principles Technologies and Materials.

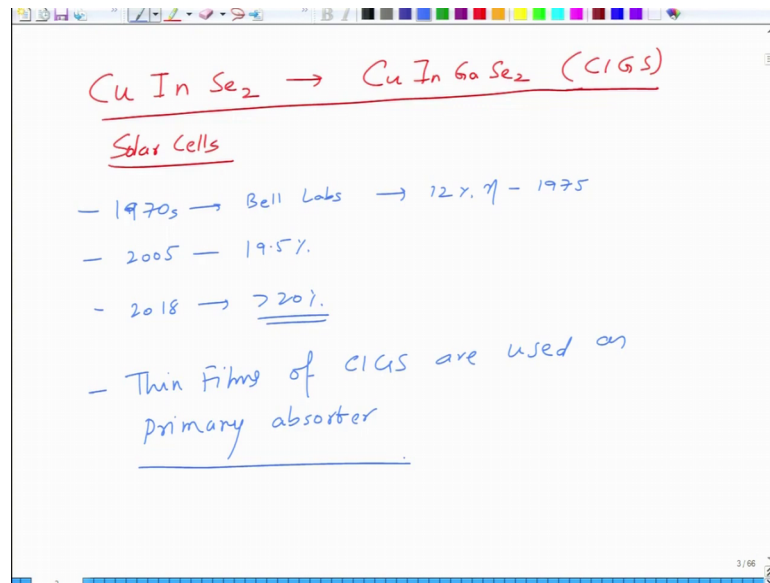
(Refer Slide Time: 00:21)



So, we will do a quick recap of last topic; in the last class we talked about CdTe solar cells; the remaining parts of processing and then how to make improvements. So, one was CdCl<sub>2</sub> treatment, copper doping at the back contact and prevent inter diffusion between CdS and CdTe. So, these are few methods which can improve process.

Then we saw the efficiency of this is about 21 percent the best efficiency is obtained. These are device level efficiency not the module level module level efficiency is go a bit lower; however, this is the very promising technology for the future.

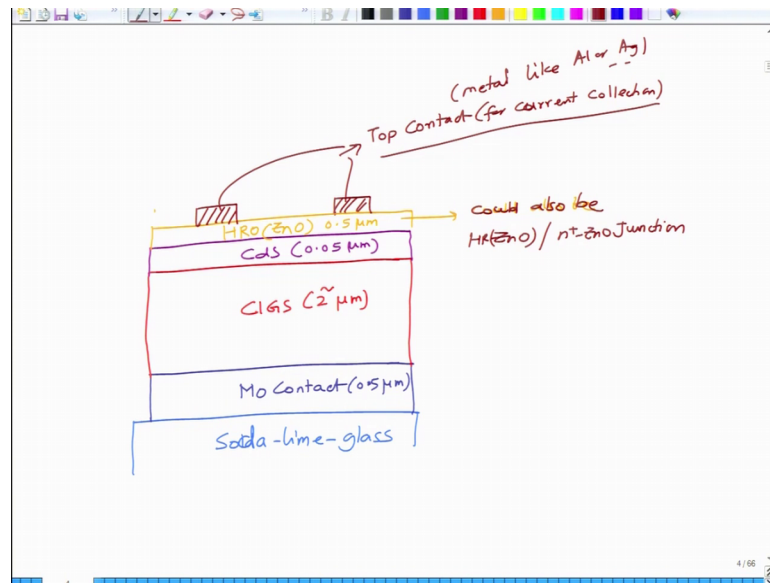
(Refer Slide Time: 01:47)



Now, we discuss another technology which is basically we can say copper; basically copper indium selenite. But it is doped with generally essentially its copper indium gallium selenite or its also called as CIGS; CIGS solar cells.

Now on this technology the work started in 1970s in Bell Labs in USA and 12 percent efficiency state away in 1975; very quickly the efficiency improvement was observed. And in 2005; we had 19.5 percent efficiency and today we stand up 20 percent in; so 2018; it is more than 20 percent efficiency in thin film solar cells. These are essentially thin film solar cells to thin films of CIGS are used as primary absorber ok.

(Refer Slide Time: 03:15)



So, the typical device structure in this is you have soda lime glass; soda it is important to choose soda lime glass not any the glass because as I will show later because in prove the performance.

And then we have molly layer on the top. So, here molybdenum is used as a contact which is about half micron tech and then we used a layer of CIS or CIGS about 2 micron ok. And then on top of it just like (Refer Time: 04:15) we use a thin layer of cadmium sulphite window layer which is about 0.05 micron or about 50 nanometers. Then again on top we use a high resistance oxide layer. So, HRO which is generally zinc oxide layer of about this is the thick half a micron or so. And so basically generally it is a junction it could also be a junction of zinc oxide and n plus zinc oxide.

So, it is possible that could also be a sorry let me use with Z n o which is high resistance then n plus Z n o junction. And then on top we have constants; top contacts you can say this for current collection which could be a metal like; it could be I think aluminum you can use aluminum on top could be a metal like aluminum or I do not know silver various other metals are possible. So, now let us see first what is this material all about.

(Refer Slide Time: 06:10)

Material Aspects

- CIGS → In/Ga → variation with large tolerance  
↓  
change in the band gap
- Grain boundaries → passive
- Cds/CIGS → Junction behaviour in terms of defects does not cause major change to the device performance
- $Cu In_{1-x} Ga_x Se_2$   $E_g = 1.01 + 0.626x - 0.167x(1-x)$  eV  
 $E_g = 1.01 + 0.626 + 0 = 1.636$  eV

CIS → 1.01 eV

So, first we look at the material aspects of CIGS; why we use CIGS is because you can vary the ratio of with large tolerance and this is basically used to tune the band gap. So, when you change the indium to gallium ratio; it leads to changes in the in the band gap. Also in CIGS grain boundary is generally these are polycrystalline since most of the times, grain boundaries are generally passive. So, as a result they do not lead to too much of damage to the device. So, you can use a smaller grain sizes because the grain boundaries do not deteriorate the performance; because of their passive nature. And generally the junction between CdTs and CIGS is very good, is does not the junction is junction behavior in terms of defects does not cause major change to the device performance.

So, these are few aspects of CIGS which are pretty advantageous, the grain boundaries are passive and junction metallurgical behavior of the junction does not affect the device performance that much. So, what is now CIGS? CIGS has a band gap. So, if you look at CIGS;  $Cu In_{1-x} Ga_x Se_2$ ; the band gap of this material is given as  $1.01 + 0.626x - 0.167x(1-x)$ . So, if your  $x$  is 0; so, CIS has a band gap of 1.01 eV this is in e V ok.

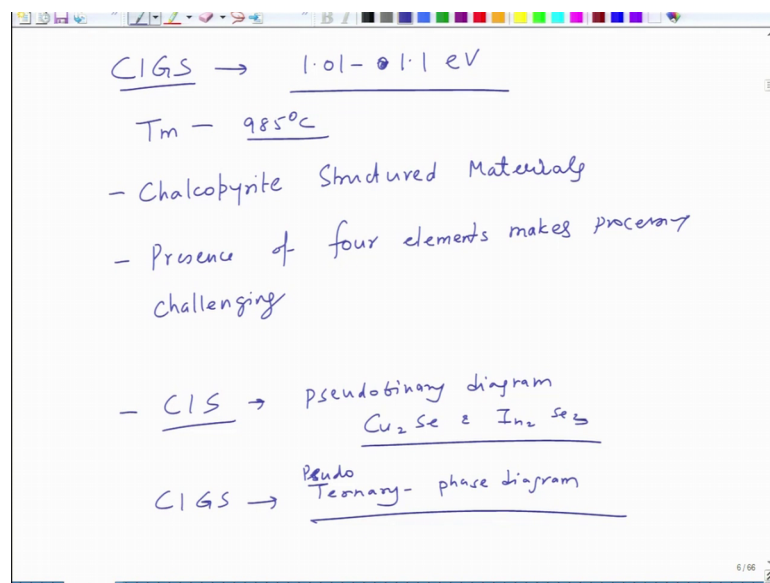
And for CIGS this band gap changes as you increase the; so you can see as you increase the value of gallium in it according to this formula the band gap will change. So, if you for instance if you take a value of let us say. So, if you take a value of for example, 0.1 if

you take gallium to be 0.1 or  $x = 0.1$ ; the band gap could be  $1.01 + 0.626x - 0.167x^2$  into  $0.1$  into  $0.9$ .

So, you will increase the band gap by doping it with. So, band gap changes significantly as you put in gallium in it. So, gallium's band gap would be  $CuGaSe_2$  band gap would be. So, if you let say put  $x$  is equal to  $0$  sorry  $x$  is equal to  $1$ ; if you put  $x$  is equal to  $1$  instead of doing this let us say we put an  $x$  is equal to  $1$ . If you put an  $x$  is equal to  $1$  then  $E_g$  would be  $1.01 + 0.626 - 0.167$ ; so this is  $1.469$  eV.

So, you can say based on this formula the band gap will change between  $1.01$  eV to  $1.47$  eV by changing the indium to gallium ratio. And we know that our band ideal band gap requirement is about  $1.4$  electron volt but you cannot keep increasing the gallium values to much because it also leads to changes in the resistivity of the material. However, we can tune the band gap by changing the different indium to gallium ratio in the material and that is why this gallium is doped in indium gallium oxide.

(Refer Slide Time: 11:01)

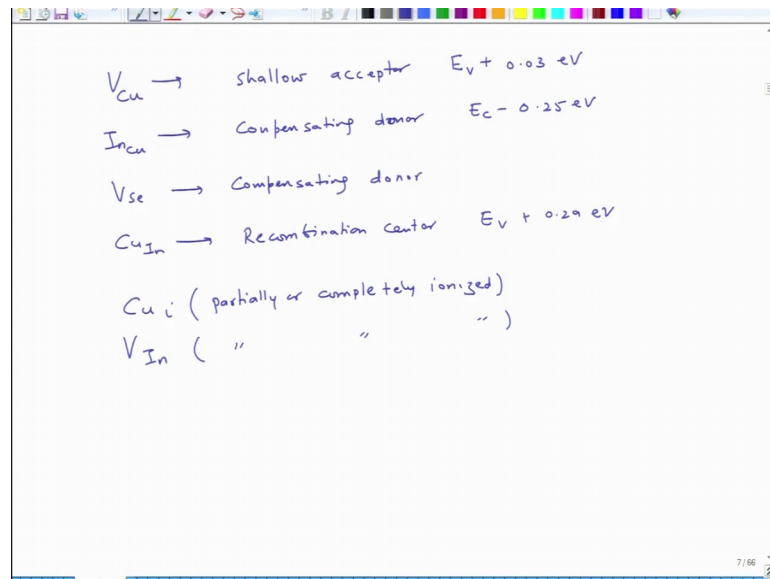


So, the band gap for; so CIGS for commercial application have a band gap between  $1.01$  to  $1.1$  eV that is what is typically used. It has a melting point of about  $985$  degree centigrade. So and basically it is some material with complex structure it is a chalcopyrite kind of material. So, it is you can say it is a chalcopyrite structured material. This belongs to the chalcopyrite category; presence of four elements make the, presence of makes processing challenging because the phase diagram is complex.

So, generally we look at a phase diagram if you look at CIS; CIS in the context of CIS we generally look at pseudo binary diagram of between  $Cu_2Se$  and  $In_2Se_3$ . But when you go to ternary phase diagram then we have; so now, we have CIGS. So, this gives rise to a pseudo ternary phase diagram and this leads to complexity in understanding the phase formation.

So, you do not have to many degrees of freedom to optimize the phases as a little bit tricky in terms of so and also since you have so many elements that defect levels also gets created quite a bit.

(Refer Slide Time: 13:05)



For example, in this case if you have vacancy of copper the vacancy of copper leads to it makes a shallow acceptor. If you have indium sitting on copper side you have it makes it is a compensating donor. If you have selenium vacancies, selenium vacancy acts as a donor compensating donor and if you have copper or indium site; this acts as a recombination center. And if you get the values here in terms of energy levels this creates energy level  $E_v$  plus nearly  $0.03 \text{ eV}$ ; it is very close to valence band.

If you look at this creates energy level  $E_c$  minus  $0.25 \text{ eV}$  this is probably (Refer Time: 14:20) similar and copper indium is about  $E_v$  plus  $0.29 \text{ eV}$ . So, these are different energy levels that one create in the one can create within the CIGS band structure by putting impurities. The various other things which are possible you can have you can have indium; so you can have copper interstitials also.

So, it is possible to have copper interstitial it is also possible to have vacancy of indium; it is also possible to have and these vacancies may also exist in partially ionized or completely ionized and as a result of that the energy levels will vary. Similarly, here it will be partially or completely ionized. So, the variety of defects which are possible in this structure as a result this composite control is little difficult in this material.

(Refer Slide Time: 15:14)

Handwritten notes on a whiteboard:

- p-type — CIGS
- Cu vacancies
- $V_{Cu}^{++} + 2h$
- $n = 10^{16} - 10^{17} \text{ cm}^{-3}$
- |         |          |                      |                  |
|---------|----------|----------------------|------------------|
| $\mu_e$ | 90 - 900 | cm <sup>2</sup> /V-s | — Single crystal |
|         | 50 - 500 | cm <sup>2</sup> /V-s | — polycrystal    |
| $\mu_h$ | 5 - 50   | cm <sup>2</sup> /V-s | — polycrystal    |
|         | 5 - 200  | cm <sup>2</sup> /V-s | — Single crystal |
- CIGS — p-type
- CdS — n-type
- } → P-N Junction

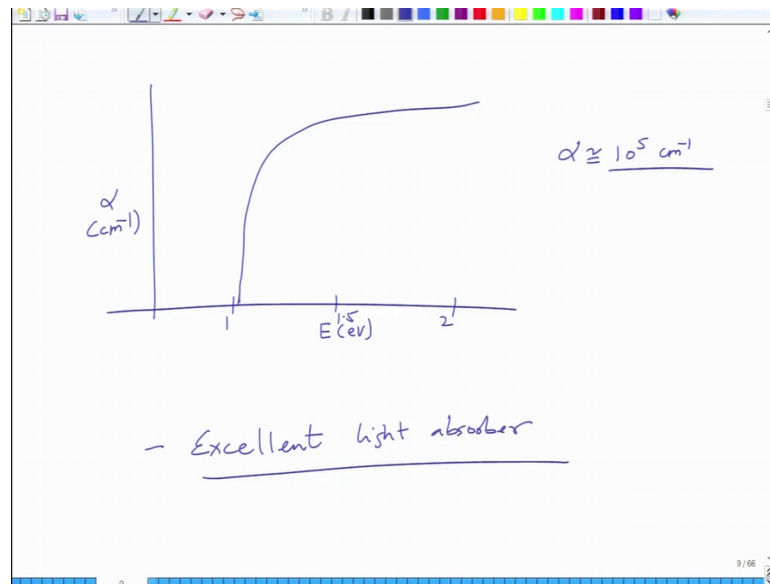
However, generally we say this material is p type in nature. So, it is generally p type CIGS and the p type behavior is achieved mainly from copper vacancies. So, copper vacancies you will have  $V_{Cu}$  which is negative in nature plus hole 2 holes ok; so this is what will give you. So, copper vacancies are the main source of p type behavior and it is generally easy to make a p type CIS than n type CIS.

The carrier density in the system are about  $10^{16}$  to  $10^{17}$  per centimeter cube. Electron mobility is about 90 to 900 centimeter square per volt second; whereas, hole mobility is about 5 to 50 centimeter square per volt second. So, this is in poly crystal; in single crystal these values would be from 5 to 200; this is also in single crystal in poly crystals these value will change to about 500 or so.

So, generally 50 to 500 in poly crystal; so these are not too bad values you know they are better than for example, if you looked at the values of polycrystalline silicon; they are better than poly crystal polycrystalline silicon values.

So, it is not a bad material in terms of electrical behavior. So, generally Cu generally we can say CIGS is generally p type material and that is why instead of making this as a n type we use CdS as n type material to make a P-N junction right. And these devices you have selenium in it the content of selenium plays a very important role in controlling the electrical properties of materials. So, when the films as we see are annealed in selenium vapors to achieve good properties.

(Refer Slide Time: 17:52)

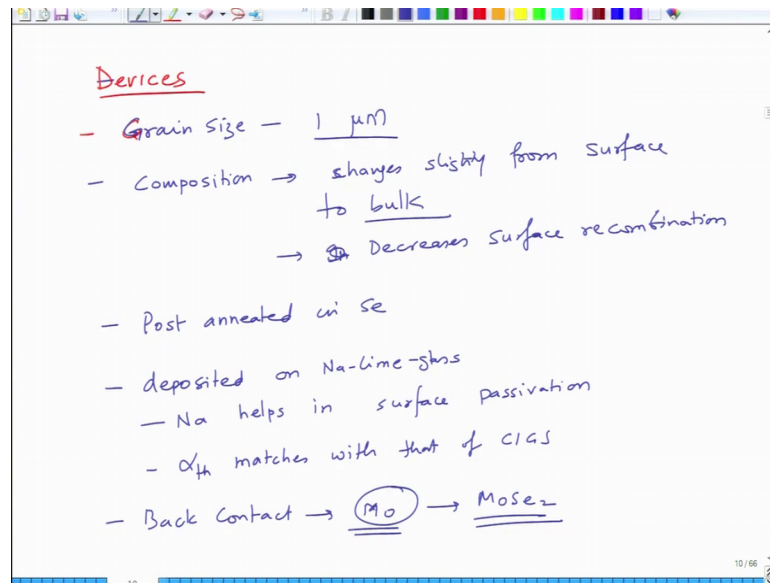


So, if you look at the absorption behavior absorption behavior of a material is very good. So, if I plot alpha as a function of energy in e V; it is around 1, 1.5, 2 it has a band gap of nearly 1 electron volt.

So, it gives you absorption which is as good as 5; so if the values reach about 10 to the power 5 centimeter inverse in the useful range. So, it is a very good absorber of light excellent light absorber. So, most of these materials are very good absorbers as against silicon.



(Refer Slide Time: 18:47)

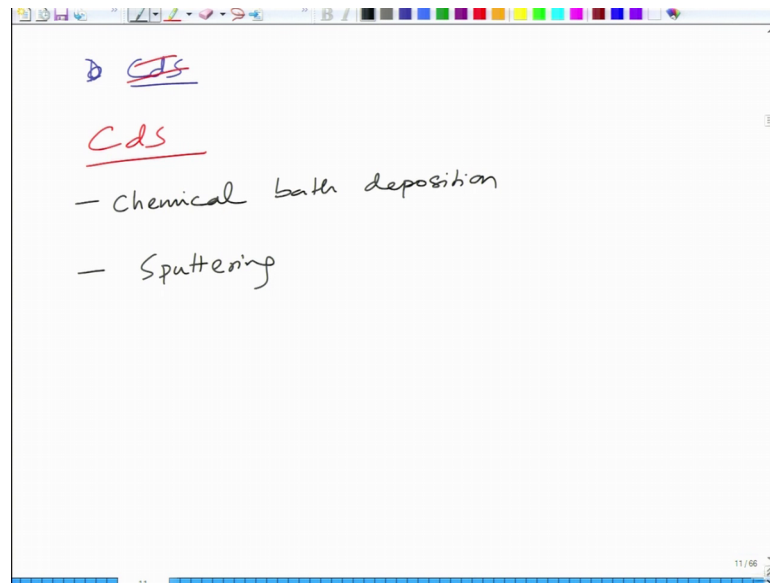


A typical devices in this case the devices have in devices; the grain size is of are of the order of about a micron, this is the typical grain size in the device that one obtains. Composition also changes slightly from surface to bulk.

So, there is a composition gradient from surface to bulk and this basically improves or decreases; you can say surface recombination. Because of some because if you have composition changes you will have energy level changes as a result the carrier velocity is not very high. And these devices are generally post annealed in selenium to control the selenium content and they are deposited on soda lime glass and this is because sodium helps in surface passivation.

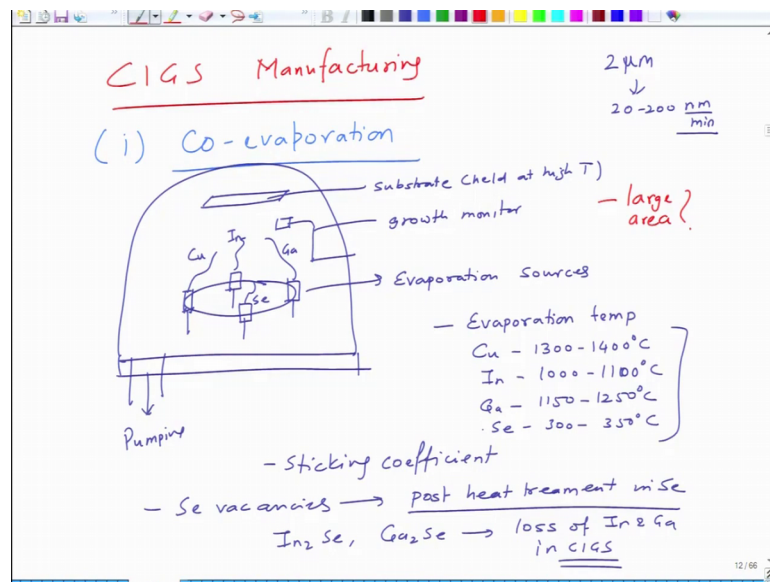
So, it controls the surface passivation by controlling the dangling bond density and it also controls the selenium vacancies and so soda lime glasses are useful in these devices. So, generally and also its coefficient thermal expansion  $\alpha_{th}$  matches with that of CIGS. So, thermal stresses in the devices are lower and you have less cracking in the thin films and the back contact as we said is molybdenum which is quite thick and molybdenum is one of the most successful materials used with CIGS. And at the back there is a formation of  $\text{MoSe}_2$ ; which prevent which suggest which; which seems to improve the addition of these device devices. So, how do you make CIGS?

(Refer Slide Time: 21:21)



Let us first look at that. So, CIGS is made by; so, C d S of course, as we said is made by chemical bath deposition or sputtering it is a very thin layer.

(Refer Slide Time: 21:46)



How do you make CIGS? CIGS is, so CIGS manufacturing the first process that we take is the co evaporation. So, what you do in this is the; you have a chamber. So, this is the chamber on you have four sources. So, one source, second source third source and fourth source they may be concentric sources basically. So, of in a concentric; so you have let me put it this way if you have this as a. So, one source will be here another source will

be here another source will be here and one source will be here there are all pointing towards the substrate.

So, these are four sources you can say evaporation sources and then we have substrate held at high temperature and as you and then you have somewhere here you can say there could be growth monitor. So, as you apply electricity to these; as you heat them they will be evaporation of. So, this would be for example copper, this would be indium, this would be gallium, this would be selenium and of course, it is connect to a pumping system.

So, you co evaporate these things together. So, evaporation temperature of for example, if you look at the evaporation temperatures copper is about 1300 to 1400 degree centigrade, indium this is in vacuum by the way right 1000 to 1100 degree centigrade, gallium would be 1150 to 1250 degree centigrade and selenium would be 300 to 350 degree centigrade.

So, they are all evaporated see when things evaporate; they get deposited on the substrate, but there is also re evaporation that may occur. So, you may have a sticking as well as you have re evaporation. So, the deposition rate will depend upon what is the sticking coefficient. There is something called as sticking coefficient which determines the ability of elements stick on a surface or deposited on a surface.

Generally, we have what happens here is the elements like selenium they are volatile elements so selenium volatile been volatile leads to selenium vacancies. So, this may require you to do a post heat treatment in selenium because selenium as high vapour pressure because of its low melting point and boiling point; as a result it tends to deplete get depleted from the devices.

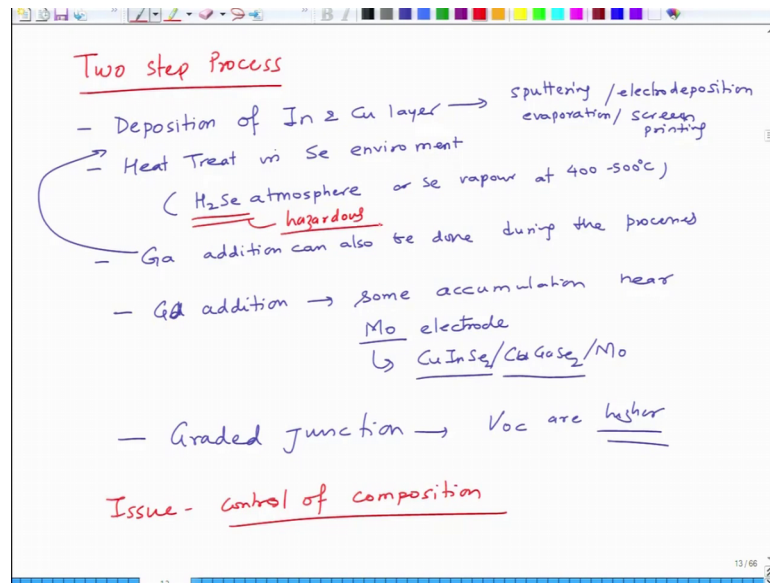
And hence it may be required to form selenium in sufficient quantities also indium and gallium may also be lost from the films. And this is mainly because indium and gallium tends to make compounds like  $\text{In}_2\text{Se}$  and  $\text{Ga}_2\text{Se}$ . So, this leads to loss of indium and gallium in CIGS.

So, instead of forming the CIGS phase they tend to form these are the phases; so phase formation is very critical in this. The good thing about this process is you can control the evaporation rate and tune the film composition and the band gap by choosing the heating

rate of each of the sources that is possible. And it is also used to make good quality devices and for a two micron film one can for a 2 micron film one can use the deposition rate from 20 to 200 nanometer per minute so it can be very fast.

But making large area devices is a problem evaporation is generally a small area process; so large area is an issue, area is an issue. So generally so, people also follow what we call as a two step process.

(Refer Slide Time: 26:40)

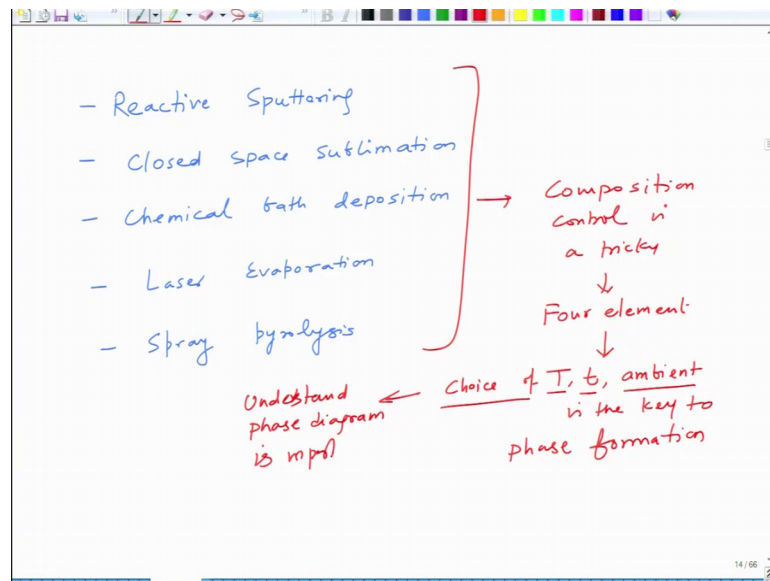


So, in this two step process first one deposits; deposition of indium and copper layers or copper indium layers followed by; then you heat treat in selenium environment ok. These deposition of these layers is done by either sputtering or electro deposition or one can do evaporation; e V evaporation for example, or even screen printing. Selenium treatment is done in a atmosphere which is hydrogen solenoid atmosphere or selenium vapor at about 400 to 500 degree centigrade.

One can also add gallium in this process and gallium. So, you can co evaporate gallium when you make indium and copper layer and then do the selanization treatment. So, gallium can go in this stage generally gallium addition leads to some accumulation near molybdenum electrode. And what forms there is generally you can form a junction which is  $\text{CuInSe}_2$  slash  $\text{CuGaSe}_2$  and this would be near Mo; so it would be like that. So, near Mo first you have  $\text{CuInSe}_2$ , then you have  $\text{CuCuGaSe}_2$ , then you have  $\text{CuInSe}_2$ .

This tends to improve the addition ok. So, this is sort of a graded junction you will make. So, first layer of C u G; S e 2, then you have a layer of C u I n S e 2; there is you can do it this way, but also you can do it together. Generally it is formed if you have a graded junction; like this then voltages are higher it is a very well standard process. The problem with this is a since you deposit these things together the control of composition is the issue. So, issue is as comparative evaporation where you can evaporate independently and control the composition evaporation rate and hence the composition.

(Refer Slide Time: 30:38)



So, here and also this H 2 S e is hazardous. There are other processes one can use which I am not going to details. So, one can use reactive sputtering just like co evaporation; you can do reactive sputtering. One can do closed space sublimation; which is a closed cousin of evaporation. Then one can do chemical bath deposition by using appropriate starting materials. You can also do laser evaporation or laser ablation and one can also make them using spray pyrolysis; just like we made CdTe thin films.

However, in all of these processes in as compared to CdTe; composition control is tricky and this is because you have four elements. So, choice of temperature time ambient is the key to phase formation. So, choice of growth temperature or heat treatment; the time and the ambient what kind of ambient you have. And this is where a knowledge of phase diagrams is very important. So, you need to understand, we do not have unfortunate time to go through details of phase diagrams, but to understand phase diagram is important.

So, we will stop here today we have done some introduction to CIGS; we will look at some more details in the next class before we switch on to the next third generation technologies.

Thank you.