Solar Photovoltaics: Principles, Technologies and Materials

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Lecture - 28
Generation-I Technologies (Mono Silicon Solar Cells)

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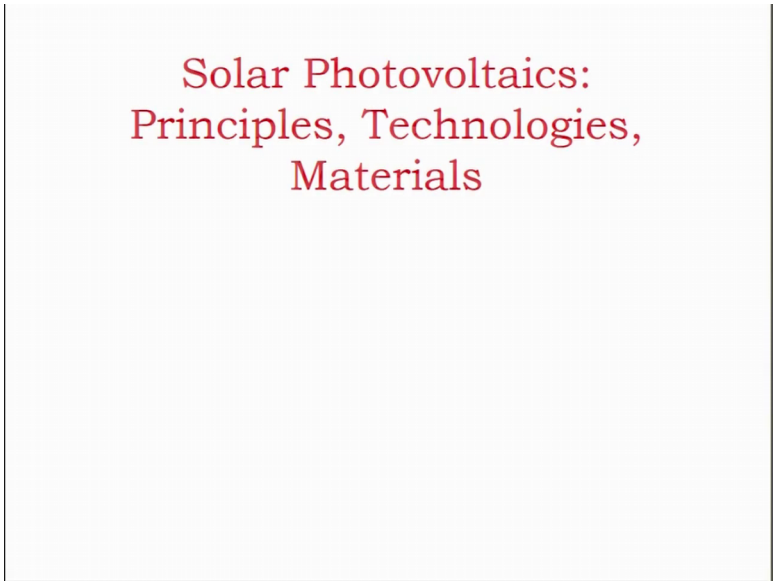

So, welcome again to the to another lecture of solar Photovoltaics Principle, Technologies and Materials.

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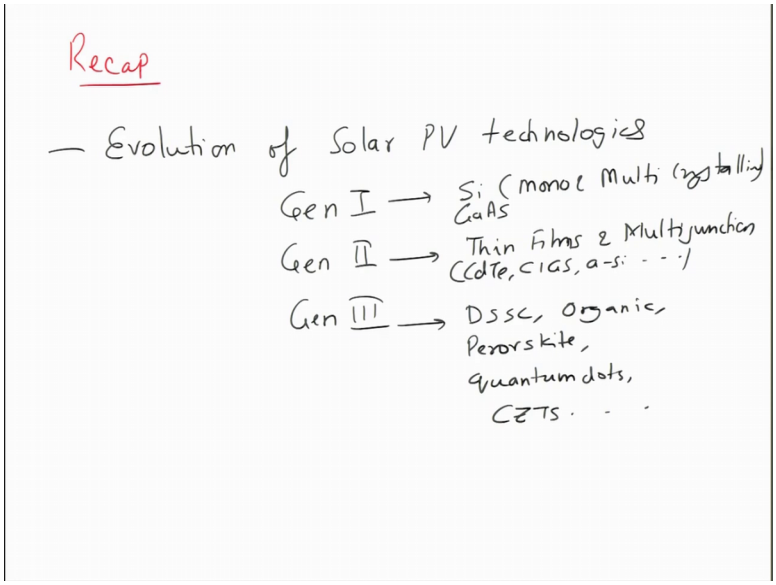

So, what we discussed in the last class is last lecture is just review that. In the last lecture we look that the evolution of solar PV technologies there are 3 so the way it goes is first we have Gen I technologies, then we have Gen II and then we have Gen III.

Gen 1 is silicon primarily based on mono and multi crystalline then we have gallium arsenide, Gen II will be thin film and multi junction thin films would be CdTe CIGS amorphous silicon and so on and so forth. Gen III will be with dye sensitized solar cells so this is called as emerging on DSSC organic perovskite there are other technologies also such as quantum dots CZTS and so on and so forth which fall under this category.

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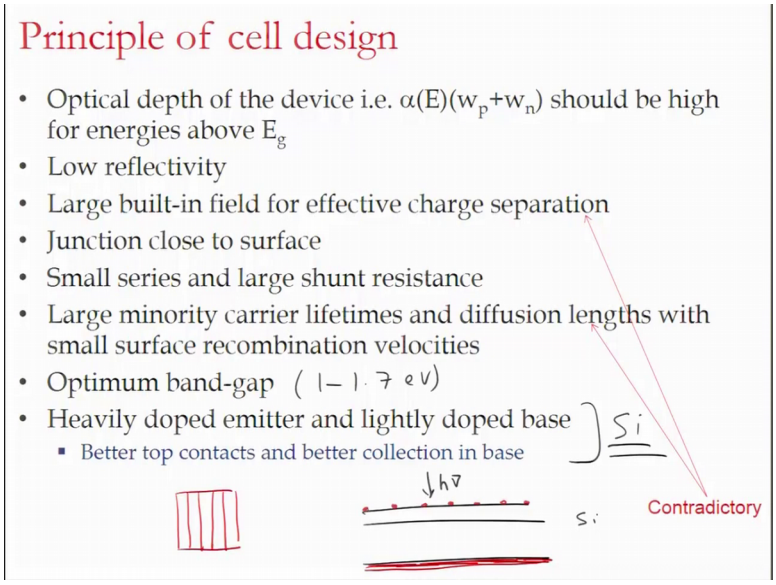

So, now let us move to so what we were doing in the last class we were looking at the principles of cell design and we said that you know optical depth should be high the reflectivity's should be low, there should be large built in field for effective charge separation junction should be closer to the surface.

There should be small series and large shunt resistance minority carriers lifetime should be larger small surface recombination velocity should be lower band gap should be optimum, so that you have maximum efficiency. So, we are looking at so but most of the materials have band gap between 1 to 1.7 e v this is the range that you have.

And then generally from the perspective of silicon especially the emitter which is the top layer is heavily doped and base is lightly doped and this helps in making better top

contacts, because remember on top you have a limitation of having maximum. So, if you have a device like this so this is silicon right silicon is a opaque material the light comes from top. So, you have to have very good contacts so that you can minimize the contact surface area on the surface otherwise most of the light will get blocked ok.

So, if you because metal is opaque right, the problem with the metals is that metals are opaque to light. So, when you are putting suppose you put a whole layer of metal on top then nothing is going to be absorbed, so what you want to instead do is that you want to minimize this coverage; you want to minimize this coverage and as a result we put in contacts which are at various places and such that you have efficient current collection.

So, that you do not cover the whole surface with metal you have only very little coverage of the surface. So, that is why if you look at the top you have these very thin lines running like this on silicon panels these are grids basically and they are arranged in such a manner, so that you have minimum surface coverage which allows maximum light penetration into the device.

On the back obviously and the back can be coated completely with metal and this will give you very good collection on the base. So, that is why silicon has certain design issues which we will see later on and these two of course are contradictory if you want if you have large built in field for effective charge separation generally that results in smaller lifetimes and diffusion lengths and these 2 generally go as contradictory we will see later on in the course.

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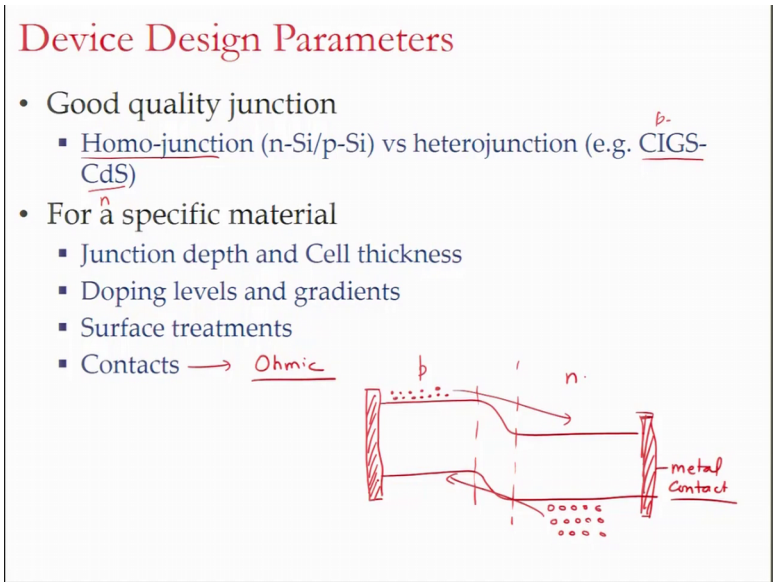

So, we have to basically optimize various parameters, so device design parameters generally you should have a good quality junction. So, in case of silicon it is n silicon and p silicon so its called as homo junction, in case of CIGS and CdS for example, the so CIGS is the p type material and this is the n type material, so there are junction is a 2 different material that is why it is called as a heterojunction. So, homo junction is the junction between the similar materials heterojunction is the junction between the 2 different materials. So, in case of only silicon we have a homo junction, whereas in many other materials whereas, in many others solar cell devices we have a heterojunction.

And for a specific material one needs to worry about what is the junction depth what is the cell thickness, what is the doping level and the gradient of doping level because doping will sometimes is not uniform there has to be gradient in the doping level specially from silicon perspective. There are some devices which requires surface treatments to remove for example certain layer. So, to introduce surface then of course, contacts what kind of contacts you are going to choose. Remember the contacts must be in this case the contacts must be ohmic so you cannot choose every material ok.

So for example, if this is the silicon device diagram this is the p n junction you have. Now you saying that you want to have a reverse current, so essentially when you are flooding the electron to so you are saying you are moving the electrons from this side for the short circuit current, the electrons are going from this side to this side right and they

get collected somewhere ok. So, the Fermi level of metal so basically you are looking at the negative current you are not looking at the positive current and here you will have holes which are created as a result of photo absorption and these are going to move here.

So, you are going to looking at the you are going to look at these electrons in such a fashion you are going to collect these electrons in such a manner, so that the Fermi level of electron does not the metal does not lie above, so this is the metal contact metal contact. So, metal has a Fermi level right the Fermi level of the metal should be aligned in such a manner, so that you have electron collection electron should not be blocked by the energy level of metals.

Similarly on this side you have another metal the Fermi level of metal should be such that the holes are not repelled they are collected by the metal. So, metal must make a ohmic contact with respect to both electrons and holes on both sides of the solar cell and that is why for a different material you will have different contact, you cannot use the same aluminium or same gold or same silver for every solar cell it will vary depending upon the type of material and that is why the choice of this material is extremely important.

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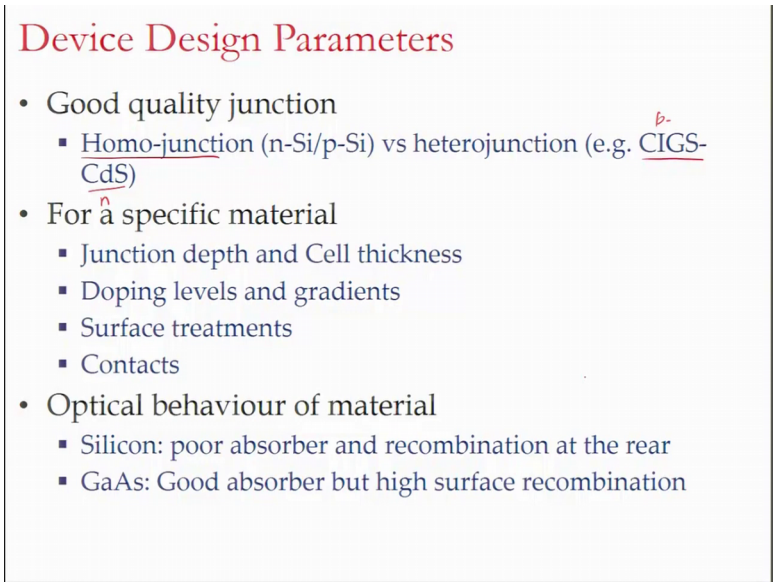

And then of course, we have this then we have this optical behaviour of materials, so you do not have much control over it. But suppose if you are; if you are; if you are using silicon has silicon is a material with it has a poor absorbing capacity because, of you

know because it is a indirect band gap material and it also tends to have recombination issues. Gallium arsenide on the other hand is a very good absorber, but it has high surface recombination ok.

So, silicon has high bulk recombination and recombination at the rear as compared to gallium arsenide gallium arsenide is good absorber because, a direct band gap material by it has high surface recombination velocities. So, there are different issues with different materials which have to be overcome by adopting device fabrication of strategies appropriately. So, let me now go to we will escape this part we will or we can I think go through this a little bit analysis of.

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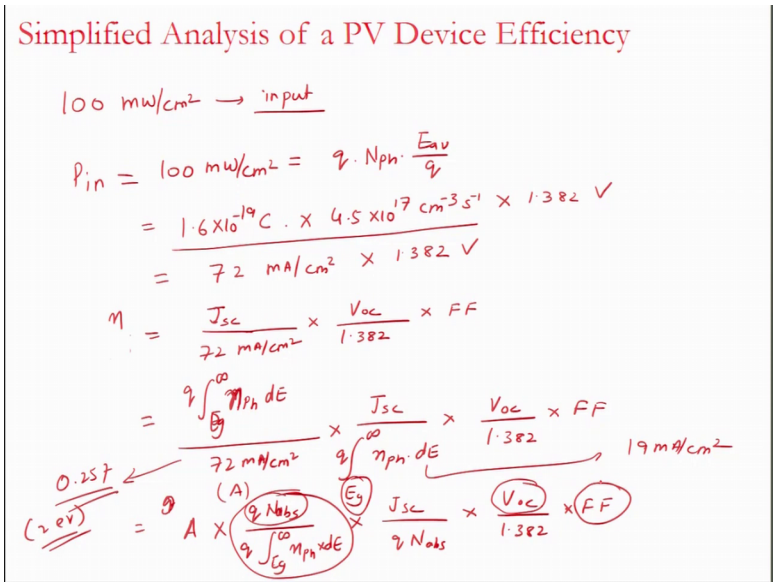

So, if you do a simplified analysis of a PV device efficiency, let us say you have a power of 100 milli watts per centimetre square this is the input. So, if P in is equal to 100 milli watts per centimetre square this can be represented as q into N photon into E average by q. So, basically 100 milli watts per centimetre square is nothing but product of number of photons into average photon energy and I have put this q in such a manner, so that I have average energy number of photons and the electronic charge.

This is essentially 1.6 into 10 to the power minus 19 coulomb multiplied by number of photons is 4.5 into 10 to the power 17 centimetre cube per second this is the photon flux and this is 1.382 volt the average energy. So, essentially this can now be equated as this can now be equated with 72 milliamps per centimeter square into 1.382 volt and so if I

write eta this is equal to Jsc divided by 72 milliamps per centimetre square multiplied by Voc divided by 1.382 both in volts multiplied by fill factor all right.

Now, this can be further broken down into I can write Jsc as q Eg to infinity n p h number of photons d E basically photon flux and since all the photons are not since not all the photons are capable of getting absorbed into the device there are some which get reflected. So, as a result we can further break this down into this term q, so this let us say this is A A multiplied by q into N absorbed divided by q into E g to infinity n p h into d E into J sc divided by q N absorbed into V oc divided by 138.

So, slowly and slowly you can see what we are doing we are doing we are dividing this simple expression Jsc Voc into fill factor into different quantum efficiency. The optical quantum efficiency the absorption quantum efficiency which clear that how many get reflected here how many get absorbed here, then finally we will break this down into. So, this factor the first factor comes to be about 0.257 for a for let us say 2 electron volt semiconductor.

And if you talk of this factor this will be approximately 19 milliamps per centimetre square for a 2 electron volt semiconductor, this factor the one we see here this depends upon the absorption how much absorption of material or how much reflection you have. So, essentially what you can do is that you can break this thing into smaller quantum efficiency terms to look at each of them every each of them microscopically. So, what basically we want to do here is if we change the band gap, for example you will increase this current if you reduce the band gap you will increase this current.

If you increase the absorption coefficient you will increase the number of absorbed photons, if you decrease the reflection then again you increase the number of absorbed photons. So, each of these terms if you increase the for example, if you change the band gap you will change the Voc also and this fill factor will depend upon the parasitic resistances that you will have in the device. So, this gives you a microscopic understanding of what you should do with the design at every stage to get higher efficiency. So, we will now move to our discussion on the technology part.

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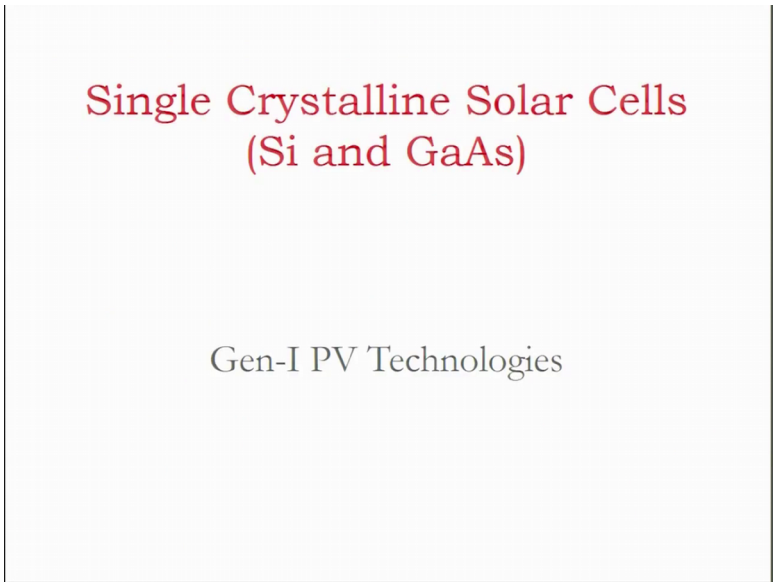

So, we will first move to single crystal solar cells we will primarily discuss silicon and we will just look at the gallium arsenide device design without getting into details of that so these are Gen I technologies.

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So, let us begin our discussion with monocrystalline silicon solar cells.

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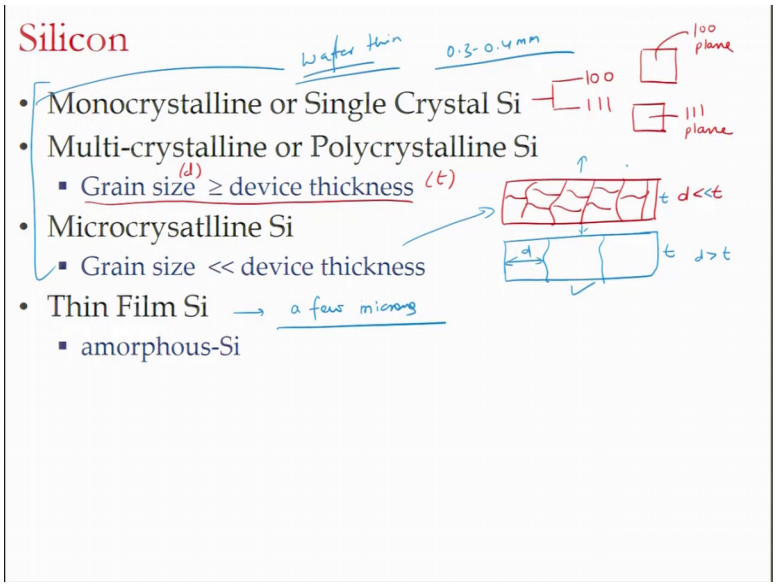

So, silicon has 2 various technologies in the silicon BV we have monocrystalline silicon solar cell monocrystalline or single crystal solar cells, which means silicon is single crystal there are no grain boundaries in the silicon it has certain orientation the wafer could be you know either 1 0 0 silicon or 1 1 1 silicon. So, which means if you look at the vapour which means if you look at the wafer the top surface is 1 0 0 plane ok, if you look at this the top surfaces 1 1 1 plane this can be distinguished by conducting x ray diffraction.

The other case could be multicrystalline or polycrystalline silicon where there are grains. So, this has no grains this has grains, the grain size however is generally bigger than the device thickness ok. So, this is a condition which minimizes the loss of current or loss of performance of polycrystalline otherwise they leave huge loss in terms of current.

So, essentially you are looking at a configuration like this, see if the grain size is smaller than the device thickness you will have this kind of configuration right these are grains. But so this is let us say grain size is d and thickness t this is d less than t, but if you have other scenario in which d is more than t then this is your grain size something like that. So, this is device thickness this is grain size d so is greater than t.

So, there so when the carriers move up and down they do not encounter too many grain boundaries, in this case when the carriers will move here and there they will find these grain boundaries which will trap the charges. Whereas, in this case since there are fewer

grain boundaries to encounter there are only vertical grain boundaries the charges do not face the grain boundaries as a result they do not get trapped.

So, this is the better design that is why grain size is larger than the device thickness in this case the grain size is smaller than the device thickness. Then there is micro crystalline silicon where grain size is smaller than the device thickness which is what is this and in fact d is much smaller and thickness and then we have thin film silicon where we generally use amorphous silicon thin film silicon's are you know the device thickness is of the order of a few microns or of the order of a micron.

Whereas, in this case the vapour in all these 3 cases it is wafer thin so the whole thing is about 0.3 to 0.4 mm thick.

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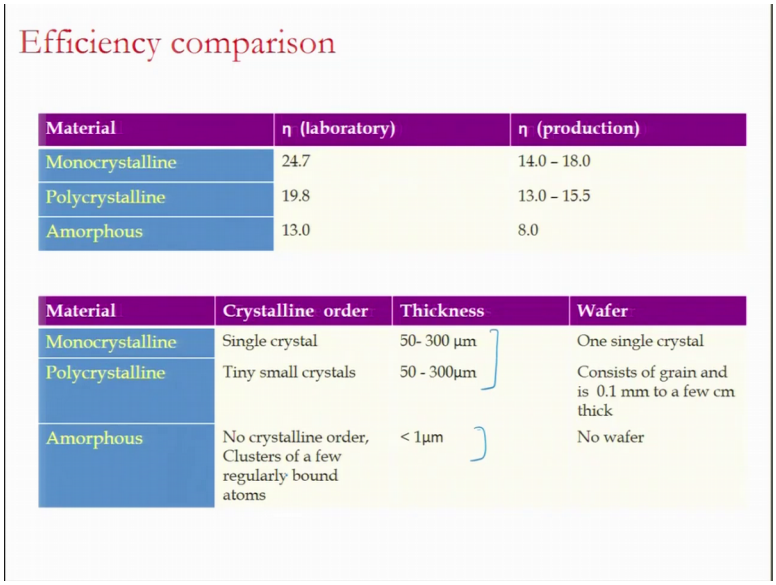

So, if you look at the numbers these are this could be updated a little bit better. So, monocrystalline for example, has efficiency of about 24.7 percent laboratory scale in the production it has efficiency of about 14 to 18 percent, polycrystalline is efficiency of 19.8 percent laboratory level which is now about 21 22 percent and production efficiency is about 15 percent as of today.

Amorphous silicon in fact it may be little higher than 15 as we speak today, amorphous silicon laboratory efficiency is about 13 percent in the production is about 8 percent. Mono crystalline silicon or poly crystalline silicon wafers have a thickness of about 300

micron which is 0.3 mm and amorphous silicon have a thickness of the order of a micron or so amorphous means there is no crystalline order basically you have atoms having short atomic arrangement having a short range order.

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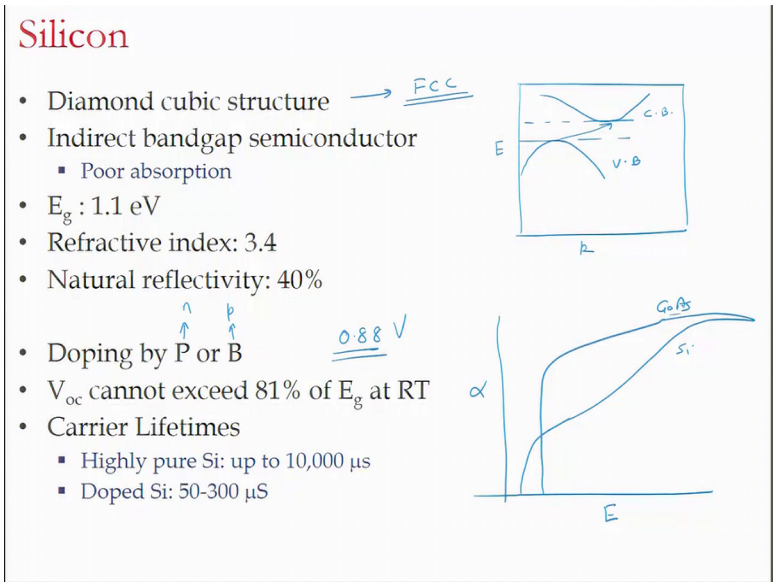

So, what is silicon in terms of material silicon has a diamond cubic structure which is basically a face centred cubic structure and so 4 silicon atoms makeup a FCC lattice and remaining 4 set atoms are tetrahedrally coordinated by other silicon atoms in such a manner, so that you have a diamond cubic structure. It is a indirect band gap semiconductor as a result it has poor absorption coefficient and so essentially what it means is that you have if you draw the E k diagram.

So, this is k this is E so basically you can say the this is your, so these 2 do not so this is conduction band minima this is valence band maxima these 2. So, the transition is like this so there is the transition in the energy space as well as in the kth space. So, hence it has poor optical absorption as we saw earlier, it has a band gap of 1.1 electron volts it has a refractive index of 3.4 natural refractive 40 percent.

So, as a result it has it is high reflective, so that the effort is to minimise the reflectivity of silicon and despite it is poor absorption can we make it work better. Silicon is generally doped by phosphorus and boron phosphorus to make it plus 5 and boron is plus 3, so this makes it and this is for n type this is for p type silicon. The Voc of the silicon thermodynamically cannot exceed 81 percent of the band gap, so as a result Voc

maximum limit of the Voc is 0.88 volt you cannot get more than that and generally it is lower than that carrier lifetimes in silicon.

In case of highly pure silicon the life carrier lifetime can be up to 10000 micro second or 10 millisecond whereas, in case of doped semiconductor when you dope introduce scattering centres as a result the lifetime reduces. So, if you as we saw last time that if you compare the absorption coefficient of silicon with respect to energy the gallium arsenide goes something like that silicon goes as a much smaller band gap. So, this is silicon this is gallium arsenide silicon has lower absorption coefficient due to virtue of it being indirect band gap semiconductor.

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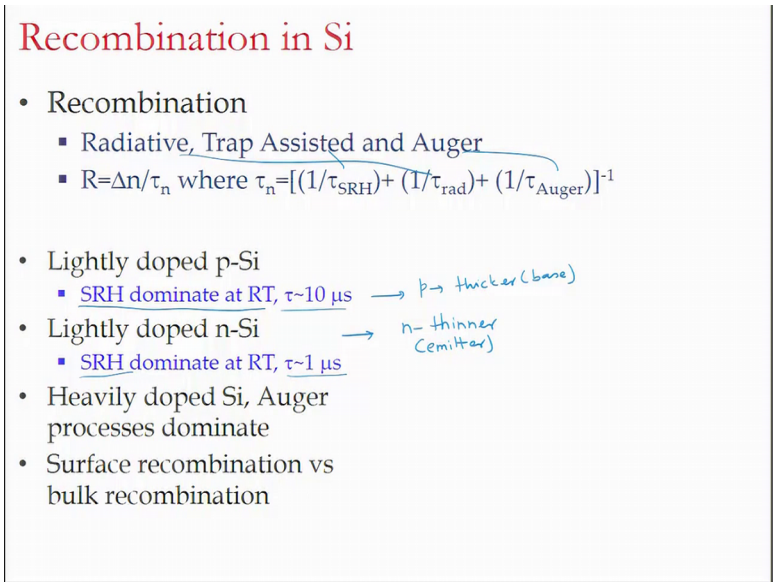

Silicon also has recombination issues and recombination is generally radiative it could be trap assisted and also it could be auger. So, generally recombination rate is given as delta n by tau n for n type careers and this is basically the average of 1 over tau plus 1 over tau rad 1 over tau shockley read hall and 1 over. So, this is radiative recombination this is shockley read hall and this is auger this we saw earlier also right.

And lightly doped silicon p silicon generally shockley read hall dominates at a room temperature and it has a lifetime of about 10 microsecond and lightly doped n silicon has a micro (Refer Time: 22:25) has a lifetime of 10 1 microsecond and again it has shockley read hall domination. So, this is why in silicon since in n silicon the lifetime is lower as

compared to p silicon the n side of the solar cell is kept thinner and the p side of the solar cell is kept thicker ok.

So, that is why n side is kept on the top and p side is kept at the bottom and silicon solar cells, so that is why n is thinner which we call as emitter and we make p as thicker which is called as base. However, if you heavily doped silicon there is a tendency for auger processes to dominate and one needs also optimize the surface recombination in comparison to the bulk recombination and silicon. So, see recombination needs to be understood well to make a device with better performance.

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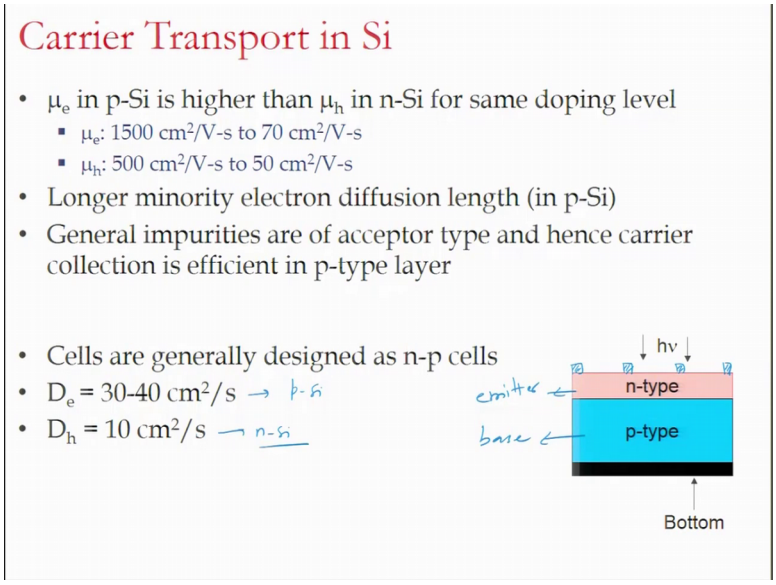

And if you look at the carrier transport in silicon has higher electron. So, as a result of lifetime the mobility of electrons in p silicon is higher as compared to holes in the n silicon for the same doping level. So, for example, electron mobility in p silicon is 1500 centimeter square volt second to roughly 70 centimetre square volt second is the range within which mobility varies, whereas in case of holes; in case of holes it is 500 to 50.

So, p silicon having higher mobility again is a reason why p side should be made thicker, so long as a result you have longer minority carrier diffusion length in p silicon that is why p silicon is made thicker. So, this is a configuration generally we have n type being made thinner and p side p type being made thicker and then since the light comes from top the top contacts have to be put in such a manner, so that they do not cover the surface they are sparsely located.

So, this is how this is a design criteria for silicon solar cell that because a diffusion lengths and lifetimes and mobility and of course the diffusivity is again you can see the same trend goes in the diffusivities also diffusivity of electron is higher as compared to hole. So, this is for p silicon and this is for n silicon that is why p type which is the base is far thicker as compared to emitter which is the top and you will put electrons and electrodes on top in such a manner, so that these electrodes do not completely cover the surface yet the electron collection is efficient ok.

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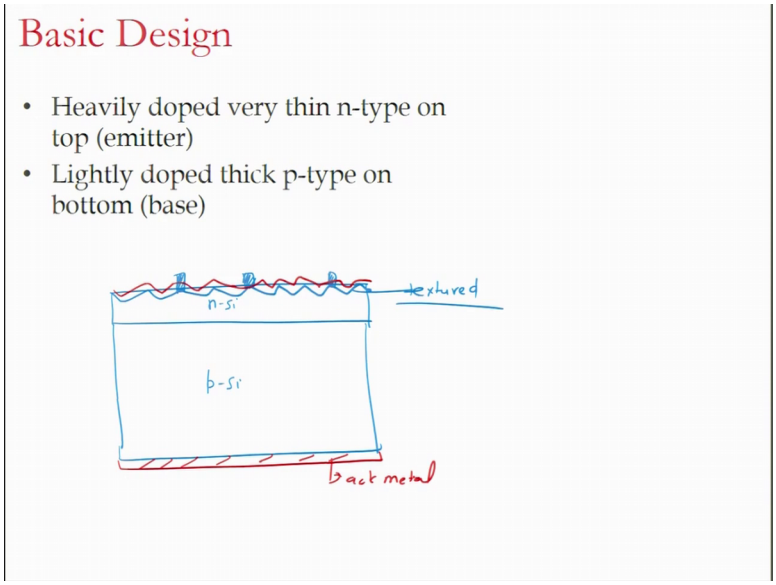

So, the basic design of a silicon solar cell will be a heavily doped very thin n type layer as top emitter and lightly doped thin thick p type layer at the bottom which is base and the so it is look it is going to look like something like this is p silicon. Then we have n silicon on top and the surface of this n silicon is little textured and this is to improve the absorption and then on top of that we have a layer of and the contacts are put somewhere like this these are contacts that put at various places. So, this is textured surface to maximize the light absorption, because you will have some internal reflection that will lead to and then on top of this we have a anti reflection coating.

So, on top of this we will have antireflection layer so this is a typical device design and on the back we will have a electrode here this is back metal this is top metal. So, we look at the more details of silicon in the next lecture. So, what we have done in this lecture is just looked at the PV technologies from the perspective of silicon what are the material

design consideration and so on and so forth. We will continue this in the next class with more discussion.

Thank you.