

Micro and Smart Systems
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Lecture - 38

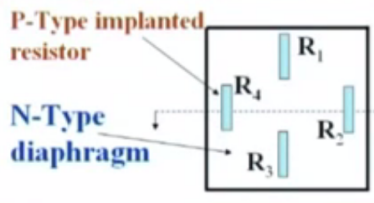
Pressure Sensor Design Concepts, Processing, and Packaging: Part -2

So last lecture we have discussed the some of the principles involved in the design of piezoresistive pressure sensors and today we will take a particular case of polycrystalline silicon called polysilicon piezoresistive pressure sensors and also will make use of an approach called SOI that is silicon on insulator approach. Now last time what we saw was single crystal piezoresistive pressure sensor that approach in a sense the membrane is made up of single crystal, a square membrane.

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Limitations of the single crystal piezoresistor approach

- **Poor isolation between resistors**
- **Temperature coefficient of resistivity**
- **Diaphragm should be n-type**



The diagram illustrates a square membrane structure. Four resistors, labeled R₁, R₂, R₃, and R₄, are positioned at the corners of the square. R₁ and R₂ are oriented parallel to the top edge, while R₃ and R₄ are oriented parallel to the bottom edge. The entire structure is labeled as an 'N-Type diaphragm'. A label 'P-Type implanted resistor' points to one of the resistors. A small inset image of a person is visible in the bottom right corner of the slide.

And the resistors are either implanted resistors or diffused resistors, they are also single crystal. So in that situation, we said that you have to locate these resistors in these positions R₁, R₂, R₃, R₄ that is in the middle of the edge of the membrane. All of them are located in the middle of the edge of membrane. 2 of them are arranged perpendicular to the edge, 2 of them are arranged parallel to the edge.

So have to achieve the maximum sensitivity we explained it last time. Now it is very good, gives good sensitivity etc. There are some problems. Will you want to use this device in harsh environment like high temperatures? As you rise the temperature what happens is if there is a

junction, junction becomes leaker and leaker. In other words, junction no longer blocks if able to block.

Here you can see you have got this resistance, which are of p-type and this membrane is n-type okay. So there is a p-n junction here and a p-n junction here and if the substrate is plus biased, this junction will be reverse biased that means the isolation between these resistors is obtained through this reverse bias junction, which will block the current flow or connection between the R1 and R3, R4 or between the 2 resistors, but at high temperature this junction will not be able to block because the leakage currents will go up.

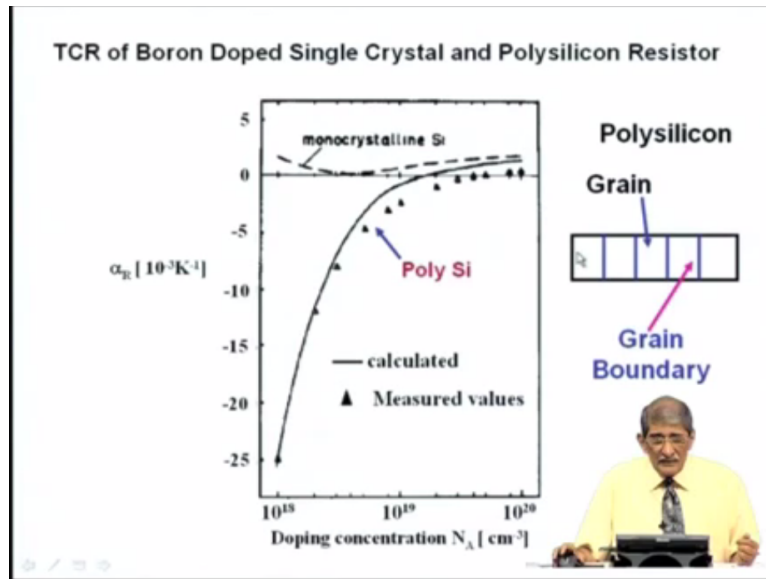
So that is the limitation of the single crystal piezoresistor approach, though it is very popularly used for higher temperature in harsh environment, which would fail. So the constraints are poor isolation between the resistors particularly when you go to high temperature. Temperature coefficient of resistivity of these resistors that is another problem, it is always positive.

So you need definitely compensation for this TCR and TCS temperature coefficient of sensitivity. This that is as a temperature goes up, you may use it in applications where temperature is varying. As the temperature varies, the sensitivity will vary, actually sensitivity should be only function of pressure not the temperature. So that is one of the drawback that this particular type of sensor has.

And there is restriction on this. If I want to use a p-type resistor, which is necessary to get better sensitivity the membrane must necessarily be n-type. So all these disadvantages can be overcome if you change the entire style that is replace these resistors with p-type or n-type whatever it is, replace these resistors instead of putting them directly on the membrane realize them on oxide.

And when you realize these resistors on oxide, you will see that that will turn out to be polycrystalline silicon.

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Now let us see what is the situation in the polycrystalline silicon? If you take polycrystalline silicon, you can see I have plotted here the temperature coefficient of resistivity alpha, monocrystalline silicon is always positive okay, quite large that is one of the problems faced in the monocrystalline silicon because of the temperature dependence of sensitivity. Now if you take polycrystalline silicon, what is polycrystalline silicon? I just put a simple diagram here.

In a single crystal silicon in cross-section of the silicon from one end to the other end, you will have one type of orientation. The crystallinity is the arrangement of atoms is same from left hand side to the right hand side, but in a polycrystalline material it is single crystalline over some region with certain orientation. You have heard about this orientation 1 0 1 1 1 etc in the previous lectures.

If this is 1 1 1, the next neighboring region will be 1 0 0 or 1 1 0 so between each of these single crystal regions there is a boundary and that boundary is called the grain boundary and each of these are called grains. So polycrystalline material will have grain boundary and grain. The grain boundary is a very highly defective region. It is not single crystalline so what happens is if the electrons or the carriers have to move from one region to the other region, it has to cross through this region, which is highly defective.

So it gives rise to a problem in the sense only those electrons, which have enough energy can go from this side to this side because it access a barrier okay. Now because of this property what happens is this polycrystalline silicon has got negative temperature coefficient of

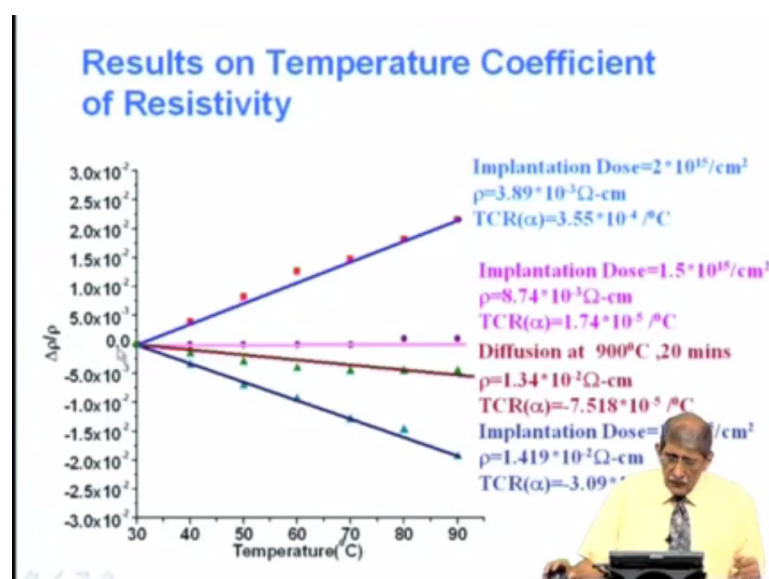
resistivity which is shown here when the doping is low. Grain behaves like the single crystalline, grain boundary behaves with a negative temperature coefficient.

Because if the temperature is raised more number of electrons will have energy to climb up this barrier here and go to the other end that means electrons can go or to get transported from one region to other region rather easily that will tell you that current flow is easy that means the resistance is less that means temperature coefficient of resistance is negative that is the meaning of that okay.

Now how much is the temperature coefficient of resistance that is negative depends upon how much is the barrier is. If I keep on adding some dopings more and more it is not getting into the mechanism of that. The barrier between these 2 layers gets reduced okay. So if the barrier becomes 0 that will affect the single crystal but we do not want that. There will be some barrier, which will give the negative temperature coefficient, which is compensated by the positive temperature coefficient of the grain.

So you can see if you keep on increasing the doping, the temperature coefficient of resistivity will keep on becoming less and less negative and it will approach 0, which would mean that I can adjust the doping in this grain and grain boundary and get a TCR that is temperature coefficient of resistivity practically 0 or negligible that is what you are looking for in polycrystalline, that is the main advantage of using polycrystalline material. So instead of single crystalline resistor use polycrystalline silicon.

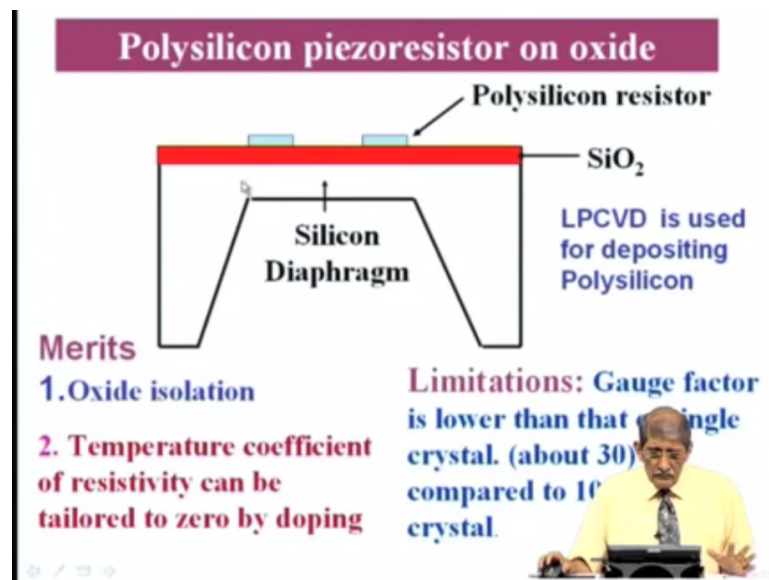
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So this is one of the experiments such that we carried out one for some of our students. This represents this plot at a particular doping level okay. Temperature on x axis $\Delta \rho$ by ρ , if the doping is low of the order of 10^{17} or 10^{18} , TCR is negative, crystal falls. As we increase the doping, you can see the slope becomes less negative and at a particular doping of about 5×10^{19} per centimeter cubed the curve is flat.

In the sense as you vary the temperature from 30 degrees to 90 degrees centigrade, the ρ or the resistivity practically does not change. That is the meaning of that, but you can see if I go to still higher doping its behavior is almost like that of single crystal during positive temperature coefficient that is not what you want so you have to adjust the doping okay that doping level is about 5 times 10^{19} per centimeter cube okay.

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Now let us see so the way you do this polycrystalline the resistor is like this. Take a silicon substrate, use bulk micromachining technique to etch the silicon from here, this is a cross section so that you get a membrane whose thickness is decided by your etching, 10 micron or 15 micron will be the thickness of this membrane and the dimension is also decided as we discussed yesterday by the pressure range that you want to use it okay.

Now I grow oxide on that and on the oxide you realize polysilicon resistor. I have shown 2 of them, there will be 4 actually so I have shown 2 so these 2 resistors are there. You can see there is no connection between this resistor and this resistor unless you make a deliberate condition outside. So if I take this resistor between these 2 that is oxide so the resistivity between these 2 layers is 10^{14} ohm centimeter, which is insulating layer.

So you get oxide isolation between the 2 resistors, which will stay in isolation even if you go to temperature like 500 to 600 degree centigrade. So you can use this type of resistors in the form of a bridge and make use of this for realizing pressure sensor, which can operate temperatures like 300 to 500 degree centigrade very comfortably okay. As you have seen, you get oxide resolution here, temperature coefficient of resistivity can be tailored to 0 by adjusting the doping just now we have seen okay.

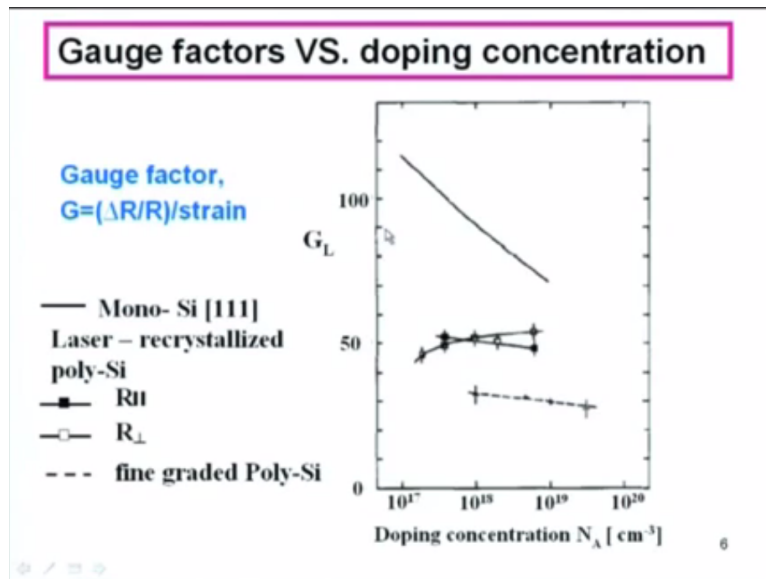
Now but you cannot get everything free, you have to pay for these benefits by something that in limitations is that gauge factor is lower than that of single crystal. Gauge factor means $\Delta R/R$ changing resistance to the original resistance divided by strain. In single crystal, you may get about 100 to 200 gauge factor whereas in the polycrystalline silicon it will be something like about 30.

So gauge factor will be low, it will be low meaning implication is the sensitivity of this device will be lower than that what you get with the single crystal silicon, it does not matter today because if the sensitivity is low (()) (12:09) low for a given pressure but you can use an electronics to amplify the signal that is not of issue okay. Now this polysilicon is deposited by a technique known as low pressure chemical vapour deposition.

What is done is into a heated furnace you pass silane SiH_4 , silane gas, it will decompose into silicon and hydrogen and silicon will be deposited on this oxide. That will turn out to be polycrystalline. This deposit is done at about 620 degree centigrade okay. So you need 4 resistors to be what you do is deposit polysilicon everywhere, pat on them, dope them, you get the resistors.

We will go through that steps now before that let us see few more things. We said that the gauge factor is lower than that of single crystal that is detected by this graph.

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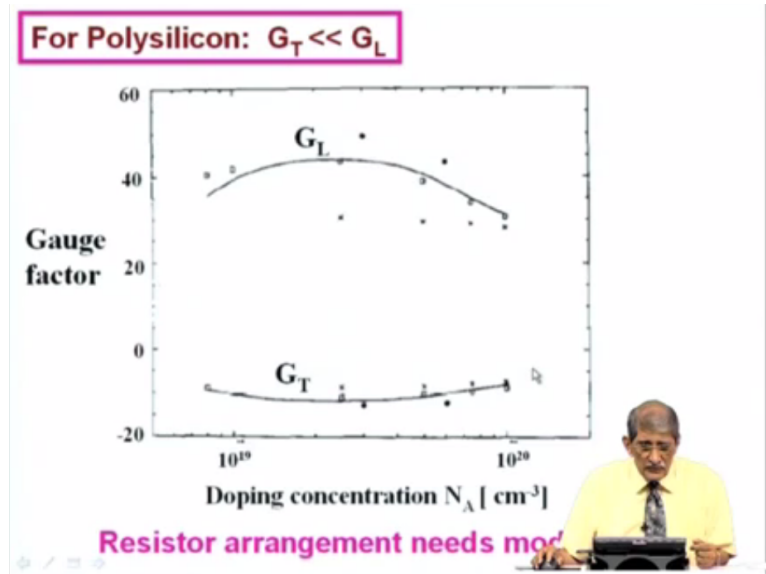


The longitudinal gauge factor means actually if I take a resistor like that okay if I have a resistor like this current flows like that the resistance in this direction is a longitudinal resistance okay. Now longitudinal gauge factor means change in the resistance divided by the resistance when the stress is in that direction that is a longitudinal gauge factor. That varies from something like about 200 to 80 to 70 as we increase the doping in the case of single crystal resistor.

In the case of polycrystalline silicon, you can see it is about 30 so most constant that is added benefit. You can go to higher doping it will remain almost 30, single crystal you can see as we increase the doping the center reel automatically fall okay. Now you take polycrystalline material subject it to laser really that is heating with laser. Then the grain size will become bigger, the gauge factor goes up.

If the grain size becomes infinite, it is single crystal. So larger the grain size better the gauge factor that is what is implied by this, but you are sticking down to this polycrystalline material as deposited whose grain size will be something like 0.1 to 0.3 micrometers size though there will be number of grains on the surface gauge factor is low as I mentioned nothing to worry about that.

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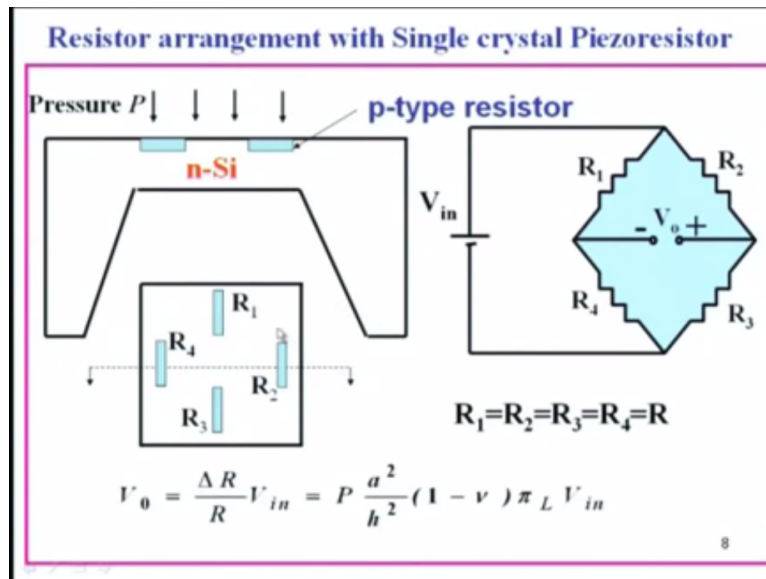


The other thing that you have to take care is the gauge factor longitudinal and transverse. They are different in case of polycrystalline material. In case of single crystal, we said the longitudinal gauge factor along the 1 1 0 direction it may be 100 and in the transverse direction or perpendicular direction, it will be -100 which would mean that if I have one resistor which is getting pulled along the length of the direction.

It will have a gauge factor of 100 that is $\Delta R/R$ divided by strain will be +100, but if you pulled in the transverse direction in the case of single crystal that will be -100 that is the resistor will fall down it will be $-\Delta R/R$ divided by strain will be 100 okay. So in this direction it will increase by factor x let us say, in the other direction it will fall by the same factor ΔR in the plus direction and minus direction will be the same thing.

We discussed this. You put them in the opposite arms of the bridge. Now in the case of polycrystalline material, the gauge factor will be high maybe about 30 to 40 in the longitudinal direction, in the transverse direction it is something like -10 on an average about 10.

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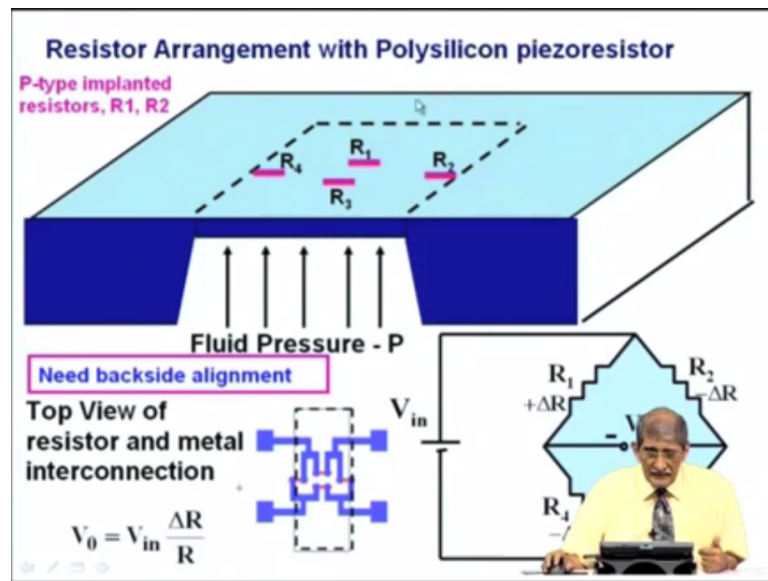
So you cannot use the resistance arrangement that is used in single crystal. See in single crystal what you have done is this is the membrane, this resistor is p-type, you have arranged them perpendicular here, they will experience longitudinal strain and these 2 you arranged parallel to the edge, they will experience transverse stress so delta R positive and delta R negative will be almost same.

And you will get very good sensitivity because R1 and R3 will go up, R2 and R4 will go down, you will get plus there minus there. So you get an output of delta R/R divided by input voltage= V_0 that is what you have put here. Now this arrangement have to modified because you if you arrange like this, R1 and R3 will go up if it is polycrystalline material because longitudinal gauge factor is good at least 30 to 40.

But the change in this resistance in R2 and R4 will be very small because gauge factor is small. So you cannot arrange them like that, but what you see here is it is longitudinal tensile stress. If I arrange resistor at that it experiences longitudinal compressive stress then you are in business. What it means this (()) (17:57) is longitudinal gauge factor is good, does not matter whether it is tensile or compressive okay.

So one of the key thing to do here would be arrange the 2 resistors where at least it will be subjected to tensile stress longitudinal, arrange other 2 resistors in locations where it is longitudinal stress, but compressive. So that is what is done in the case of polycrystalline. The arrangement is modified. So you can see instead of arranging it like this on a membrane, the polycrystalline silicon resistors are arranged in this fashion.

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This is the membrane I have shown only one portion of membrane. These 2 resistors R₂ and R₄ are perpendicular to the edge that means they will be stretched along the direction longitudinally, longitudinal tensile stress will be experienced by R₂ and R₄. That gauge factor is about between 30 and 40 or 30 on an average you can say. Now R₁ and R₃ is at the middle of the membrane.

If you remember if I analyze the stress at the center of the membrane along this direction, it will be tensile here, it will be tensile here, but when you go down into the membrane it will become less tensile 0 towards the center and it will become compressive okay. That means if I locate a resistor or If I lay out a resistors at the center of the membrane in this fashion that will be compressed in that direction.

And that is compressed along the length of this resistor that is compressive stress so if I take a resistor okay and if I compress it like that, L will fall area will increase okay. So resistance will fall. So compressive tensile stress for p-type material the resistance will fall and tensile stress the resistance will increase. So you have located the piezos to polysilicon piezoresistor in the region said that R₂ and R₄ experience longitudinal tensile stress, gauge factor is about 30 let us say.

And R₁ and R₃ experience longitudinal stress, but compress you gauge factor is -30. So these R₂ and R₄ will go up, R₁ and R₃ will go down by almost same factor. So that sorts out the problem of the poor sensitivity of the polycrystalline material if you arrange it in this fashion

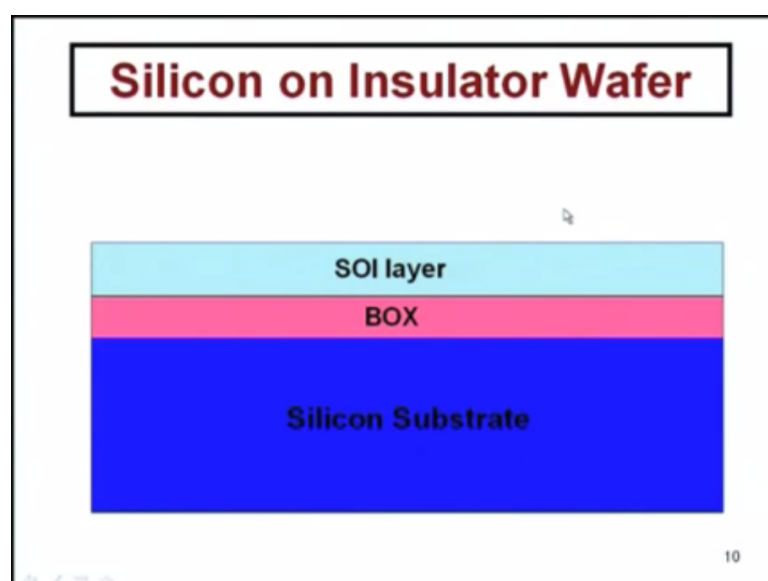
so modify this. Now these 4 resistors you can see they are arranged here this red color what you see in the bottom here dotted line is the membrane okay and the blue color that you see is the interconnecting metal lead out on the surface of this wafer okay.

So these resistors are joined together here by means of metal on the surface of the wafer and then taken to a pad to which wire can be bonded when for packaging the device. So these 2 are joined together and taken to the pad you can see here, R1 and R4 okay. They are joined together here and I am not showing the pad here, they are joined here, taken out of the membrane to the pad.

So pad is provided somewhere outside the membrane because on to the pad you will bond the wire. If the pad is on the membrane if I am bonding the wire on to that, it will puncture the membrane because it is after all about 10 micron thickness. Here it is very thick maybe 300 micron or 200 micron thickness here. So pads are located outside the membrane okay. So 4 pads are there because here it is joined, here it is joined so 2 pads are used for the power supply, other 2 pads are used for the output.

So since ΔR positive and ΔR negative are same in magnitude you will get when the bridge on which as we have discussed yesterday in our last lecture $V_{naught} = V_{in} \cdot \Delta R/R$ okay. So of course you need to have backside alignment as we discussed in the previous lecture that is done by IR mask aligner or backside alignment system. So that you locate, realize these resistors exactly where the membrane is present okay.

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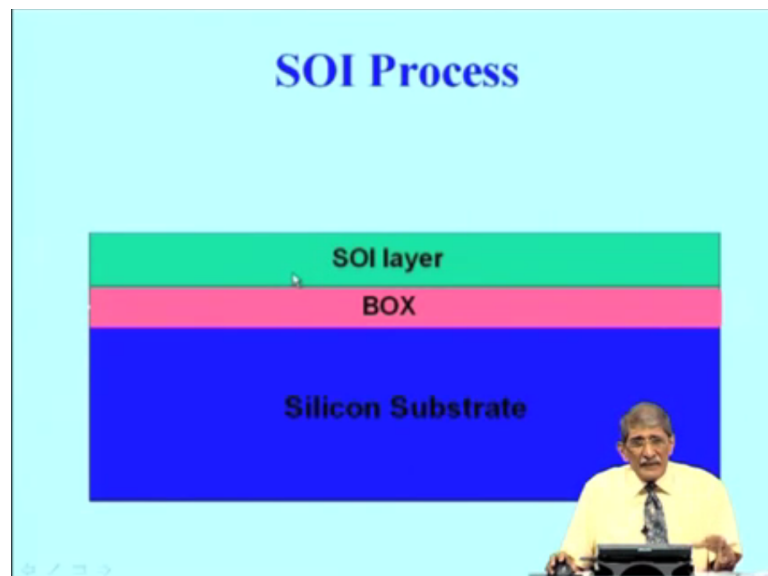


Now let me go through this approach. So all that you need is to have a silicon membrane on that top of that have oxide, on the top of that realize these resistors okay. Now we will go into one more additional input that is silicon on insulator approach. Silicon on insulator is used today in integrated circuits. IBM has used it in main stream for making the VLSI. So in many companies they are trying using this because it has several advantages for making very large scale integrated circuits.

Because devices can be operated at higher temperatures, higher packing density is possible. I am not getting down into discussion on this but that is not relevant, but if you can make your sensor also on a silicon on insulator wafer there is chance for you to integrate the sensor with the electronics on the same chip that is our target that is why we will see how this SOI is made, how the piezoresistor is made on the soil and how the integration can be done that is the topic that we are going to complete today that is the case study.

So here silicon on insulator that is SOI it is said because it is on an insulator. So here you have got 3 layers, silicon substrate, BOX buried oxide, it looks as if this oxide is buried below this silicon layer okay. So that is why it is called BOX buried oxide SOI layer. How to make this? Very simple and quickly go through an animation the process for that.

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This can be done in laboratories scale both at IIT Madras and Indian Institute of Science. Our students have done this sort of SOI and fabricated devices on this. Take one wafer, oxidize a wafer okay the process to make the SOI layer. Take another wafer, oxidize it and bring them closer together, see this top silicon, bottom silicon both of them are oxide grown on them, put

them together and apply a pressure maybe 1 atmosphere pressure or more. You can see this gap between them very close bonding, they merge together okay.

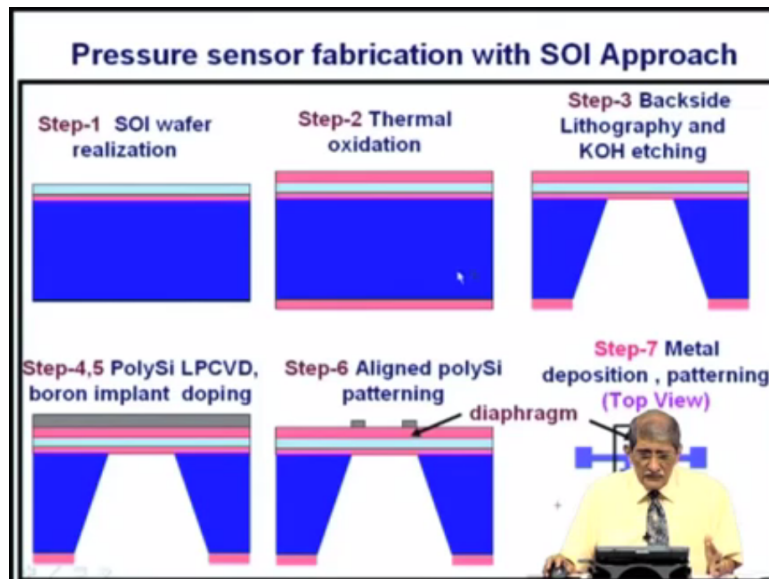
The technique is initially when you bring them together, the initial bonding takes place because of some OH which is present on the surface, you have to give some chemical treatment so that the surface becomes hydrophilic that means water loving, hydrophobic is water hating, so make it hydrophilic by making some chemical treatment. There will be OH molecules and when you bring them together the initial bonding pre-bonding will be between silicon OH OH silicon.

Then you take it to high temperature okay that from the OH, the hydrogen comes out and you have silicon oxygen oxygen silicon that is SiO₂ bond, you will have the bonding through the SiO₂ itself okay that is the 2 wafers are bonded. Now what you do is I want this top layer to be very thin actually this rotating backside, etch it down, please note very carefully that portion etched deep from here that is the etch back, bonded and etched back we call it as (()) (26:56) okay, bonded and etch back SOI silicon insulator.

So you have got now silicon on layer oxide, 2 wafers bonded together, top layer reduced to required thickness. Why do you reduce it to the required thickness? You need for integrated to make integrated circuits a thin layer there. Also I can use this for realizing a membrane for making pressure sensor and membrane thickness will be decided by how much will be the SOI layer thickness.

So if you want 10 micron thick membrane, I will have to reduce this layer to 10 microns so originally that must have been 200 micron I let it down reduce it to 110 micron okay. So you can use this layer to realize the pressure sensor and also electronics.

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Let us go through further. How the pressure sensor is made on this? So starting with you have made this SOI, starting wafer is the silicon on insulator wafer that is realized, silicon buried oxide red color there is SOI layer. Grow oxide on the top of that because you are going to put resistors on oxide. So on this SOI layer, grow oxide and then do lithography from the backside, open this oxide subject it to etching, so etch it all the way down, this oxide thickness will be just about 0.5 microns.

So this membrane 10 micron, 15 micron depending upon what you want for the membrane. The advantage of this is KOH etching will etch the silicon anisotropically, but etch rate of oxide is very small. So when it reaches this oxide, the etching automatically stopped. So we got a membrane here whose thickness is that of the starting SOI layer thickness that is the merit, automatically we get a 10 micron thickness if I had a 10 micron thick SOI layer.

So now this SOI layer you grow oxide on the top of that, it is already there, use this layer now to realize, your membrane is realized. Right now, I am showing only how to realize sensor here. On this oxide, deposit polycrystalline silicon by low pressure chemical vapour deposition in the sense in a furnace where the pressure is something like 200 millitorr, you pass silane, keep the furnace at temperature of 620 degree centigrade, the silane decomposes into silicon and hydrogen, that silicon gets deposited on this oxide and that is polycrystalline okay.

Now you pattern this polysilicon by means of lithography. Remember you want to remove the polysilicon from everywhere except in the 4 red color region here if this is a membrane

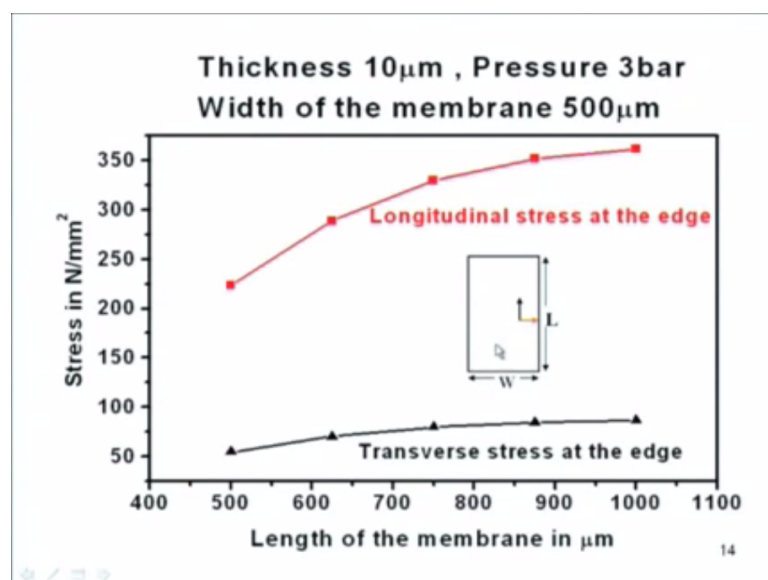
look here at the top view this is the region where you want to retain that. I have shown the cross section here so I have shown the 2 here therefore in the cross section you will see only 2 okay. Before patterning you need to introduce boron dope end which is p-type.

You introduce dope ends to resistant that it brings the temperature coefficient of resistance to 0 that is about 5×10 to the power of 19. This doping is done by diffusion or implantation, the temperature and time of diffusion will decide that doping concentration and implantation, number of dope ends which you have implanted will decide the number of dope ends okay per centimeter cube.

So once you get that doped by lithography aligned with respect to the bottom membrane, realize this resistor and once you do that next step is deposit metal all over, pattern the metal to remove the metal from all regions except in this portion in the sense you have these resistors connected together and pads are all provided. With that your device is ready on the wafer level.

Remember I have shown only one device, but in the full wafer there will be 100s of such devices side by side, this is repeated this whatever I am showing here is repeated from all over the wafer in the x and y direction okay. You have to separate them out afterwards by dicing. Will see that litter later. So this is the piezoresistive pressure sensor which is complete.

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Now the ANSYS simulation so the other thing is in the previous years we were showing square type membrane here we have switched over to the rectangular type of membrane. We have done this because if I make this membrane rectangular instead of square, the stress along this longitudinal direction becomes more if the length of the membrane is more than a width.

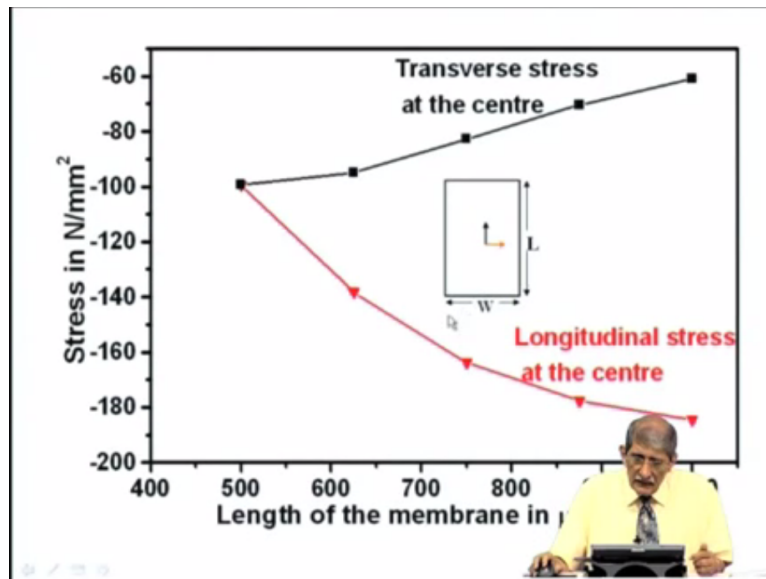
Both tensile stress at the edges and compressive stress in the middle both of them increase for a given pressure. So what you want is for a given pressure the stress on this resistors will be more. So you choose this membrane to be rectangular type. For example, this is the simulation using software called ANSYS for mechanical engineers, they use that software. There are other softwares like counterware.

W is the width let us say 500 micron and membrane is 10 micron thickness and pressure 3 bar, if the width is equal to length 500 microns, the stress at the edge here longitudinal stress is about 50 newton per millimeter square, which is about 500 bar okay the transverse stress in that direction, but the longitudinal stress is about 2200 bar 220 newton per millimeter square is 2200 bar.

Now if I increase that width to L if I increase the L and make it double that width is 500 micron and length is 1000 microns, the stress at this edge longitudinal stress which was originally 225 becomes almost which is more than 350. So this stress is more that is strain on the resistors will be more that means for the given gauge factor $\Delta R/R$ will be more that is sensitivity will be more.

So the transverse stress is not increasing much we are not going to use that since length is increased you will have the stress and the sensitivity will be better.

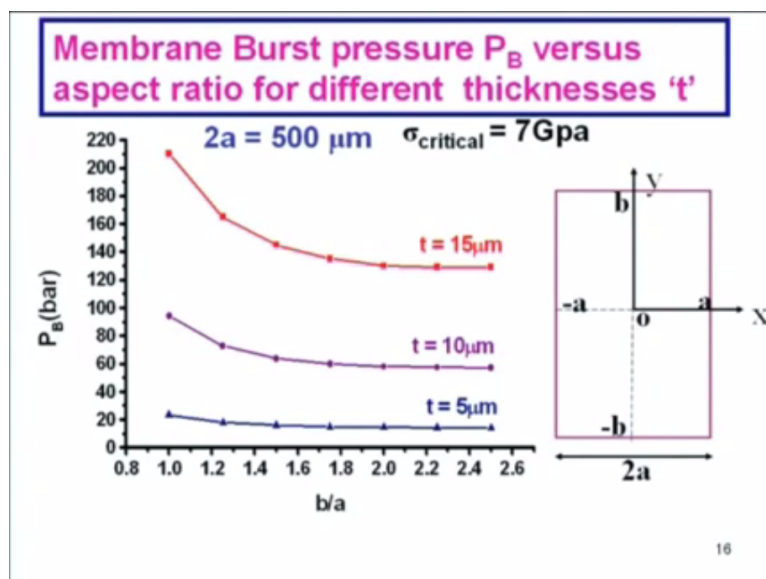
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Similarly, if I take the resistor at a center, there the stress is compressive so I have shown it as a negative value as we increase the length from 500 to 1000 the transverse stress goes up from -100 to about close to 200. So if the aspect ratio L/W is 2, it is almost the factor of 2 the stress here compressive stress.

Now this resistor it is also longitudinal compressive stress, but stress in the transverse direction we are not looking at that actually becomes less which is good because if there is a stress in transverse direction, that will actually reduce the effect of the longitudinal stress okay.

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So with this in the use of the guideline that you have a rectangular membrane rather than a square membrane so that the stress in the resistors along this direction is more both at the

edge and at the center okay. Now let us see what will be the impact of that on the burst pressure. See burst pressure is the maximum pressure that you can apply to this membrane and when you apply that burst pressure that is the maximum pressure, the membrane will rupture because the maximum stress that silicon can withstand is 7 gigapascals that is 70,000 atmospheres okay.

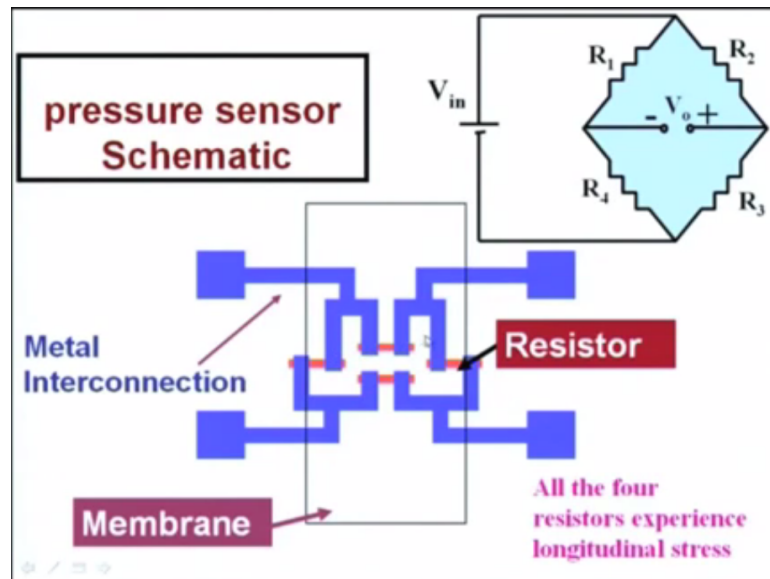
So you can see I take $2b$ as the length, $2a$ as the width of the membrane and the stress will be maximum at this $x=a$ and $x=-a$ at the smaller width the stress will be maximum in this direction. So we have to see by again using the ANSYS simulation what is seen is if b/a ratio is 1 okay that is it is 500 and this is 500 you saw that the stress for a given pressure the stress is less here that means to reach the critical pressure or you will reach the critical pressure when you apply higher pressure.

Now if you increase the b to twice that a , the stress here is more that means you will reach the rupture stress even with the lower applied pressure that is the thing what happens. So for example 15 micron thick membrane, the rupture stress will be about 220 atmospheres okay when the length and width are 500 microns. Now if I take it almost double here that is width is 500 micron, length is 1000 micron that is 1 millimeter.

At that point, the stress is much higher here for a given pressure that means rupture will take place at a lower applied pressure. So the burst pressure occurs, earlier it was about 210 bar or when the ratio is 2 for a 15 micron membrane it will occur even at about 120 or 130 bar so that means you must remember that if a designer rectangular membrane, the burst pressure will be low and the usable range goes down.

But as I mentioned last time the usable range is decided by when the nonlinearities are seen that is output voltage divided by the pressure should be linear, it will stop being linear above certain pressure when the deflection of the membrane, maximum deflection at a center becomes one tenth of the thickness of the membrane. So the membrane thickness is 10 micron you will see at what point what pressure the deflection becomes about 1 micron one tenth on that.

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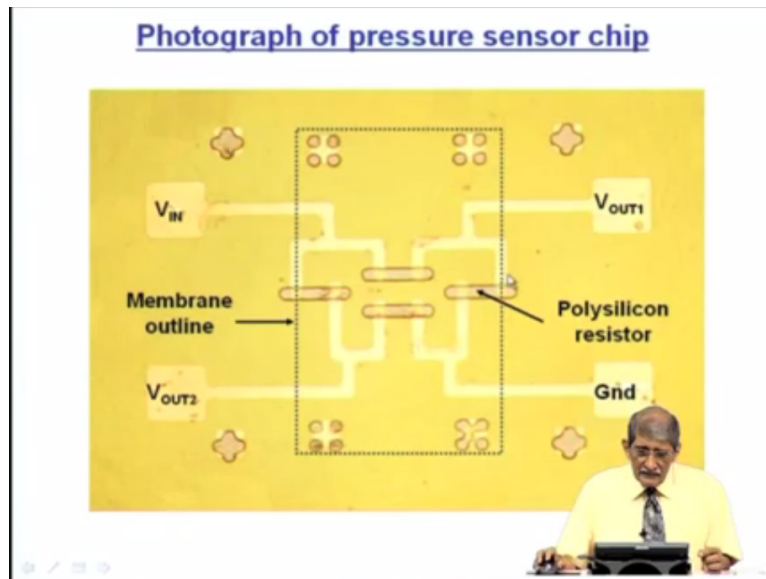


That is mathematical apply okay. Now we will see it soon how it will work out. So these are the guidelines for designing and all the time I have mentioned is the resistors are put on opposite arm for the bridge see for example here they are put on the opposite arms of the bridge these 2 will go up, these 2 will go down okay.

Here you realize the resistors, these 2 resistors on the edge are located they are R1, R2, R3 if I put, R1 and R3 are going up because they are longitudinal tensile factors, R2 and R4 they are put on the other opposite arms, they are compressive tensile stress, they are going down by the same amount okay. So as discussed on single crystal because this is going R3 okay if R3 goes up and R2 goes down if this voltage go up and here similarly R1 goes up and R4 goes down this voltage becomes negative, this positive.

Otherwise if I apply 5 volts that is 5 volts here and 5 volts here this goes up and this goes down, this will be 5+ something and this will be 5- something that is why there is a difference voltage plus minus here. So this is the way they range out by considering all the points that we have discussed and you take this length of the membrane as double the width of this membrane you get best sensitivity.

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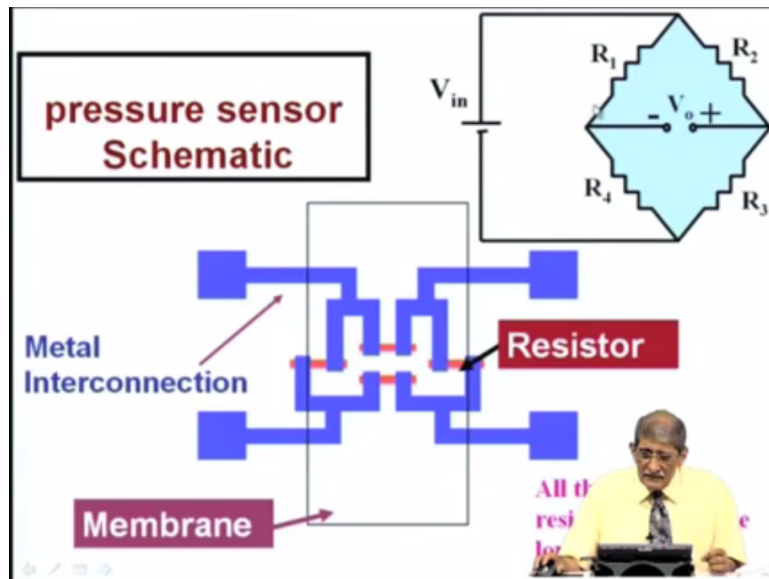
Let us see this so with that SOI approach this has been realized in laboratory. The photograph of the device that you can see that I have put this dotted line here to, this is the photograph taken from the top, you cannot see where the membrane is but to tell you where the membrane is located I have put this dotted line after taking the photograph. So these marks what you see here .

They are all the marks which are there to align one layer to other layer because backside membrane is here I must align these resistors exactly in this location those are done by some of these alignment morph on the wafer that is the photolithography technique, which you would have discussed already alignment okay.

So you can see these are the resistors, these are at close to center, these are at the edge and this white what you see is aluminium wire laid out on this oxide, this is all oxide, there is a resistor on the oxide, these are connected together, taken to this pad where you can bond wire. Similarly, other 2 are connected to it and the taken to the pad. The symmetry structure is used because you do not want to have difference in the resistance from here to here and from here to here.

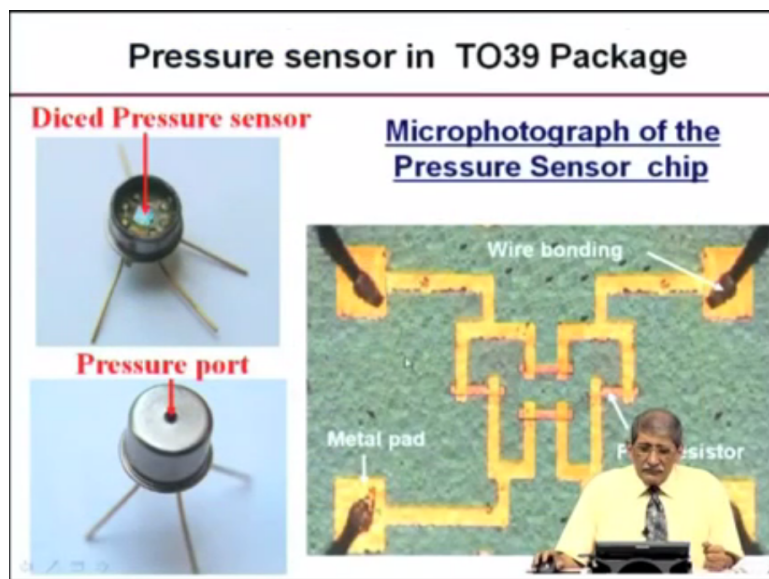
Because otherwise then this is where you apply the voltage and take the voltages otherwise there will be extra resistance, which are different from here to here and here to here.

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So the R that you talk of will have this resistance of this wire also, so this length and this length is chosen equal so that resistance from here to here and here to here is the same thing so that the bridge is exactly balanced okay.

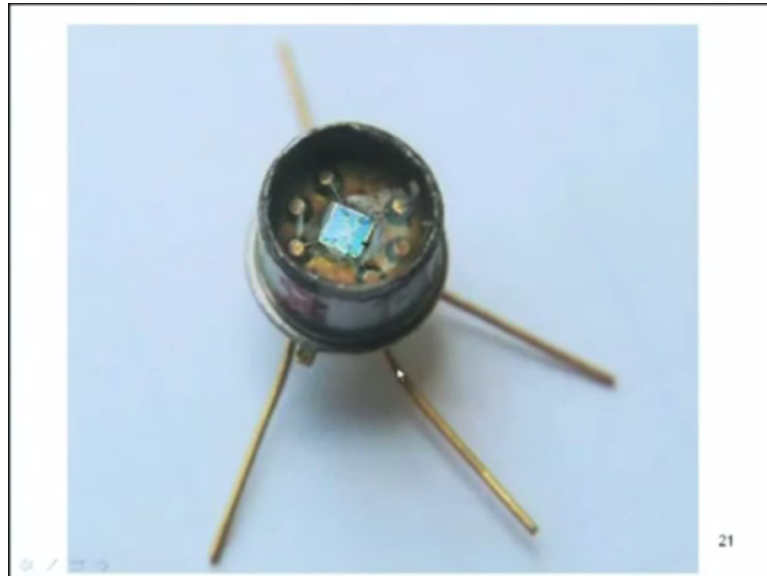
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Now this is the photograph of this wafer, but this was on a different chip instead of aluminium you will have gold in that, for some reason we have changed that in one of those runs. This is the silicon, you can see it is a surface was etched you can see this is rough and these are the 4 resistors and membrane is somewhere here. I have not marked that here.

These are the gold wires on the wafer which oxide is present and you can see these pads here where the wire is bonded on to that and taken out of the chip on to the posters will see what it is. So 4 pads which are connected we cannot see it here, here probably you can see better.

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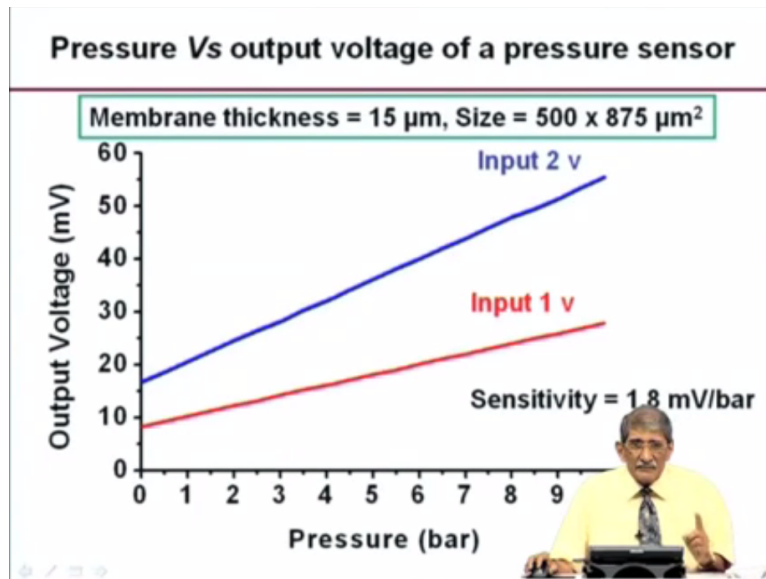


There are 4 pads 1, 2, 3, 4, wire is connected to that to the port and the port is coming out, the port from here to here it comes that is this wire which is coming out. All these ports are isolated from each other by insulation around them. I will show you in the different pictures this is seen much more clearly okay. So this is a packaging that is you dice that into a wafer, mount the die on this header by some glue.

And then do the wire bonding and then put this cap so when you put this cap you put a hole there or put a tube there so that this can be connected, this is the pressure port you can connect it to the region where you want to measure the pressure, you can even take the tube out, put it into the chamber where you want to measure the pressure, put it into region where you want to measure the pressure.

In our case, what we did was by means of a jig we connected it to a gas cylinder so that inside this there is pressure okay. So you can pressurize that and you can see that when you do the bonding etc, membrane is on top, the other side is actually sealed so only one side is a pressure okay. So this is the header, this is the die, this is the wire bonding and the wire taken out and that is the closed one here and this wire can be gold or aluminium okay.

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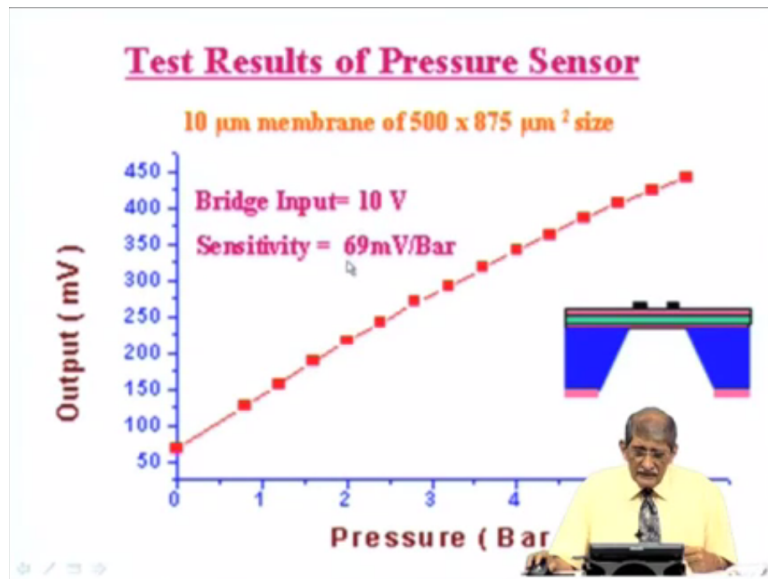


Now quickly going through this is the output, with this device applied pressure and applied voltage to the 2 terminals here like this measure the output voltage as a function of pressure. So you can see that for 1 volt input, the output is linear when the membrane is 15 micron and 500 micron width of the membrane, 875 micron length you get a sensitivity of about a 1.8 millivolt per one bar pressure change.

So one bar pressure change is from here to here which has gone even up to 10 bar pressure, linearity is there okay. If I apply larger voltage, it will get larger output voltage. There is some offset voltage that is even when the pressure is 0 there is some output that is because of some slight difference between the resistors. In practice you do not have to worry if you are changing the slope of this.

Otherwise you will have to compensate this. In an electronic circuit you can compensate that okay.

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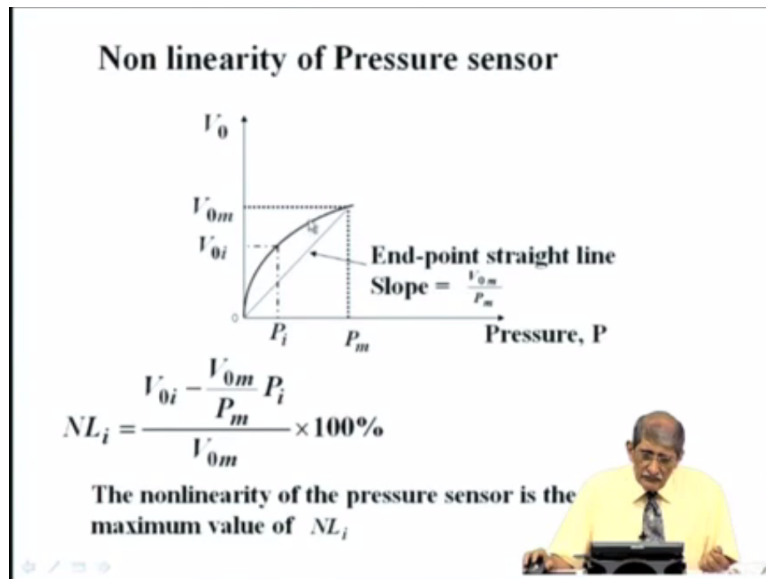


Now let us see this. See this is a 15 micron thick membrane. If I make the thickness less 10 micron, you can see that output sensitivity goes up, for 10 volts it is 69 millivolts that is for 1 volt it is 6.9 millivolts. In the previous case, for 1 volt it was 1.8 millivolts. The sensitivity is better because thickness is smaller, deflection is more. If deflection is more even at lower pressure, the deflection will become comparable to the thickness, thickness is 10 micron so by the time you apply 3 bar pressure the deflection will be about 1 micron.

So beyond that point you get the nonlinearity, the output is not linear. It has not gone to burst, it can be operated even up to 6 bar, but linearity will not be there but if you want to use it without considering the nonlinearity you can use it. If you want linear range over a range of pressure you must restrict it to about 3 bar where it is linear you get about 69 millivolts per bar per 10 volt input.

For 1 volt input it is about 6.9 millivolts okay. So there is a term called nonlinearity, which is defined.

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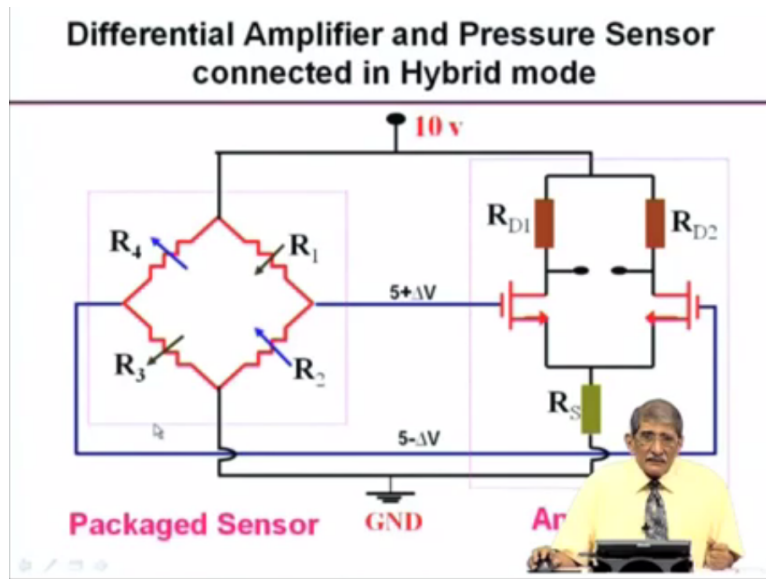
The nonlinearity came to scene like this. If there is a nonlinear characteristic in the pressure sensor and output the maximum pressure from something like P_m , find out what is the output voltage, join these 2 lines if this is actual output characteristics at a given input pressure, see what is the difference between this linear curve and this actual curve, see the difference okay V_{0i} – this point that is second term that is numerator is this difference divided by that that gives you the nonlinearity.

So the nonlinearity will vary where you are operating so for example here if I am operating this at 6 bar pressure that is the maximum pressure, maximum output is 450 millivolts for 10 volts. Now if I am using that 3 bar pressure okay if it were linear, it should have given 250 millivolts output, but because of nonlinearity it is given about 275. So this difference between the 2 the actual curve and the linear curve is 75 millivolts, 75 millivolts divided by 450 millivolts that is the full scale output that is about one 6th.

So the nonlinearity in this case will be about 16% you cannot tolerate that. So this type of device, we can use only after about 3 bar pressure if I use 3 bar pressure, the nonlinearity all over this range will be less than about a percent okay. So one would recommend this sensor with this thickness and these dimensions to use for only up to about 3 bar. If I want 10 bar, recommend 15 micron thickness with that dimension.

So hire pressure for the same dimension lateral dimension membrane to be thicker and thicker okay.

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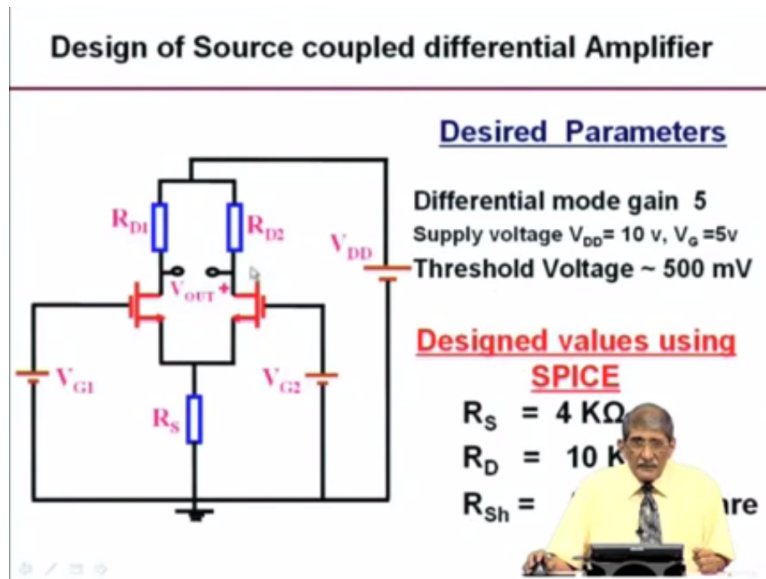


Now quickly going through the integration. I can integrate this pressure sensor with a differential amplifier on the same chip with the SOI approach. So this is the differential amplifier that we will not get down into discussion on that. That is I can give the output of this pressure sensor, connect it to the gate of the MOSFET and take the output at the drain of this MOSFET.

You will get output is equal to difference between the 2 voltages. So the difference between the 2 gates is 5 volts and 5 volts here 0 you will get 0 output that is there is no pressure, all the R_s are same for 10 volts input divided equally 5 volts, 5 volts no output 0 output. If the output is 0.1 volts by -0.1 volts, 2 volts will be output that will be amplified by the differential gain that is 5 volts if you have gain 5 output will be 1 volt.

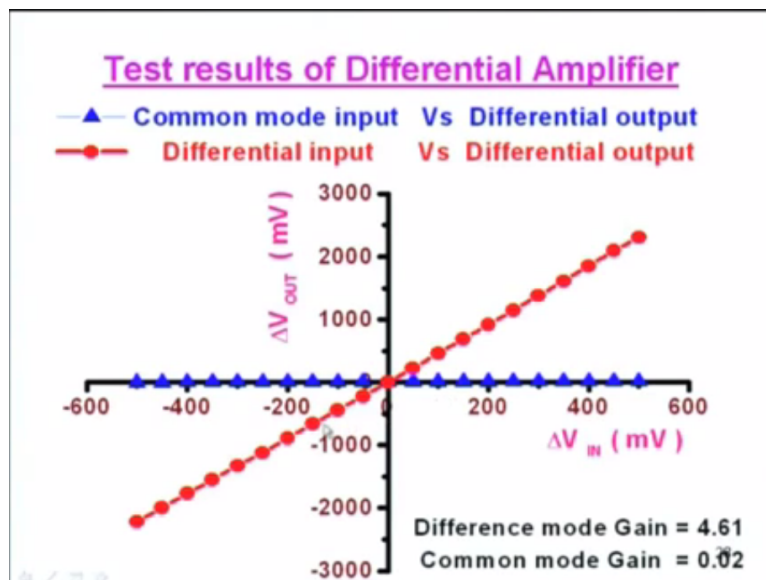
So you can amplify depending upon the gain which is decided by these resistor values. I am not getting down into the design of this in this presentation okay.

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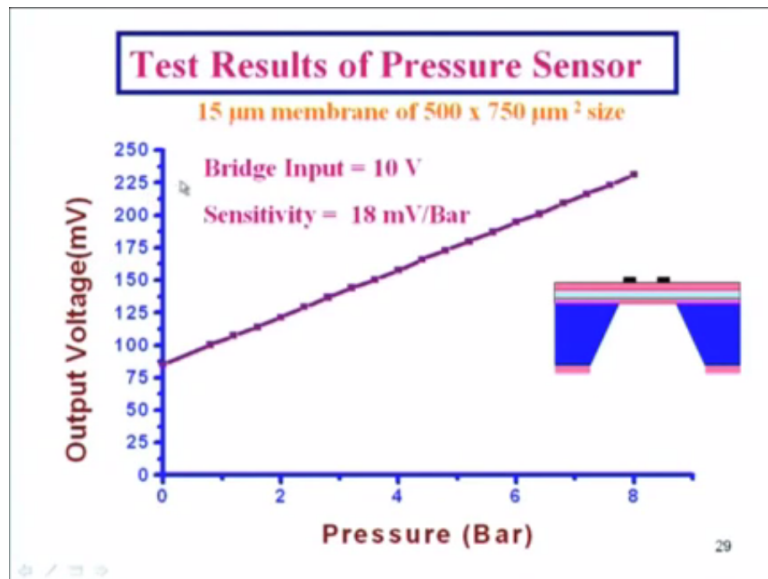
So this is design with the certain values of resistors to get gain of 5 using a simulator.

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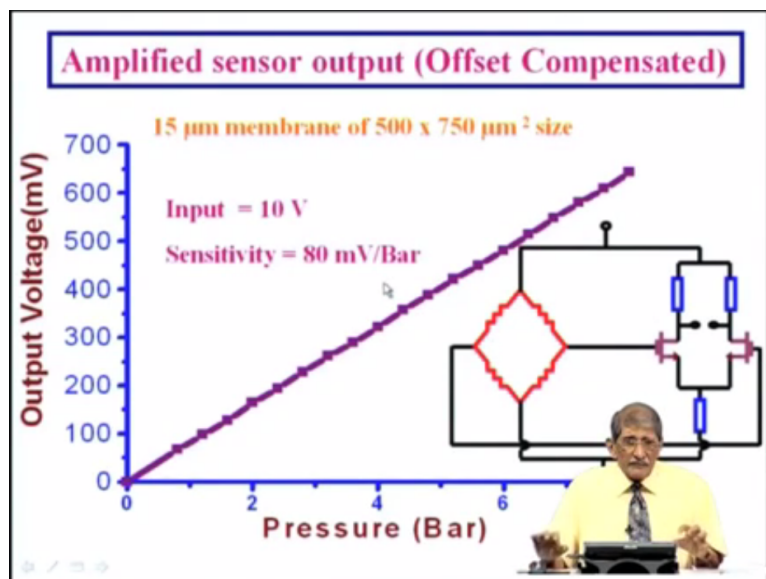
And you can see that differential input gets amplified, delta V output versus delta input is linear, the gain is about 4.6 for this device when fabricated, design was about 5 and if I apply same voltage that is a common mode gain is very, very small. So remember common mode rejection ratio should be high for differential amplifier, this is about 160 okay, $4.6/0.02$, 230 okay.

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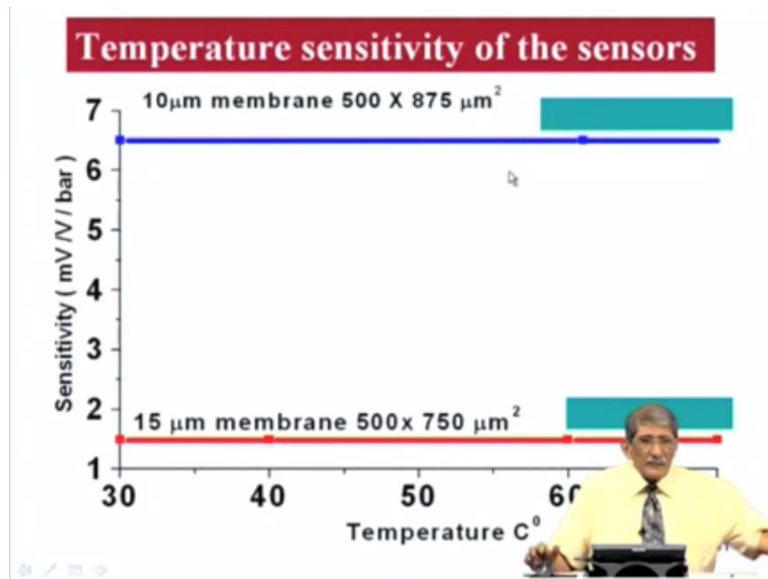
So now what I am pointing out is that 15 mm thick membrane without amplification give 18 millivolts per bar for 10 volts, for 1 volt it gave 1.8 millivolt per bar okay.

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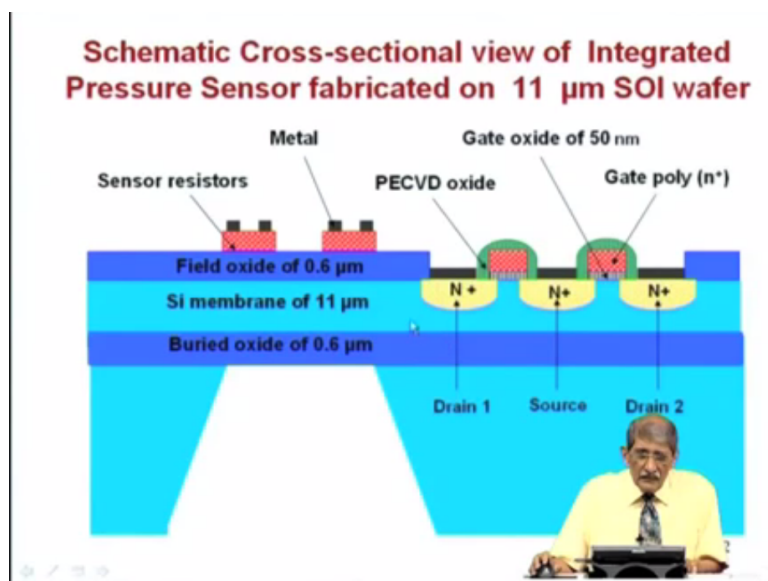
Now I connect an amplifier like this, these 2 are fabricated separately initially and if I connect that gain of 5, I get what was originally 18 millivolts now which gives output of 80 millivolts. This was initial run to check the optimization of the 2 processors.

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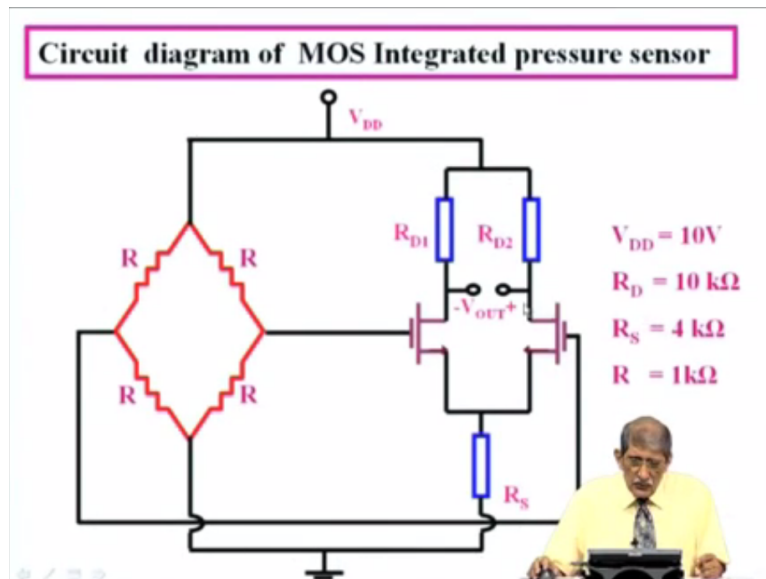
And if I take the sensitivity as the function of temperature that is almost constant from 30 to 70 degree centigrade. So that polycrystalline resistor, which is used as a resistor worked out very well for higher temperature operations okay.

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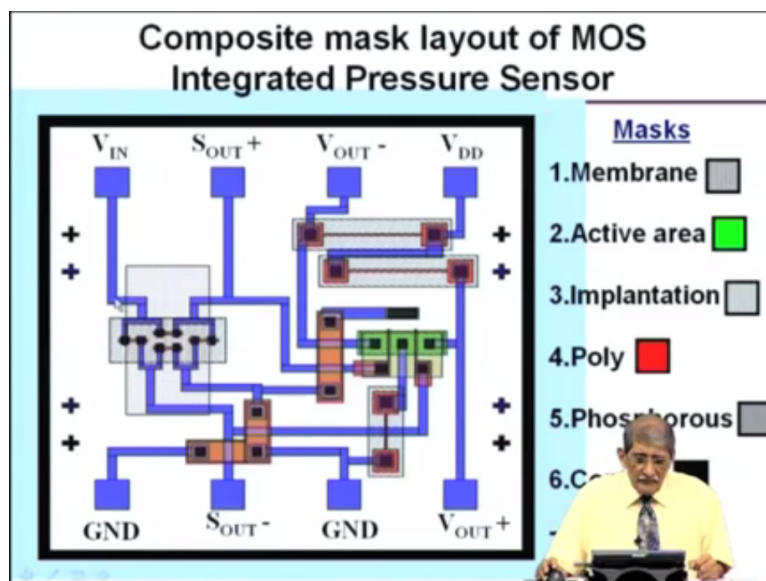
Now you can see the SOI approach, silicon on insulator silicon oxide silicon, in this portion of the wafer, fabricate the sensor by etching from bottom, the SOI layer thickness decides the membrane thickness then you have the resistor here 4 of them from which the 2 is cross section and then the MOSFETs, source drain and source drain, resistors I have not shown here we will see in the top view.

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This is electronics and the pressure sensor together. So that is to show on this we will have pressure sensor here Wheatstone bridge right hand side you will have the electronics. So pressure sensor on the left hand side on the chip, right hand side of the chip you have the pressure sensor and the electronics of gain 5.

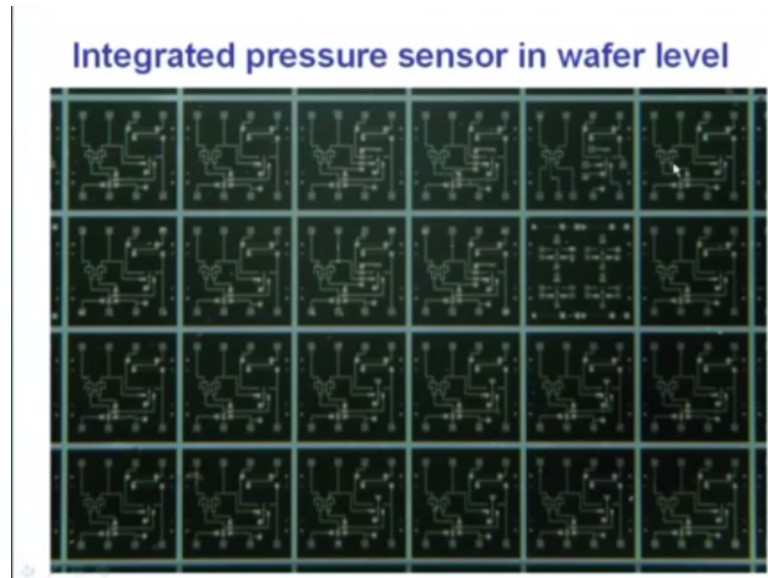
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Now this is to show you how the layout of that will be. See this is repeated number of times on the wafer using the integrated circuit technology. You have the membrane on this portion, I am showing with one device here, membrane, the sensor, blue is the interconnection using aluminium or gold you can see the output is connected to the gate of this, this is the MOSFET, source, drain, gate.

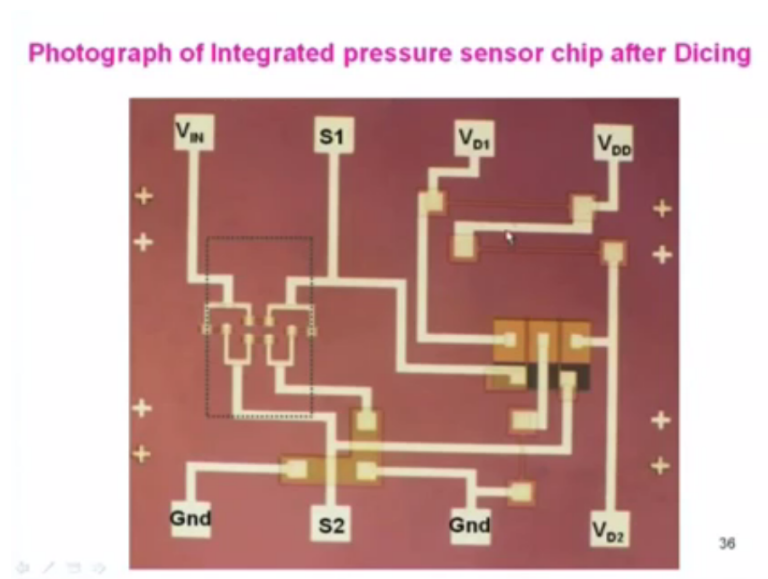
So this output is connected to the gate, the other output is connected to the other gate and from the drain, a resistor comes out supply and here also other drain resistor and the supply, resistor and supply and resistor and supply like this, from the drain resistor and supply okay that is getting down in more, what I am trying to point out is you can integrate to in this thing.

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Now this is actually the photograph I deliberately showed you this. On the chip whatever you saw here is repeated like 1, 2, 3, 4, 5, 6, 24 devices are in this area side by side devices are made on the wafer if you take a photograph this how it looks and these are all the aluminium that you see the connection and what you do is you dice the wafer along these lines, which are known as scribe lines, separate out individual devices okay.

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And individual chip has got one pressure sensor and also the electronic circuit, you can just take them out cut it like this, dice it and then if you take a look at this alone the dye looks like this, see all this together wafer it look like this if I dice it virtually by 5 with a diamond wheel that is the packaging technique okay, cut it in this direction and then you can take out this individual chips that is how it looks.

This is the membrane portion where the 4 resistors are there and this is the MOSFET portion, the MOSFET has got 2 resistors which are tenuous load you can see here, 2 MOSFET, 3 resistors that is electronics here, they are here the resistors okay.

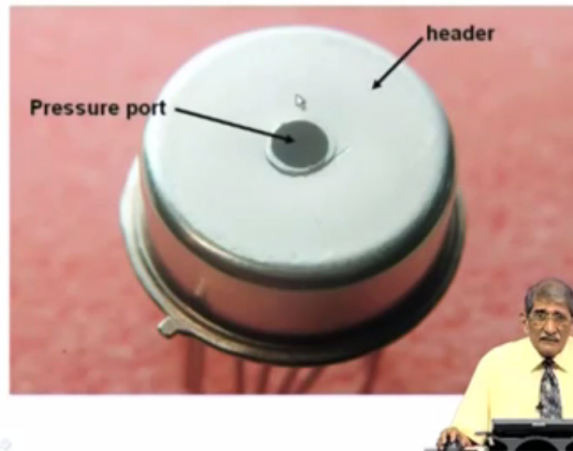
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Now if I take a look at this, this dye see what you have done is scribe this or dice this, taken this dye, mount it on the header you can see on the header there is a chip and you can see the bonding parts here, you can see the wire bonded to this taken to the other ports and this port and this port are isolated form this insulator. So there are all each one of those pads are connected by means of this wire very clearly you can see okay that is chip mounted on the header by means of glue, wire bonded on to this mount pad and take along to the poster that is where the pressure port is.

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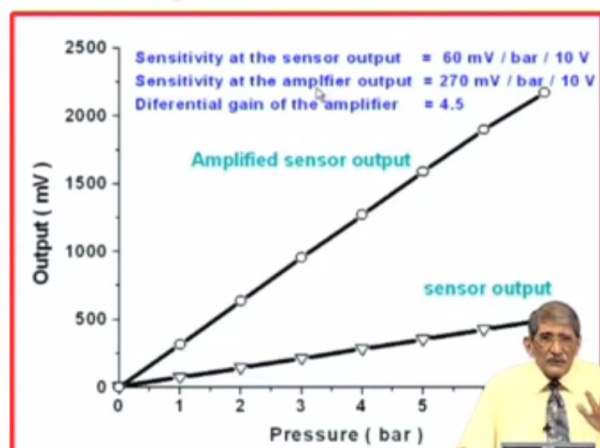
Integrated pressure sensor in a package



I can apply pressure to this, test it.

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Pressure Vs Output Voltage of the packaged Integrated Pressure Sensor




That is the test result. You can get without the sensor with electronics this gain of 4.5 and to demonstrate that you can use this for realizing this integrated electronics okay several applications are there which I have mentioned earlier.

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Summary and Conclusions

- Despite several engineering challenges, MEMS offer high performance and are small, low power, and relatively cheap.
- Micro machined Sensors have been fabricated along with Electronics by the batch process of silicon wafers .
- The pressure sensors find wide range of Applications for industrial, automotive, biomedical and aerospace and defense establishments.



And in summary you can make these devices integrate them, pressure sensor and electronics together okay.

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You can use these references where some of the articles written by me, review article on pressure sensor then some of my students on this integrated sensor, papers have been published on this (()) (58:10). Thank you very much.