Micro and Smart Systems
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Lecture - 12
Extended Approaches for Working Microsystems

In this lecture, I plan to cover some of the approaches that we have seen in previous lectures towards building useful Microsystems.

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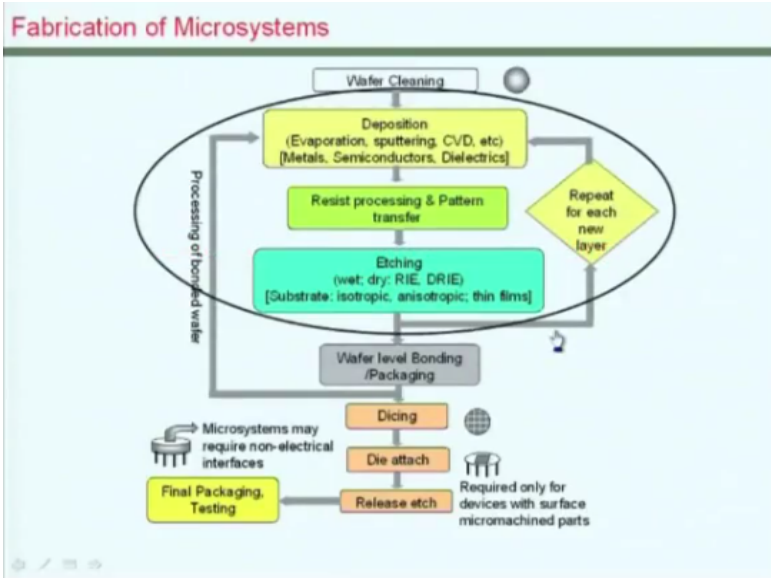

If you may recall Microsystems fabrication involves a series of cross steps, many of them are done within this loops where you have deposition patterning or pattern transfer and then you know repeat those to build useful Microsystems. Deposition schemes involve evaporations, pattering, these are 2 of the physical deposition schemes commonly used. There are several chemical vapor deposition schemes.

On top of these films we transfer the resist and then transfer the pattern using lithography and then use various types of etching to remove part of the film. Then you can add another film and then continue this process.

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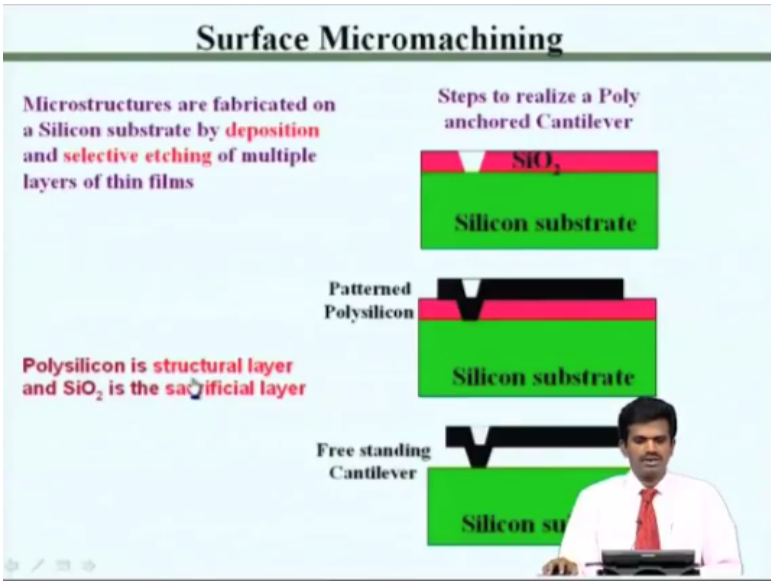

We have seen how this could be extended towards building freestanding cantilever structures like the one that you see here. What we do there is to start with the silicon wafer and then add a silicon dioxide layer which works essentially as a sacrificial layer later and on top of this silicon dioxide layer we had a polysilicon which would remain here as the structural member. These materials are tentative you could use possibly other various other materials with some constraints in terms of their chemical and other properties.

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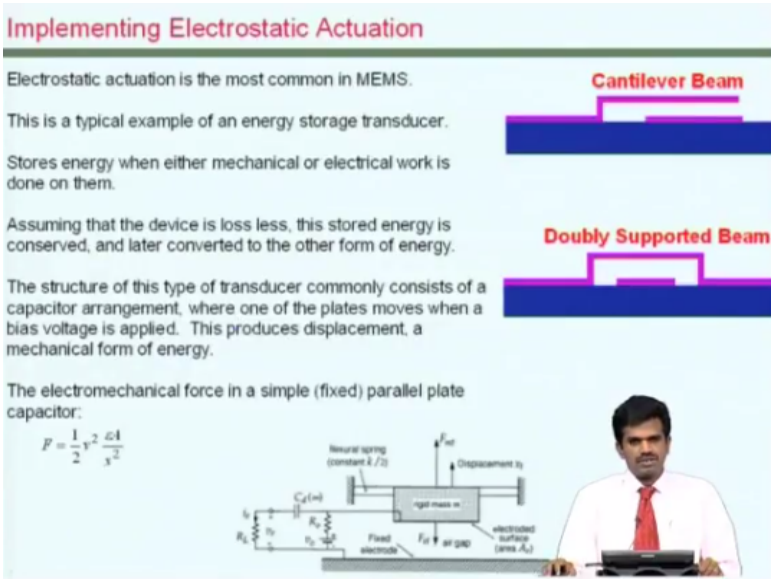

We will see now how this could be extended to building useful devices for example a micro relay or an RF switch. The configuration of this could be one of these it could be either based on a cantilever beam or a double supported beam. In this first case when the beam is actuated

electrostatically, the contact is made and there will be a transmission from one side to the other. In this case, in this example you can see here, when the actuation takes place there is a short-circuiting happens which essentially bypasses the circuit.

So in both cases as you see what we essentially have is equivalent arrangement that you see here where you know the beam structure is supported and is actuated in electrostatic force basically pulls it down. Now to realize these devices, we will essentially need to create this gap while fabrication and that is where machining can help.

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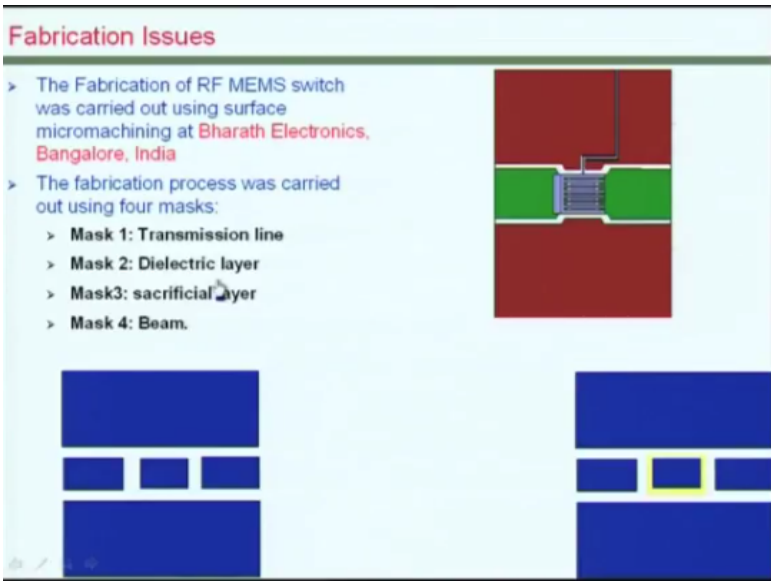

So in one of the devices that we have designed for this purpose you know there is a slight difference in the beam structure that you see here and you may notice that there is a small electrode behind those things. So, the first layer of this whole geometry would look somewhat like this where this is essentially the input side, this is the output side and these 2 bigger patches that you see are essentially the ground traces.

The square pass that you see here essentially the bottom electrode that will be used and that you may see behind the mesh like thing on this side. Obviously, we will need to have these traces also. So the next step would be to add after patterning this. So if you actually see the various masks that would be used to build such a device. The first mask should essentially define something like this.

In the next mask, we need to define essentially a dielectric layer which would be protecting the bottom electrode rotating because it has to prevent the arching happening when this top electrode comes down and touches that. So it essentially protects that so that has to be patterned obviously after deposition. The next would be to deposit and pattern the sacrificial layer so that essentially creates the elevation required to put the cantilever beam in this case.

So after this cantilever beam is defined and patterned and in this case as you see it consists of a series of fingers, is essentially to help in increasing the speed of etching while you know the sacrificial layer is later removed. It also helps in the dynamic characteristics of this device. It sort of reduces the voltage required to activate this device and things like that. But this is one improvisation that we have done to fabricate a micro delay kind of this device.

So as you could see there are all these at least these 4 mass are required to fabricate a device as which may appear as simple as this.

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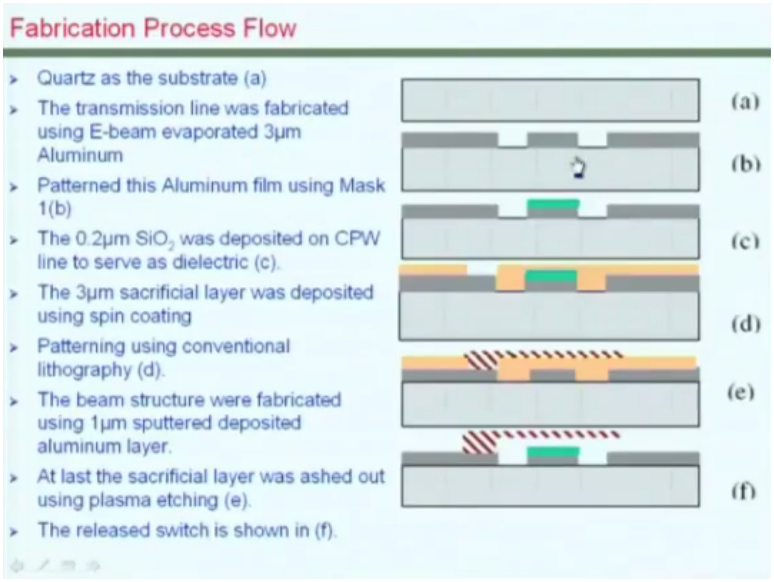

And if you go through the process steps, we can start with the substrate and on top of this first as we have seen the transmission line is fabricated by first evaporating aluminum on to it and then patterning this aluminum. The next step is to use SIO2 to basically add this protection layer that I mentioned and on top of that after patterning this we will add the sacrificial layer to create this

height and in this particular case we create some room here so that an anchor can be built to construct the cantilever later.

So the anchor is first built and then the cantilever structure is built and this is patterned and then the sacrificial layer is removed by plasma HA. So as you could see a number of process steps are required and all of these have been discussed in detail in the lecture on sacrificial, in the surface micro machining process that we have seen.

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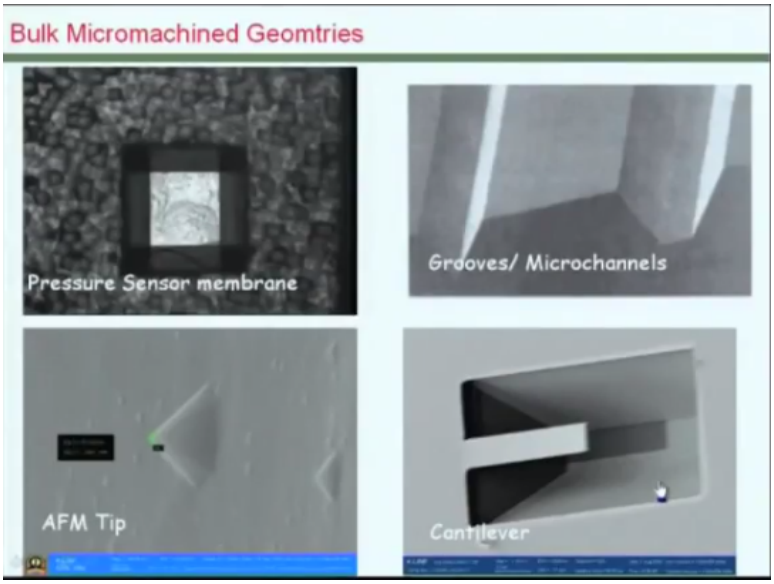

Bulk micro machining also discussed can be used for various devices as you see here one can built cavities one can built tip like structures, one can build cantilevers or gross using bulk micro machining process, all those processes have been discussed separately.

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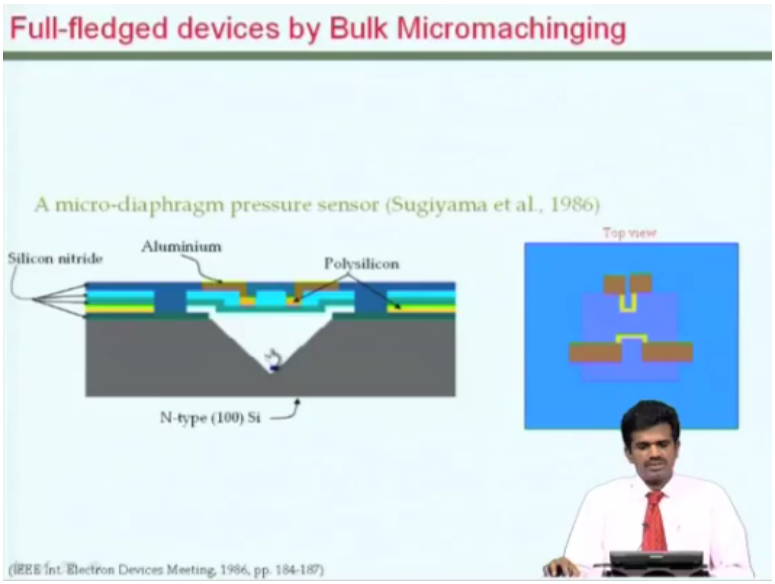

Now look at full fledged pressure sensor using this approach. You see that there is a diaphragm kind of geometry here and then there is this cavity below that. How do we go about building this? As you see we need to build all these thin films, we also need to create this cavity, we have seen that cavity like this could be built by bulk micro machining. You have seen that all these layers could be added by this series of deposition and patterning steps.

And one can build all these layouts on the top. How about going fabricating the device like this? The first thing you should remember is that if you first do this etching you can obviously not put all these additional layers horizontally like this because if you do this first when you deposit these layers they will grow and sit conformally on to this cavity here. So how can we actually fabricate geometry like this? We will have to think of alternate ways of doing it.

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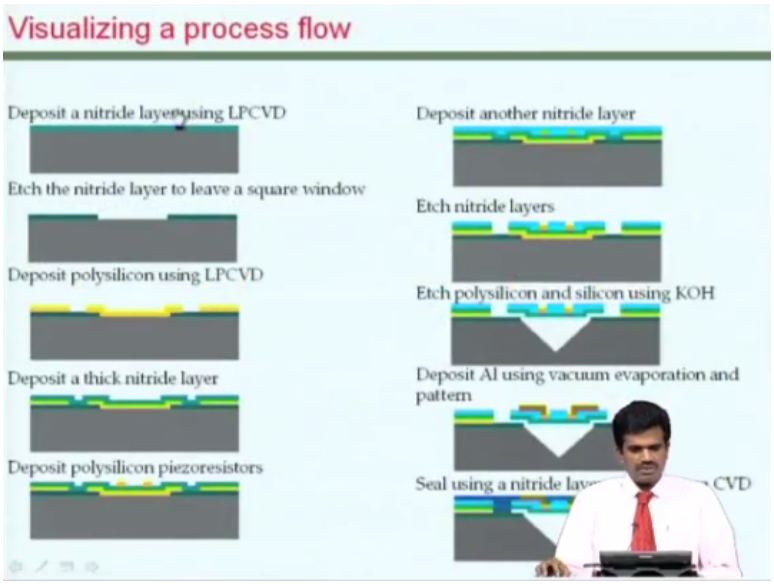

We will basically first build all those top layers and pattern them and then only etch through sideways and etch down towards the substrate. So in this particular case we have nitride deposited and patterned and polysilicon layers added which would essentially work as those resisters which would, whose resistance would change based on the deformation and additional layers and finally this KOH etching the anisotropic etching of the silicon.

To recall, anisotropic etching of silicon can result in significant undercuts. Undercut meaning etching below some top geometry. So if the window is defined properly, the etch window from the top of the wafer is define properly, it is possible to go underneath and create a cavity below that.

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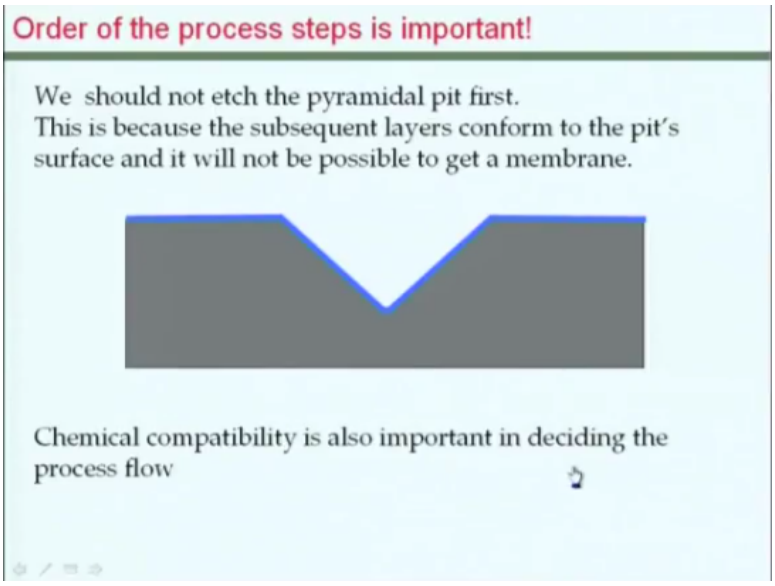

So the thing to remember is that although this geometry you know it looks appealing that we are going from bottom to top. You should not be etching the pyramidal pit first and you should also think about the chemical compatibility in deciding the process flow because if you are using this KOH etching the layers that you how you put previously here should not be affected by this KOH etching.

So we may how to choose materials and processes for these previous layers based on what is going to come. So this is one approach of building something on top of a cavity like this.

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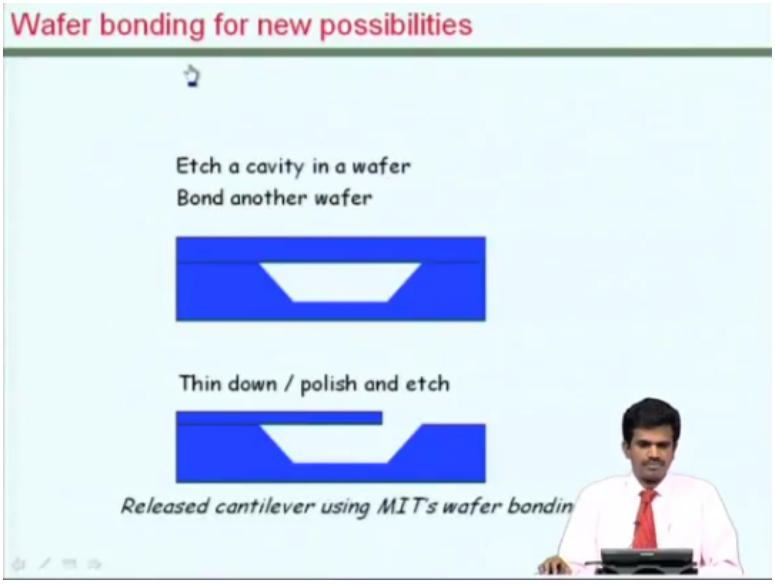

There is an alternate approach to built structures above cavity. And many of those use what is called the wafer bonding process. What can be done is that you create this cavity and the bond another wafer on top of it to create this kind of closed cavity. It can be etch standard for cantilever kind of structures as well. This process as I mention is called wafer bonding process.

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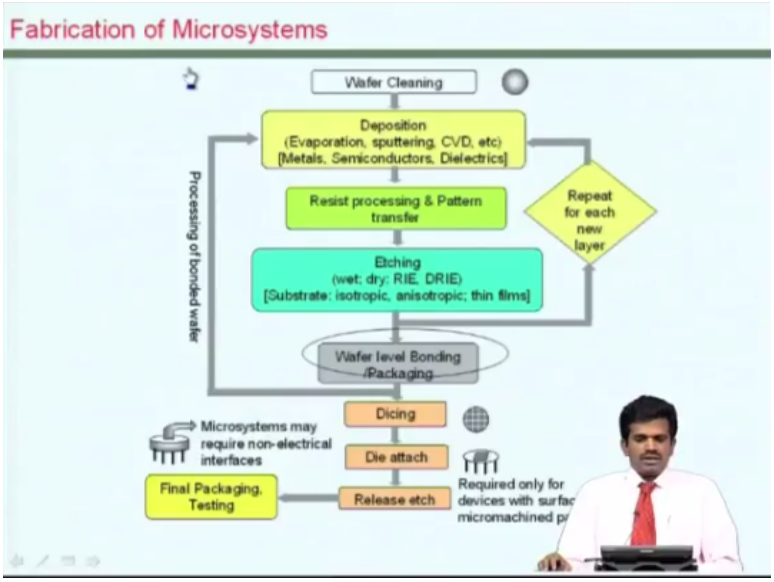

As you see from the flow chart that we have been using the wafer bonding process is one of those steps which is used in this closed loop what I mean to say is that even after it is done first of all while the full wafer is under process, secondly it can be subjected to subsequent processing of deposition and etching afterwards. The question is how do we do this and you may recall this is now a partially made geometry.

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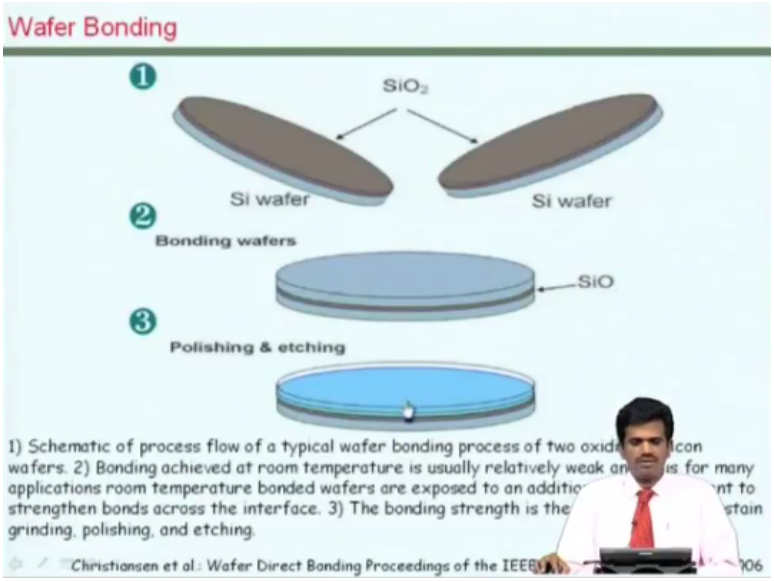

So how do we add wafer on to the surface of a partially made structure? To do that there are various approaches of attaching 2 wafers. May be silicon to silicon, maybe silicon to glass, various options are available to do that and basically what we do is that we start with these 2 wafers in the silicon to silicon case, we have an outside layer in between which essentially facilitates this close bonding between them.

And this bonded wafer is so well neat that it works as good as you know a regular single wafer that you would otherwise see. So we will see the process steps involved in creating this kind of bonded together wafers and how to build devices out of that.

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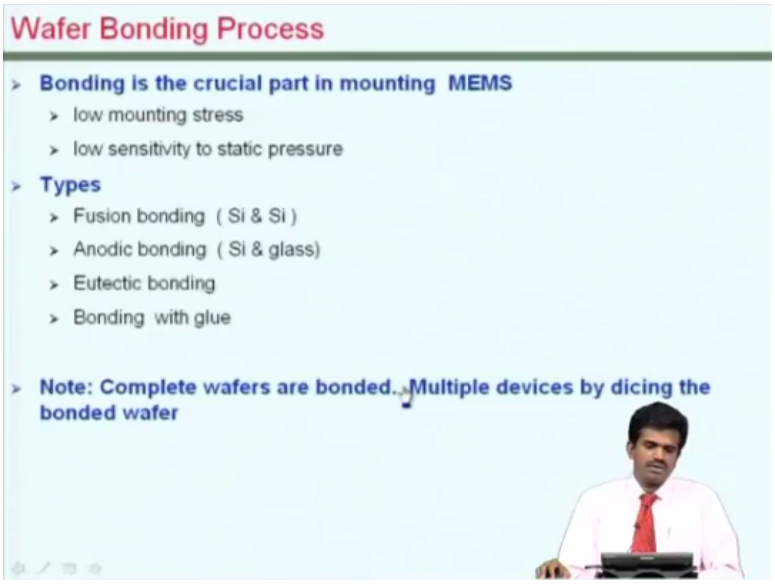

So as you would notice this kind of bonding is the very crucial thing in many Micro Systems. There are several approaches to build bonded wafers of silicon or silicon and a glass wafer or it could be based on additional layer as you would see later in this lecture. One thing that you should note is that this is bonding usually to complete wafers. This is not a part of a device getting added to a part of another device.

So you know it is not like the conveyer belt approach of fabrication. It is a batch approach of fabrication as you have seen.

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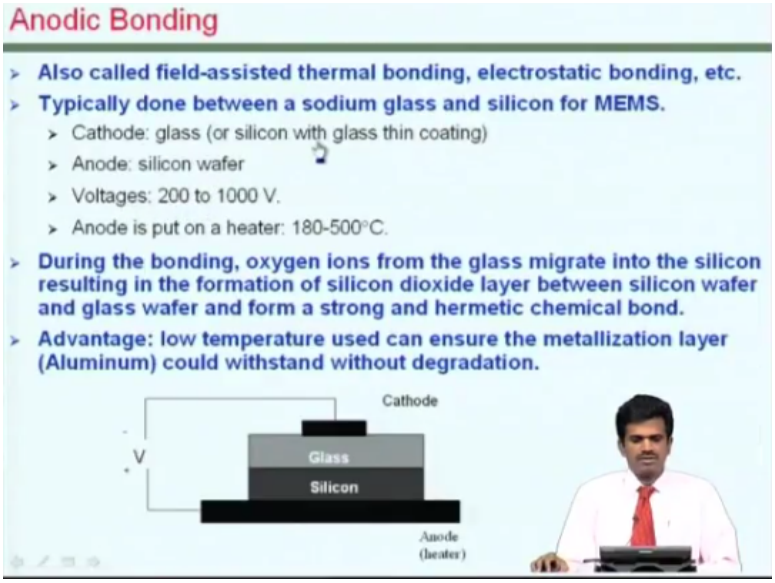

One of the approaches as we mentioned for bonding 2 silicon wafers is by Anodic Bonding. So as the name suggests there are electrodes and you know you apply the potential between them and to bring them in contact you also need to provide a sufficient contact force and pressure and also to enable the bonding will also use the temperature of the order of 400-degree centigrade. So what happens is that you may know that if you put 2 glass pieces together they have developed sufficient bonds that you know unless you apply some kind of a shear force.

They do not separate out. So when you have this kind of mirror finish to the wafers that you have, there is a chance that they already in good contact. But we need to ensure that this contact remains and does not even go anywhere even when you apply a shear force. And that is why this additional process steps are used to create this bonded wafer.

This is relatively low temperature of process which could therefore be used even when you know metal layers another are included within the on the surface of silicon or glass. So the process conditions would be applying this potential, applying a contact pressure and also applying the temperature.

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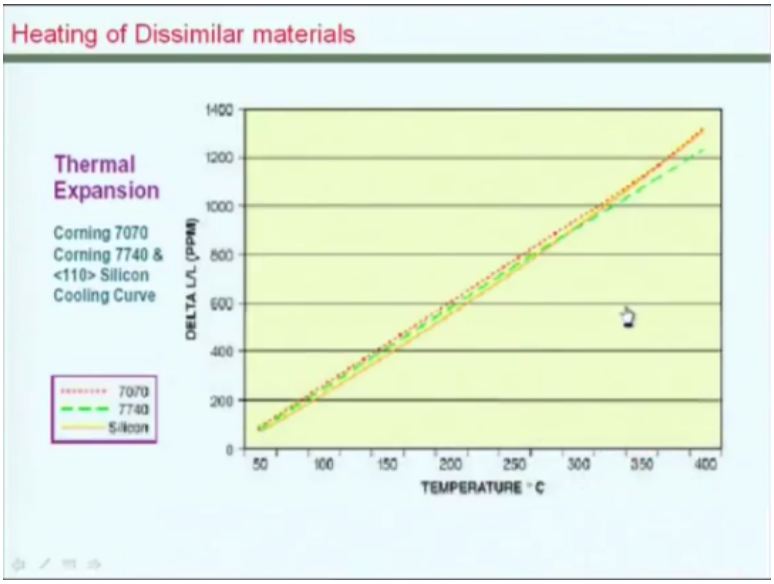

We wonder what would happen if you are to use these 2 different materials, silicon and glass. It so turns out that some of the glass composition that we use for this kind of purpose have the same thermal expansion characteristics as the silicon wafer. So there is no shear force that would happen at the kind of temperature ranges that we are subjecting it into. So it is not a problem from that point of view.

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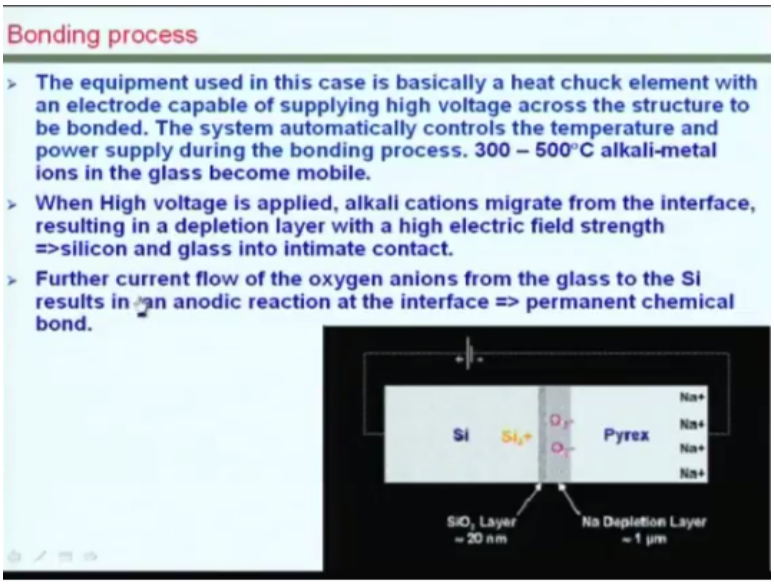

So when these kind of glass that you see there and silicon wafer that you have, when these are bonded together essentially there is some kind of migration of ions happening at the potential that you apply which would essentially facilitate the bonding to happen.

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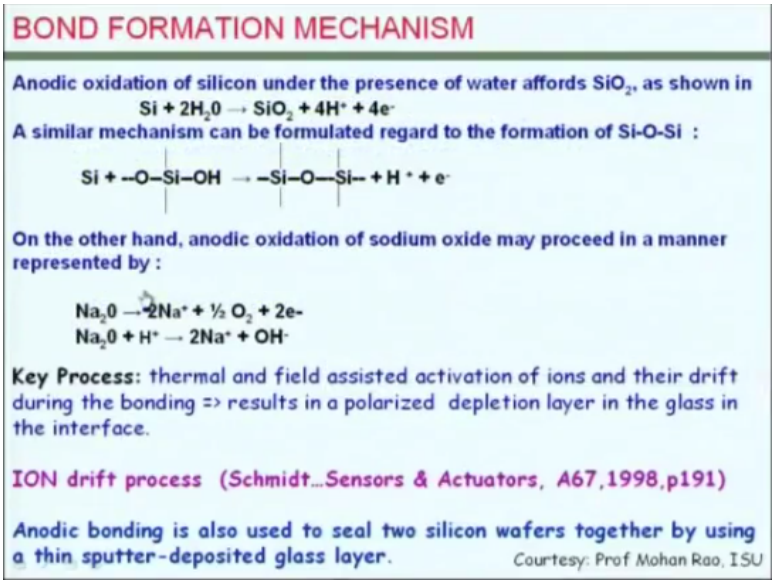

So the bond formation mechanism is explained here. So silicon under the presence of water would create this SIO2 and you know it is also resulting this SI-O-SI kind of a structure on the surface of the wafer when there is sodium present in the kind of glass that we see there this would resulting an OH bond being created there. So the key process involved in this wafer bonding of glass and silicon is essentially this thermal and electric field assisted activation of these ions and there drift which essentially result in the bonding together of these wafers.

By the way these wafers need not be completely clean you could have partially built geometries as I mentioned on top of them but essentially we need to ensure that there is sufficient blank area on top of the wafer which could be put to contact to create this kind of bonding mechanism. What I mean to say is that if you have a totally covered geometry on silicon then it may not work as well.

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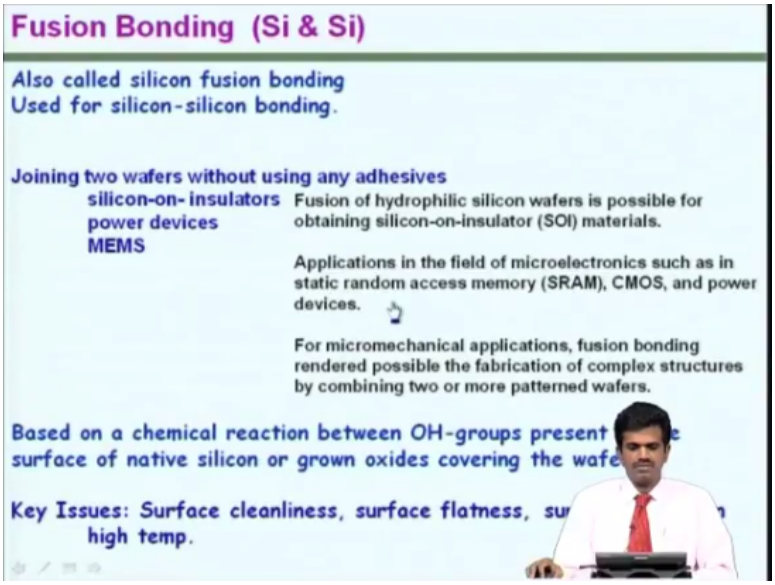

Alternately, it is also possible to bond to silicon by wafers by a process called fusion bonding or it is essentially a silicon to silicon direct bonding approach. This can be used to create what are known as SOI silicon on insulator wafers. It is also used as Microsystems and many microelectronic devices. So in this case also essentially the surface cleanliness the flatness of surface and retaining the hydration of the surface at this high temperature this will be subjected to that would matter in the process.

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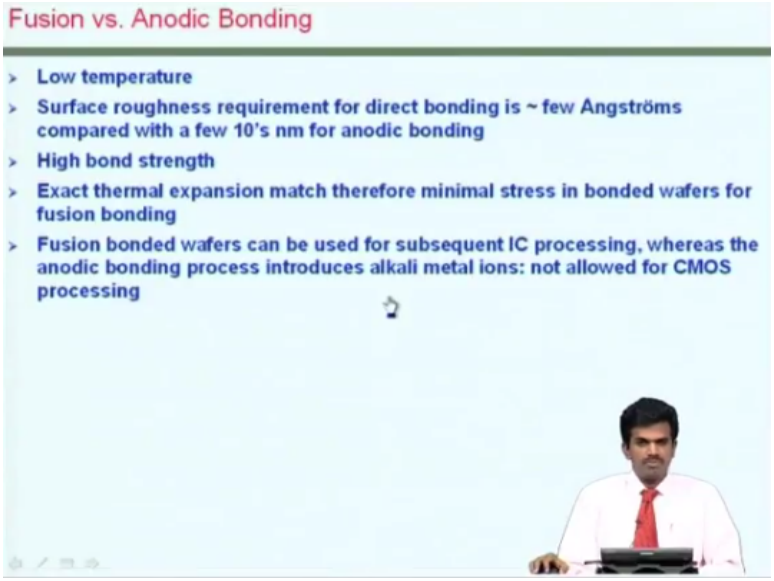

So the surface roughness is a key thing in success of controlling the surface roughness is a key thing in the success of these approaches. These wafers can be used and have been used in IC processing itself and many of the CMOS processes could be subjected to because you have both on both sides silicon wafers.

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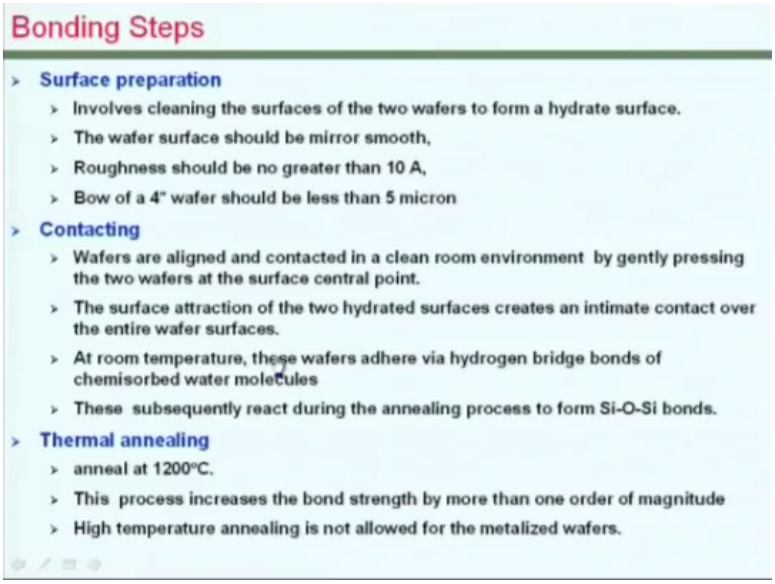

So as I mentioned preparing the surface and retaining the roughness and bow of the wafer within control is the key thing in the success of bonded wafers by this approach. After that just like you put 2 glass pieces together here you know we need to make them in contact and apply the temperature and then make them to bond together and usually we anneal it higher temperatures so that permanent contact is made.

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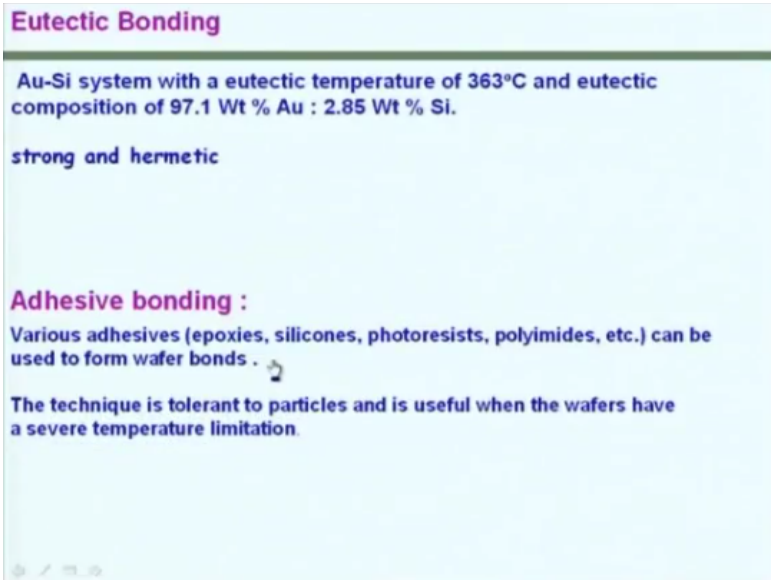

Another approach that is often used is known as eutectic bonding in this case a thin layer of gold is used on top of the silicon to essentially enable this bonding. The temperature is of the order of 360 degrees with the kind of right; basically the weld material has the composition as you see there. And the next approach is by adding an extra adhesive layer of various types like epoxies or polyamides which could you know create bonding between this at relatively lower temperatures.

So that you know wafers when this serious temperature rises that are required in the previous cases can be avoided.

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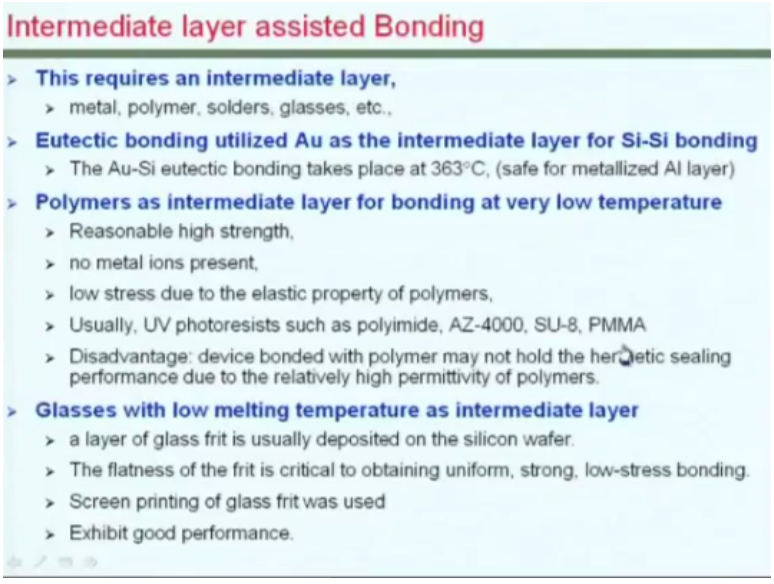

So all these approaches could be used for bonding to wafers, polymers as I mentioned have this advantage that you know their requirement is relatively lower temperatures. It is also possible to use some kind of a glass free layer to facilitate this bonding which could happen at relatively low temperatures and low stress.

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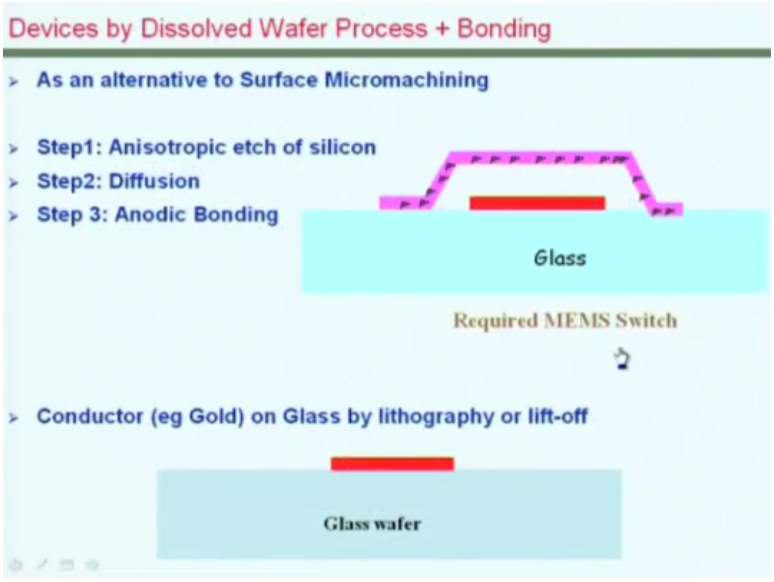

Now we will see how this can be extended to building Microsystems. What I show here is an alternate approach to build a micro switch using a process known as the dissolved wafer process which involved the glass to silicon bond. Essentially happens in 3 steps how we attach this top moving member on to this glass. We obviously start with the glass wafer and then pattern this conductor the red color conductor which could be gold and can be patterned by either lithography or lift off.

Lithography if you recall is a process in which first the conductor layer is deposited and then you spin the hotter resist and transfer the pattern and etch the conductor layer. Liftoff on the other hand which start with the resist and then pattern the resist and on top of the resist you put the conductor and subsequently remove the resist and along with the resist the unwanted region of the conductor is lifted off.

Both these approaches could be used to create the conductor layer on the glass wafer that you see. But this all novelty or you know interesting characteristics come on fitting this additional, the beam on top of this glass wafer that you see here.

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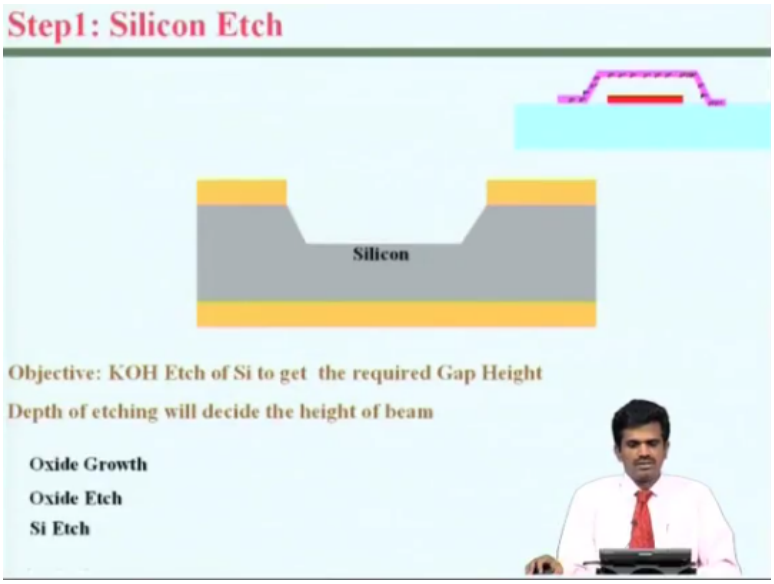

To do that will actually start with a silicon wafer and we will do KOH etching which is essentially anisotropic etching to create this height on silicon wafer. So eventually the silicon wafer is going to sit on top of this glass wafer and we will bond them together. So the depth of etching will be decided how deep, how high this beam would eventually be.

So to create the thing we obviously need to first grow outside and then etch the outside to create the window and then etch the silicon to create this gap and then remove this outside and you have this patterned silicon wafer.

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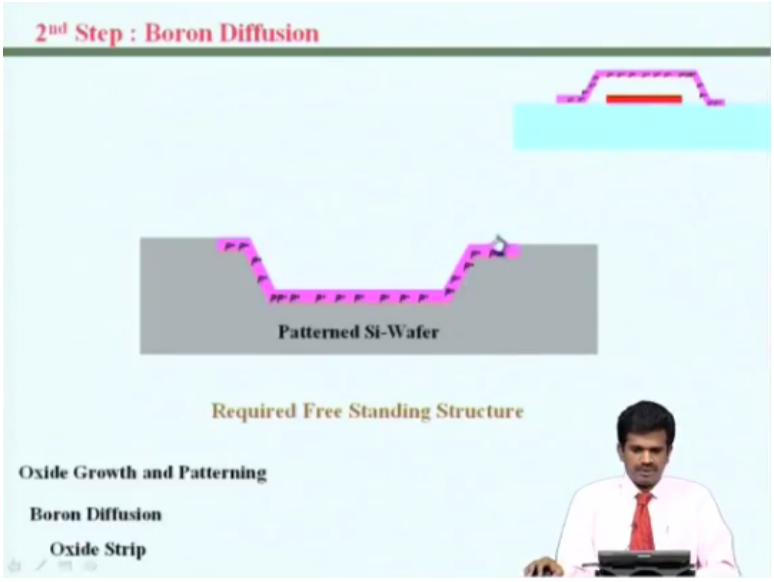

Onto this wafer, we now do boron deposition, a serious deposition of boron and so that it becomes a heavily doped thin layer. So again we do outside deposition and again pattern the outside so that this region is exposed and then diffuse by putting this in a diffusion furnace and then after the diffusion the outside is trapped and how this layer which will be heavily doped region of silicon.

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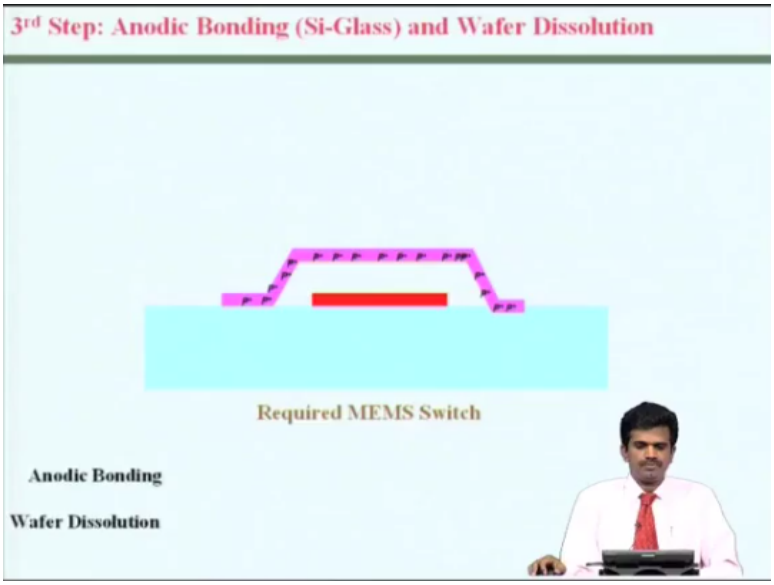

The next is essentially the anodic bonding which could be used to bond silicon and glass wafers. So these are added together bonded together and then we essentially dissolve this gray shaded region of silicon and after that what would remain is this structure that you see there. So in this

case, ultimately what we have on the working device would be the glass wafer on which there is this conductor layer which works as transmission lines.

And we how this heavily dark region of silicon which would work as the top electrode, which could move up and down. So by combining anodic bonding and wafer dissolution, we can construct geometries, freestanding geometries, like this almost the same way as surface micro-machining but without getting into issues caused by the removal of sacrificial layer such as etchants and associated problems. So this is one of the early successful approaches for building freestanding structures.

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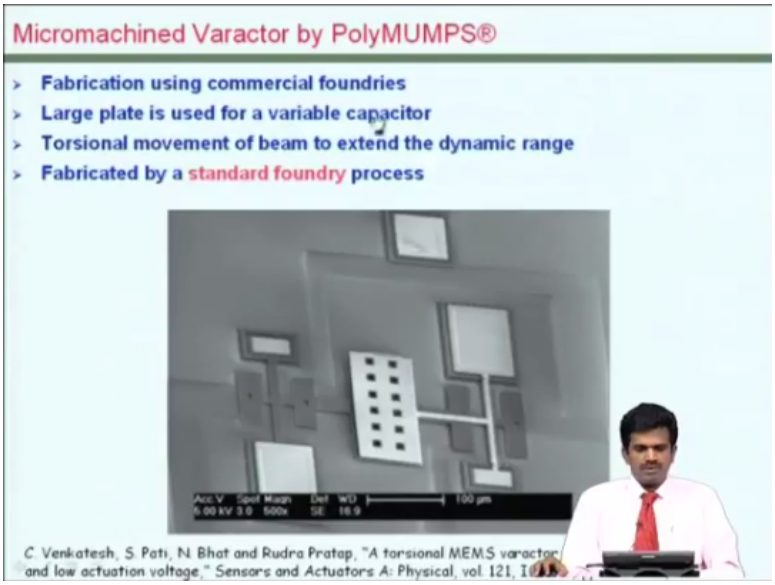

There are also several commercial approaches which could be used for building fairly complicated Micro Systems. What I show here is the picture of a varactor used fabricated using commercial process. As you see here a large plate which is essentially a moving structure and associated with this, there is a smaller plate which would be actually the actuating electrodes in this particular case and you know so fairly complicated looking geometries could be done by this approach.

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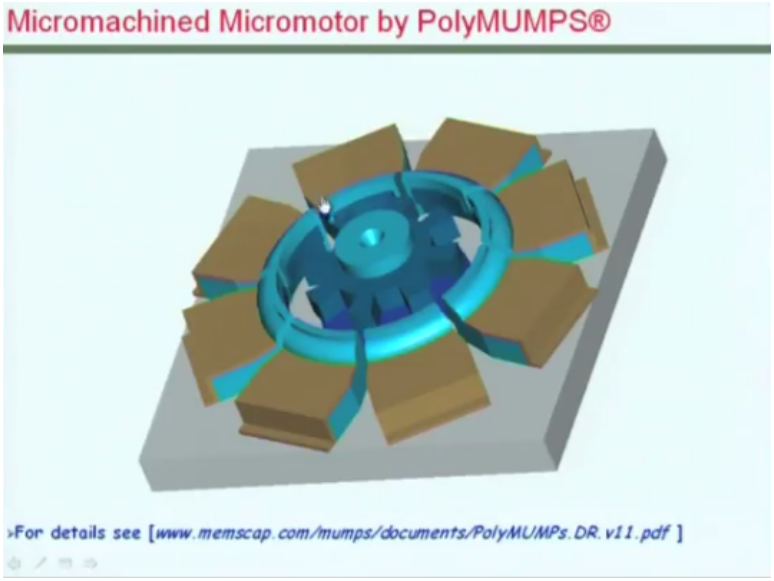

It could also be the same approach as you will see from the websites that the same approach could be used for building even more complicated structure such as a micro motor. We will see how a structure which has you know air straighter and air rotor can be built by the planner processes that we have seen so far and create how to create such a micro motor using these approaches.

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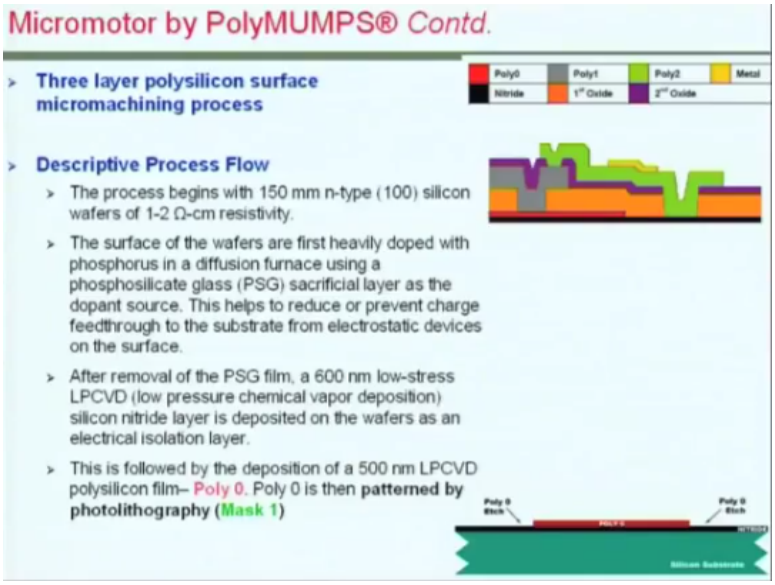

This approach essentially has 3 layers of polysilicon by surface micro-machining such complicated looking geometries could be fabricated. The detailed process flow available from the website has been discussed here. We start with a regular silicon wafer and build all these

geometries and release them to create this freestanding straighter and rotor geometries on top of the silicon wafer.

So a regular silicon substrate is used for this purpose and on top of it a PSG, phosphosilicate glass is first deposited which works as dopant source. So it is you know it has to be first patterned using and then there is a polysilicon layer on top of this place which would be patterned by the first mask layer that you have.

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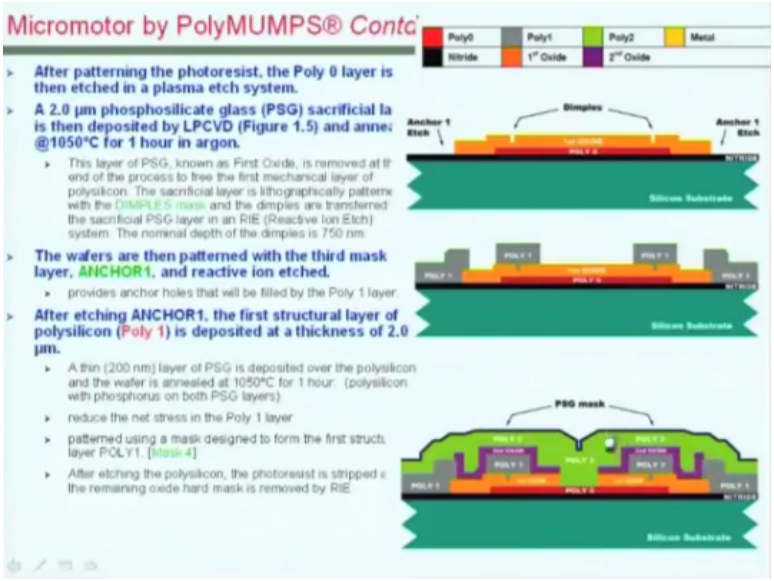

On top of this we again, you know, after it is etched using plasma H and LPCVD is used to add another layer of phosphosilicate glass. This is essentially known as this first outside layer which would create the room when it is removed for the free movement of geometries and then on that essentially these anchors are built to build those rotor geometries. After the anchor is built on the first structural layer, again another thin PSG layer is added and it is process so that you know the stresses are removed and it remain continuous.

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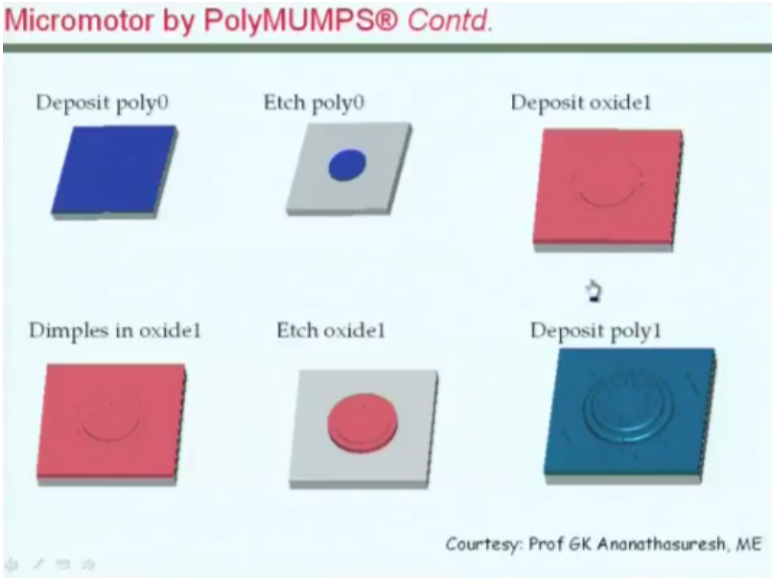

So what we essentially have is that we first deposit a poly0 which is patterned and then an oxide which is again patterned then again poly.

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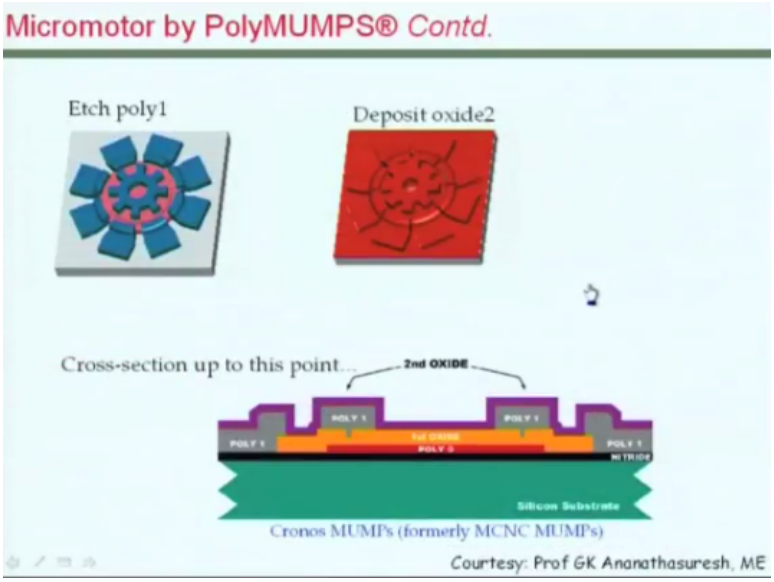

So essentially it is a series of oxide and poly deposition and patterning and you know if you go continuously like that we can create you know this rotor and stator structures on top of this silicon. So by you know obviously one may need to take protective steps in the process so that you know unwanted layers are not removed. So we essentially have these 3 layers of poly poly0, poly1 and poly2 which would be used for constructing these geometries vertically.

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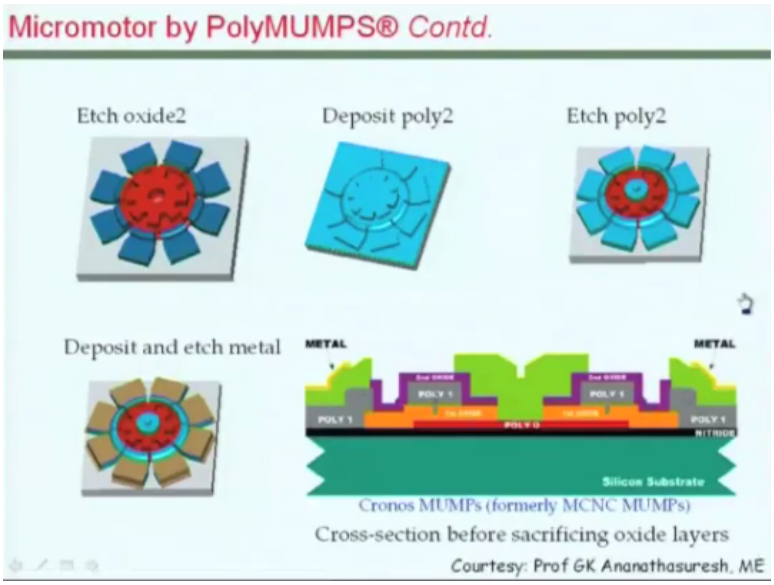

And with the poly2 layer we can create all this stator and rotor geometries as you see it here. On top of it, we can add a metal layer to create the electrical contacts later.

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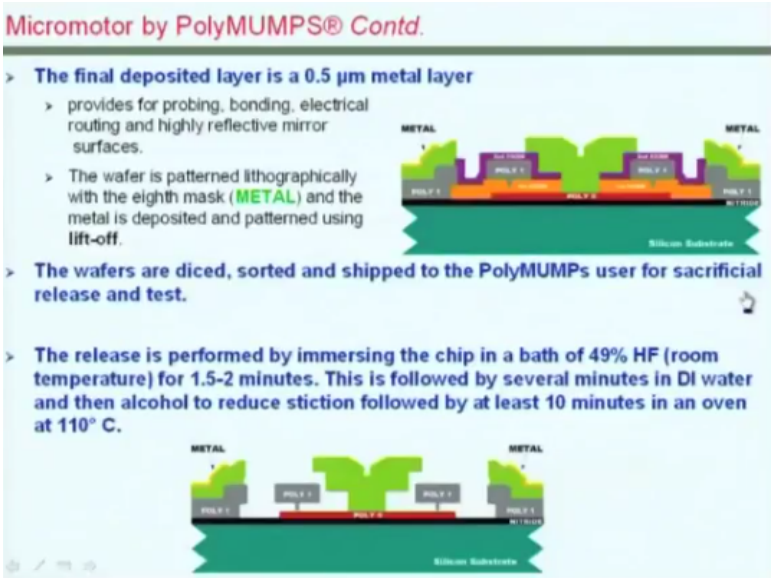

With this after removal of those oxide layers we can create these geometries to be freestanding and the wafers could be used as individual devices by dicing them usually, usually if you recall dicing is done before the sacrificial layer is removed. So sacrificial layer is removed if you may recall by usually by this critical point drawing process if it is used the situation can be avoided.

So you have seen that it is possible to build fairly complicated looking geometries by these 3 layers of polysilicon which remain as structural layers. Are there any constraints? what can happen if you go on adding such layers to even more things?

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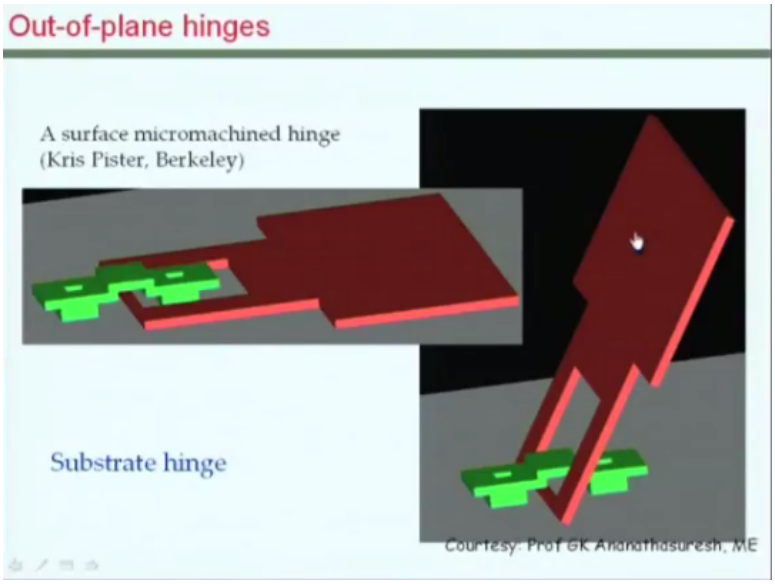

Is it possible to build geometries that can actually know stand vertically. What you see here is you know a schematic of a hinge that has been fabricated by micro fabrication and made to stand vertically.

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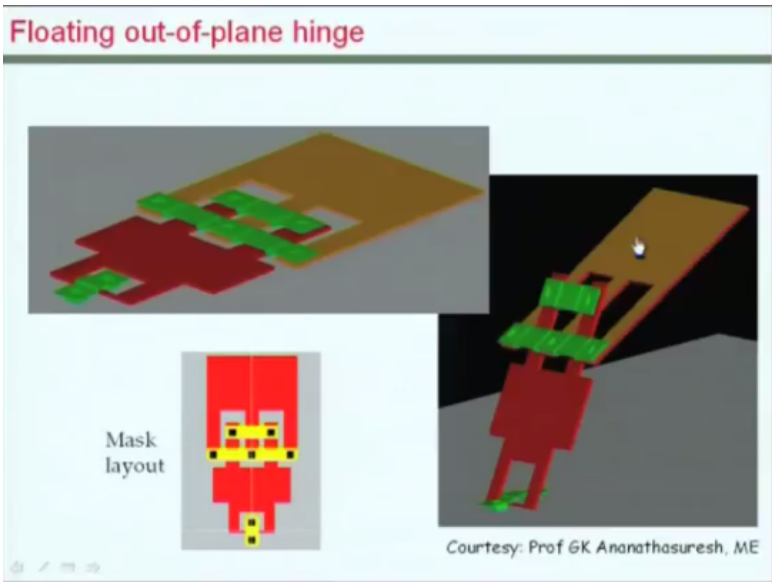

It is possible to do that by having this you know it is only very few as you could see with the colors, there are only very few layers that are used here.

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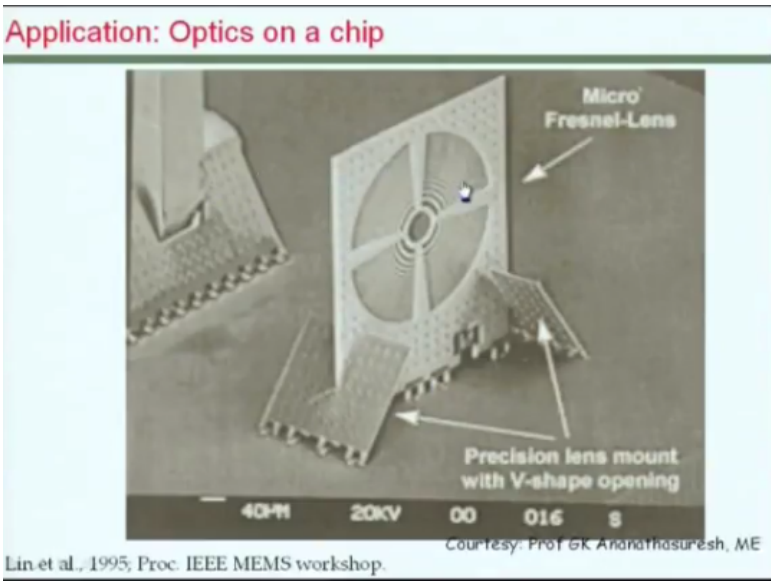

It is possible to make them to stand vertically by slight modifications to the processes and we can even use them in an optical chip.

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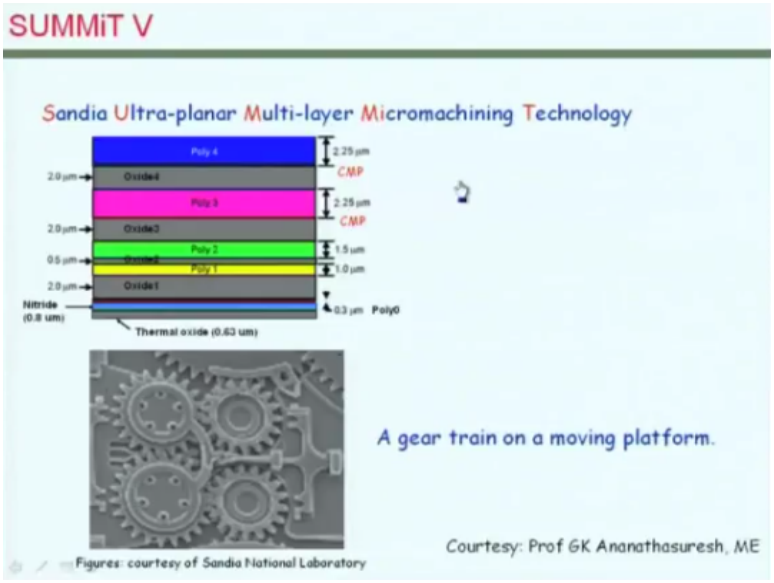

But there are problems when you know if you just use those processes to build too many layers and then if you want to build something as complicated as gear chain that has been developed by Sandia National Labs sometime back. What happens is that when you add the subsequent layers they sit conformally on to the surface of the existing layer. So you know each subsequent layer that we are adding after removing a thick layer, will sit conformally and have these ups and downs on them and essentially the subsequent layers will not be flat.

So when you need geometries like this which should remain flat, there will be problems. To avoid these problems, a process known as CMP, chemical mechanical polishing, is developed.

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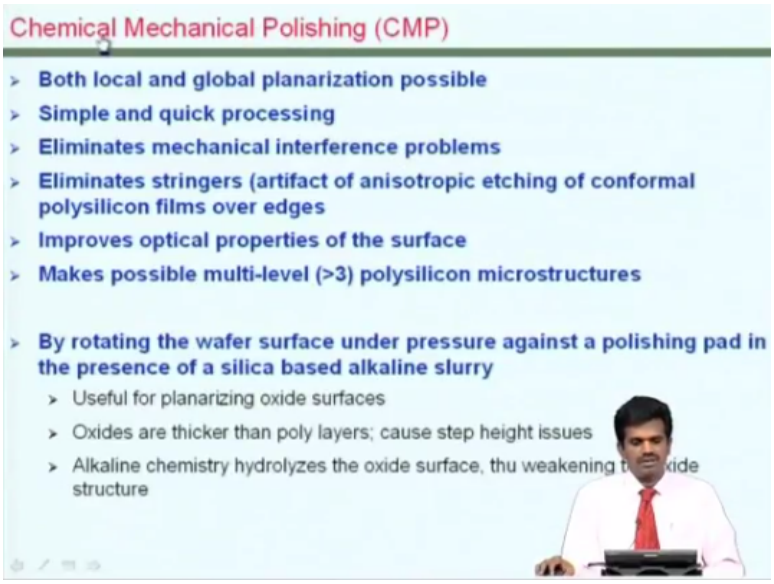

This is essentially used for planarizing the wafers which is partially processed. So as you see here it has both chemical and mechanical aspects of polishing. How do we polish it chemically by essentially etching and we have seen that the isotropic etching of silicon can be used to even out the surfaces. Obviously you all know that mechanical grinding also do the something same.

But in this case you know suitable materials are selected in such a way that we get something better than what could be achieved by individually by either of this. We can get the good optical properties for the surfaces and can create multilevel more than 3 levels of poly silicon by going with this approach. So it has both the elements it involves rotating the wafer under pressure for the polishing in slurry which will also affect the chemical etching of the surface.

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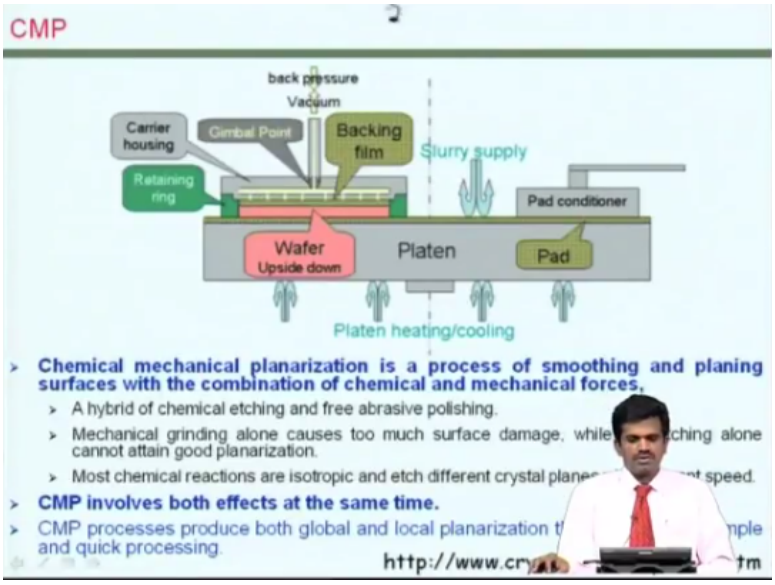

So the process involved would be you know to put the wafer for on a platen which would be rotating and in a slurry which would be chemically active slurry and also which cause the mechanical action mechanical grinding action to happen. So in CMP both those actions will happen together and can be therefore used for quick polishing of the surface of the silicon wafer and this is widely used these days for both microelectronic wafers and silicon wafers.

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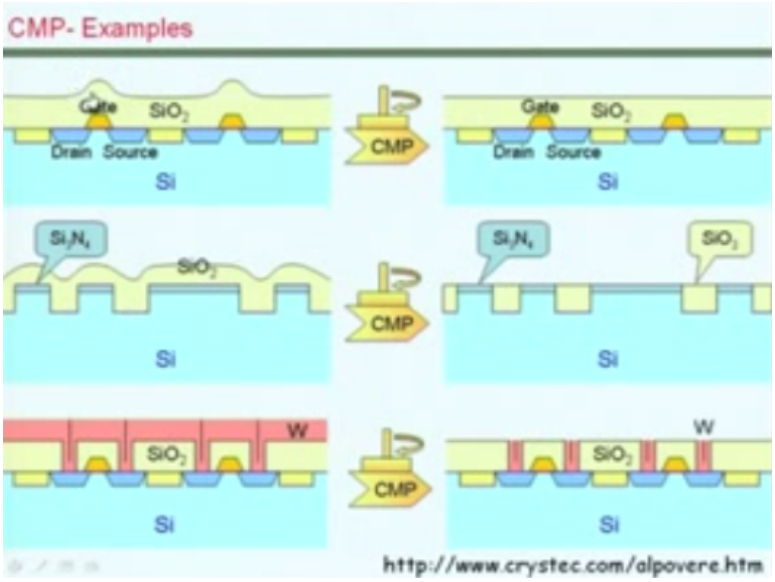

The use of CMP is very clear from the pictures that you see here. As you could see when you have the electrodes built on silicon and then we add the oxide layer above it, the oxide layer will have this bounce, it could be removed or you can even remove you know layer almost entirely by

having limit switch based chemical mechanical polishing of the silicon. It is also possible to do a similar thing even with metallic layers on top not just the oxide that you saw there.

So the bottom line is that you can create planner geometries even after multiple deposition patterning steps, optically flat surfaces can be created by the CMP. The use of CMP is clear from the slides that you see here. If you see, there are these curved surfaces which could be removed by CMP. See these curved members which could be avoided if we were to see use CMP in the middle.

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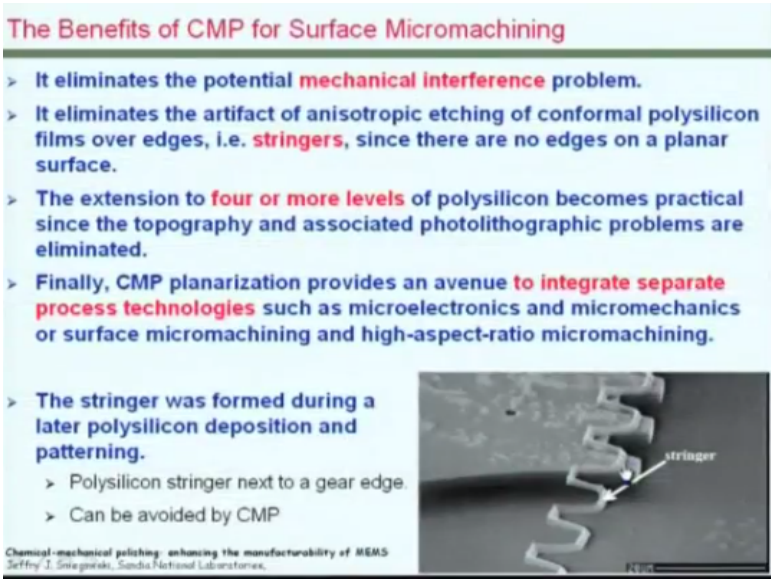

So there is also another advantage in using CMP especially for surface micro-machining. It is the removal of what is known as stringers. When there is this continuous processes you know, because this deposition is conformal, the layer would go down and add to the sides and essentially it may remain even after etching and a thin string kind of thing could remain and that is known as the stringer.

This in polysilicon deposition and pattering is a major issue especially when we do this poly above previously formed structural layers. It could be avoided we have mentioned the flat links could be formed.

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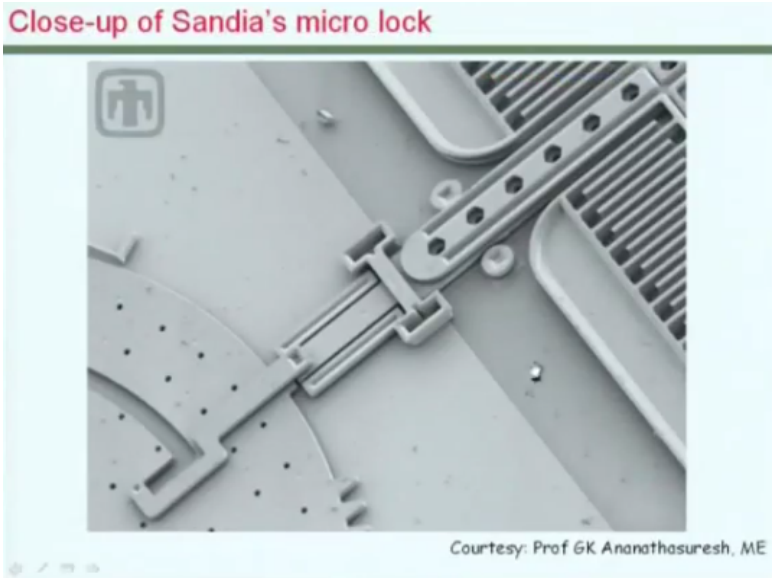

It also enabled multiple layers of polysilicon structures to be form to built complicated looking microstructures as the one that you see here from the Sandia labs.

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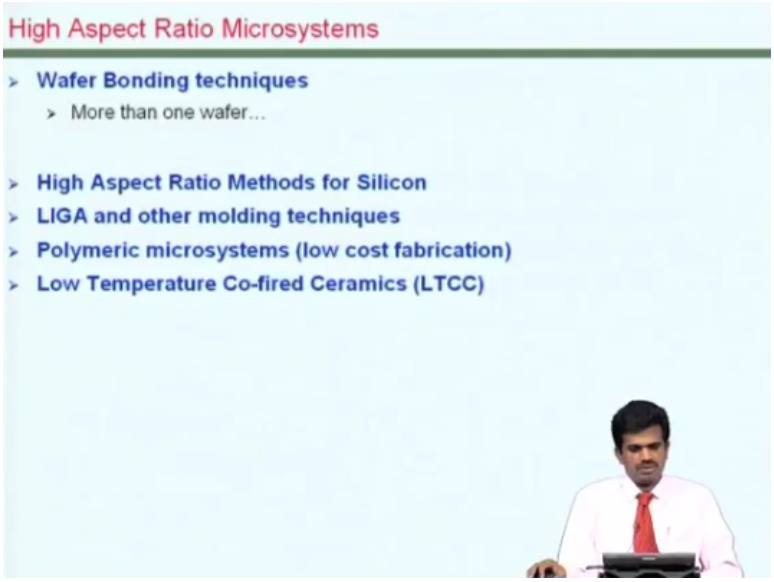

So what we see so far is you know various possibilities with which adding a few layers of poly silicon or other materials one can build fairly complicated microstructures. As we have seen today wafer bonding is a key process that can enable various new possibilities into building Microsystems on silicon. This essentially adds more than one wafer either 2 silicon wafers or a silicon wafer and a glass wafer.

There are several high aspect ratio methods for extending the process that we have seen so far into building geometries which have sufficiently high aspect ratio. What we mean is that usually it means that high vertical dimensions for the structures or geometries. One of the common processes or one of the early processors suggested in this direction is known as LIGA.

There are alternate approaches based on a totally different kinds of materials such as polymers for the would essentially be used for low-cost fabrication of such high aspect ratio geometries there you will also see that the approaches such as low-temperature co-fired ceramics could also be used to build high aspect ratio geometries.

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So we will see now how the LIGA which is an approach which is now available for about 30 years could be used to build geometries based on the fabrication approach is that we have seen previously. In involves lithography to build thick layers but different from what we have seen before it then you know uses electro plating and kind of molding of parts to build these extended geometries.

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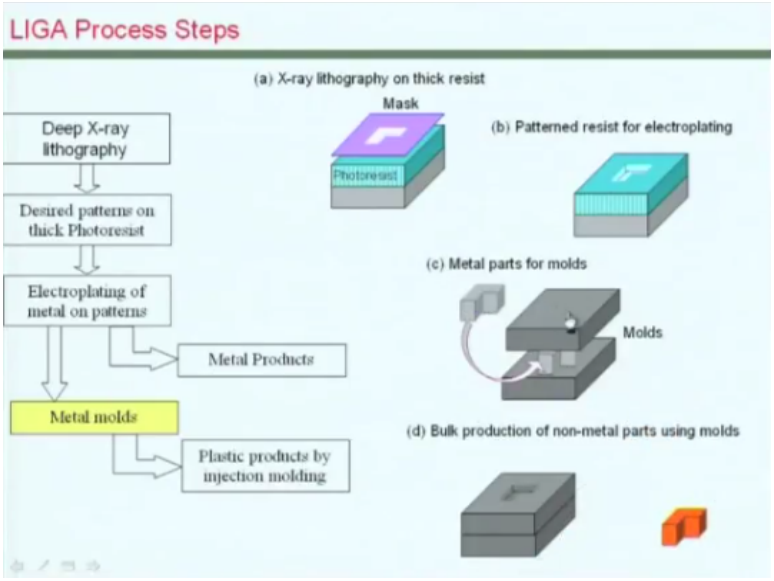

How does LIGA work? We use as I said X-ray lithography, why X-rays? Compared to the optical lithography, this can go deeper into the resist, so we can use the thick resist layer which could be patterned by this X-ray lithography. Obviously the mask that you would use should also be different to enable the X-rays being used for this purpose. So the desired patterns are formed first on this resist. This resist in fact sits on a metalized let us say wafer.

So after it is patterned we essentially have this cavity formed. We use electroplating to build the metal parts within this cavity that is there. Then use this metal, if we can use it as actually the metal products or we can use this metal molds essentially combine with plastics to you know bulk produce parts like this. It is worthwhile to in respect on this approach compared to the silicon approaches that have seen previously.

There are several key differences, one it uses the X-rays for the lithography, second it creates parts in numbers by a kind of molding or electro plating. Both these are different, but still the initial parts, the moulds themselves where created by processes which are very similar to what is used in the silicon fabrication. Once again the mask that we use should be different because you know it has to withstand the X-rays.

Obviously, the X-ray based lithography is far more expensive than the optical lithography, which is in turn compensated during the bulk production steps because it is not involved there,

essentially this creates somewhat like the mask that you eventually used in a typical photolithography process. We create the molds by the X-ray lithography. So it is used less frequently as compare to the volume production approach, but still this could be used in bulk batch production and hence the approach is somewhat similar to the previous approach that we have seen before. So with this, because we use X-ray for the lithography, we can have parts which have high vertical dimension.

So essentially by changing this one step from optical lithography to X-ray lithography even though it is the expensive preposition, one can build geometries which are relatively thick.

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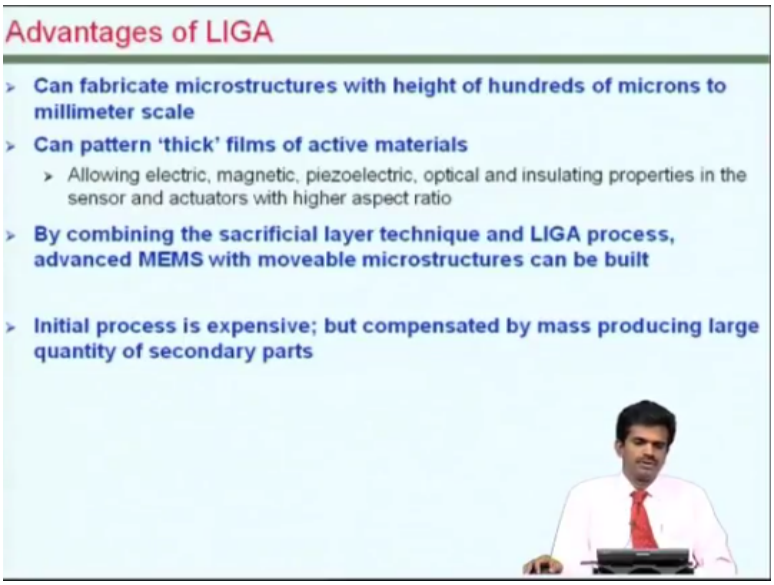

So advantages of LIGA process would be that one can build you know even up to 100 of micron thick microstructures which could be patterned and this can even be combined with surface micro machining and other conventional MEMS based approaches for building really useful Microsystems. The point to note is that the X-ray lithography process which is the first step is fairly expensive, but this is compensated by the mask production of the large quantities of those secondary parts that were formed.

So you know this is one of the early approaches for building thick structures.

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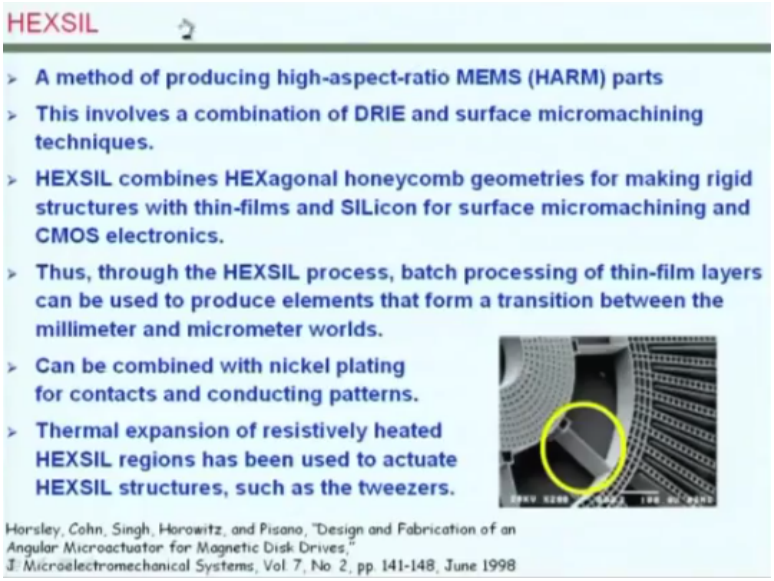

The next approach again fairly established for building a high aspect ratio microstructures is known by the acronym HEXSIL which has this hexagonal honeycomb like geometries on silicon or polysilicon which could be, you know, the process steps are somewhat similar to micromachining and it is compatible with CMOS based electronic processes. So this is a truly batch processing based approach.

But it makes you know truly vertical geometries as you see a motor kind of geometry here which has been fabricated by this approach. It essentially combines again nickel plating for creating this conducting structures. It can be used to build geometry such as micro tweezers.

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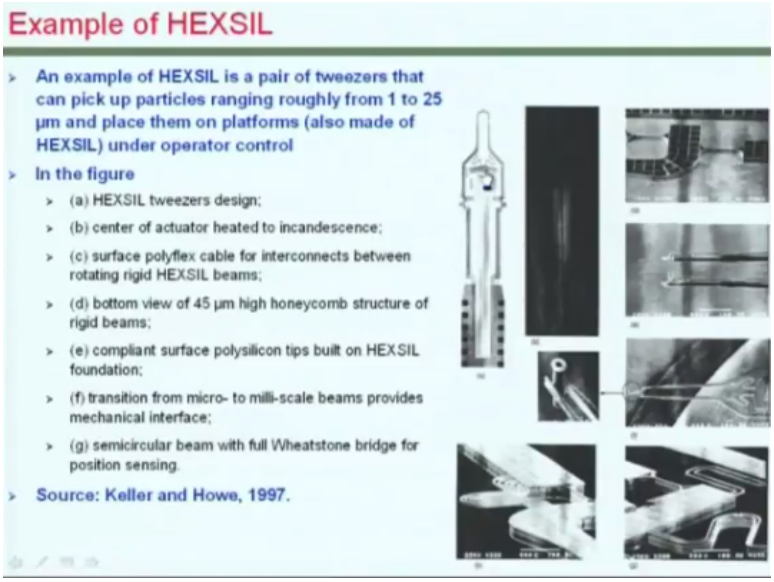

Fairly long and thick, vertically thick kind of geometries could be built by this approach. Obviously from the Mesoscale or large-scale geometries that you see when you would need such long beams you need to provide sufficient mechanical support and which is essentially provided by those honeycomb structure. So these could be fabricated by the geometries such as this could be fabricated by the process steps that are developed well over decade ago.

So you know when geometries such as this are built, it could be you know even used as a thermal actuator so that it could move and when we built such thick geometries as I mentioned, you can how fairly long geometry. What you see here is the bottom view of this honeycomb structure which essentially retains the polysilicon structure, a long polysilicon structure intact. So this HEXSIL approach developed is also a very effective way of making thick geometries on silicon.

You will see that it is possible to built similar or even thicker geometries by using non-silicon materials. We will discuss that in another lecture separately and thank you for listening to this.