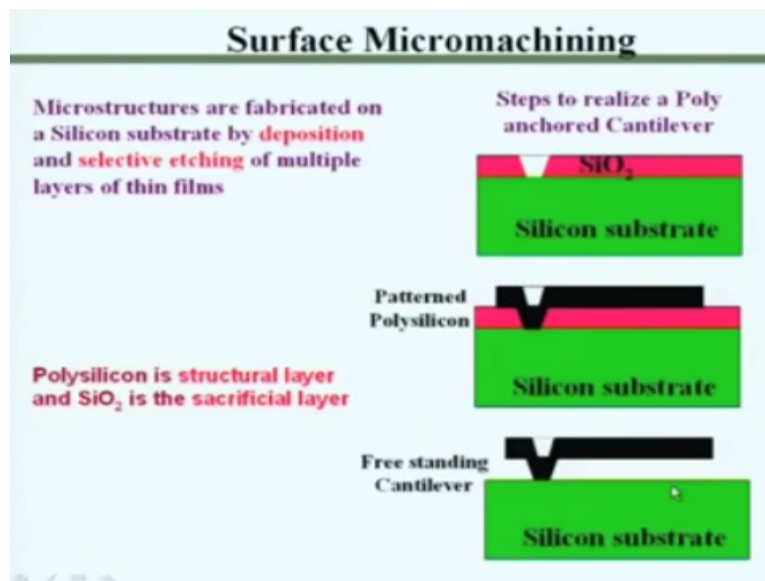


Micro and Smart Systems
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Indian Institute of Science – Bangalore

Lecture – 10
Surface Micromachining of Microstructures

Good morning, my name is Vinoy, I will be talking to you today about one of the conventional approaches for building microsystems known as surface micromachining.

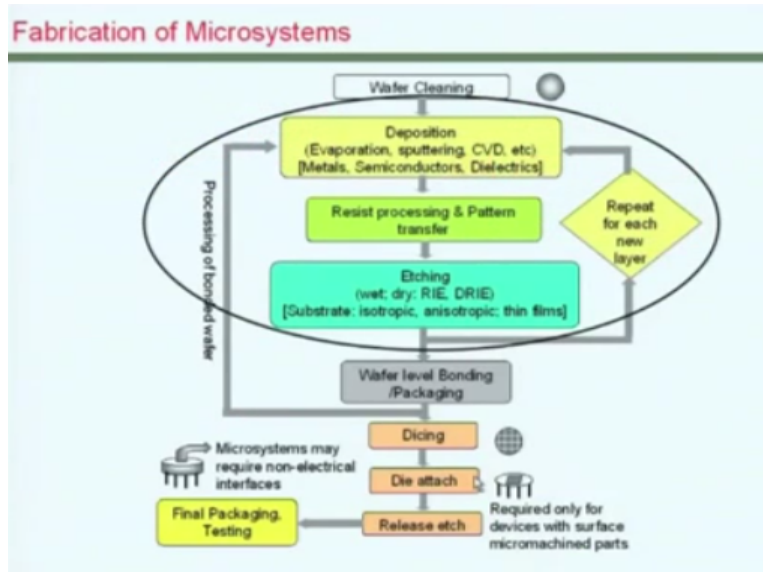
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In surface micromachining what we do is that we build structures like this cantilevers, beams and other structures on top of the silicon wafer. To do that we will have to go through several process steps of depositing silicon dioxide as you see here depositing polysilicon which is going to be the structural material in this context and then patterning both of these. The polysilicon in this particular instance is going to be the structural material for the cantilever and hence that is called the structural layer.

Silicon dioxide in this instance is working as a dummy material during the deposition of polysilicon and later after the structure is defined and hardened, it has going to be removed and hence silicon dioxide in this instance is called sacrificial layer.

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So as you could see the process steps required for the fabrication of microstructures like this is, know very much structured, ordered and we can sort of say that involves these steps in a repeated sense. Steps such as deposition of thin films, pattern transfer and then etching of these thin films, we need to organise these steps and hence surface micromachining would involve several of these processes.

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Process Steps

- **Deposit** or Grow thick silicon dioxide layer on the top surface of Si wafer.
- **Deposit** photoresist by spin coating and pattern transfer by UV lithography.
- Develop photoresist to expose regions of silicon dioxide for etching. As in **lithography**, the resist is baked to withstand the etching step that follow.
- Remove silicon dioxide from those areas at which the cantilever beam (polysilicon) anchors on the Si wafer. This involves coating with photoresist, its exposure, developing, **etching** of oxide and dissolving the photoresist.

Deposit polysilicon all over theon the surface by **CVD process**. This is doped to change its etch characteristics and conductivity. The beam area is defined by patterning through steps similar to that followed for etching oxide.

- **Dope, pattern and harden** polysilicon layer to form the cantilever beam. Patterning of polysilicon invoves coating with photoresist, exposure, developing, **etching of polysilicon** and dissolving the photoresist.
- Remove SiO₂ sacrificial layer by **release etch**.

If we come back and look at it once again, we can say that the process steps would start from the deposition of silicon dioxide on top of the silicon wafer. Then adding a photoresist layer, according a photoresist possibly by and usually by spin coating so that you know pattern transfer by lithography can be performed and then you know, we need to define the silicon dioxide for example to define the anchor for the structure to follow.

So that it would stick well to the surface of the silicon wafer itself so that it has to be done by etching of the outside for their own the structure itself will have to be deposited. And you know it has to be hardened to a certain extent and then we need to etch so that it takes the shape. So a number of these process steps are required for the successful completion of the surface micromachining of microstructures.

So the final step is the removal of the sacrificial silicon dioxide layer by a step which is usually known as the release etch by during this step the structural polysilicon layer is essentially released and it is free to move and hence it is called release etch. We will quickly go through the steps involved in the fabrication of such microstructures.


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Thin films used in MEMS

- > Thermal silicon dioxide
- > Dielectric layers
 - > polymeric
 - > ceramic
 - > silicon-compound
- > Polycrystalline silicon
 - > poly-Si
- > Metal films
 - > predominantly aluminum
- > Active Materials
 - > Ferroelectrics
 - > Piezoelectrics
- > Usually thin film materials may have multiple functions

Role of Thin films

- Structural
- Sacrificial
- Dielectric
- Semiconductor (epi-layers)
- Conductor



The unit processes required as I mentioned include deposition of thin films which could be done by physical vapour deposition or chemical vapour deposition. Physical includes techniques such as you know sputtering or PLD or other similar techniques. Chemical is CVD like LPCVD which is low pressure or PECVD or similar techniques. If structures are made of metals and if they are required to be thick, electroplating may be required.

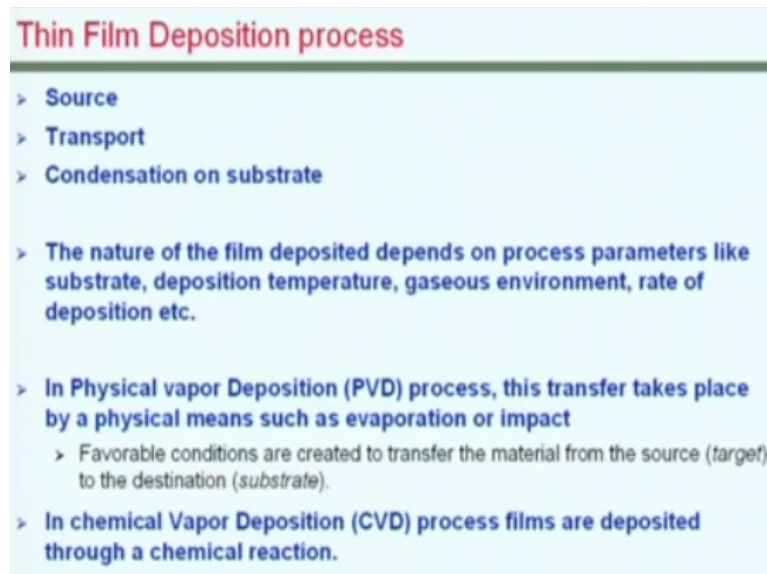
If structures are made of materials such as SU-8 possibly if this can be done by spin coating. As you have seen in the previous slide, it may be required to dope various layers used in making microstructures like this and one of the reasons is that when we add these dope pens the structure obviously get changed and that result in significant changes in some cases of the etch characteristics of those layers.

So it is possible by adding a little dopant the layers the thin film layers chemical activity could be significantly affected. And obviously pattern transfer and etching are required for the completion for the definition of those structures as well as for their release. Thin films used in MEMS in general are of various types and coming from various materials types and various applications.

Talked about structural material, structural layer the example that we saw was polysilicon, talked about sacrificial material the example was silicon dioxide in this particular exam in this case. And for other parts of the device these materials may have other rows as well. We have a number of dielectric layers can use polysilicon, polycrystalline silicon very effectively for building structures in microsystems.

Metal films are also useful in building microstructures as well as for defining electrodes and contacts and other purposes. In several micro systems including sensors smart materials such as ferroelectrics, piezoelectrics are also useful in their effective functionality.

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The diagram is a light blue rectangular box with a title 'Thin Film Deposition process' in red text at the top. Below the title, there is a list of bullet points in blue text. The first three points are 'Source', 'Transport', and 'Condensation on substrate'. The fourth point is 'The nature of the film deposited depends on process parameters like substrate, deposition temperature, gaseous environment, rate of deposition etc.' The fifth point is 'In Physical vapor Deposition (PVD) process, this transfer takes place by a physical means such as evaporation or impact', which has a sub-bullet point 'Favorable conditions are created to transfer the material from the source (target) to the destination (substrate)'. The sixth point is 'In chemical Vapor Deposition (CVD) process films are deposited through a chemical reaction.'

Thin Film Deposition process

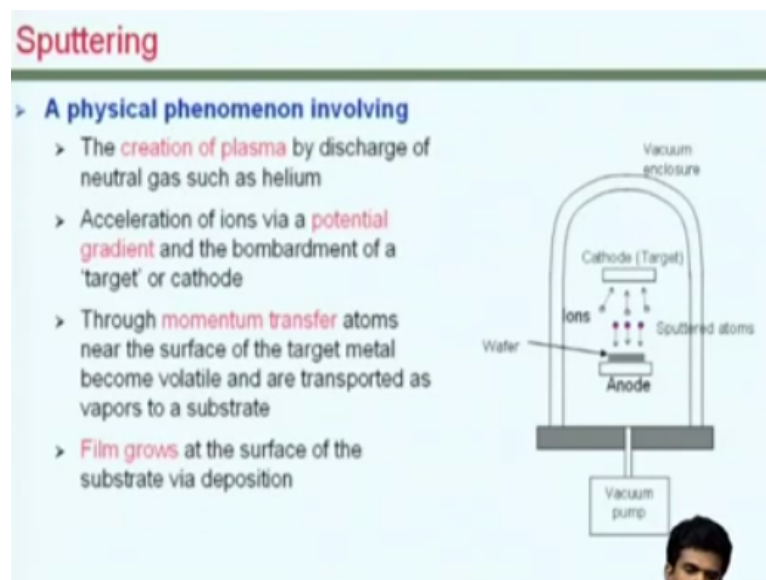
- > Source
- > Transport
- > Condensation on substrate
- > The nature of the film deposited depends on process parameters like substrate, deposition temperature, gaseous environment, rate of deposition etc.
- > In Physical vapor Deposition (PVD) process, this transfer takes place by a physical means such as evaporation or impact
 - > Favorable conditions are created to transfer the material from the source (target) to the destination (substrate).
- > In chemical Vapor Deposition (CVD) process films are deposited through a chemical reaction.

So thin films have varied users in the context of microsystems. Thin film deposition process essentially involves transferring the atoms or molecules of this material from a source and transporting it and condense it in condensing these on to the substrate. The quality and performance characteristics of the film thus depositor would certainly depend on the process parameters such as the substrate used and whether it is heated, the deposition temperatures, the gaseous environment.

And then you know the rate at which the film is being deposited. There could be physical vapour physical techniques for deposition which is essentially transferring from a source to the substrate which is essentially the destination, the surface of the substrate and this is only a physical means there is no chemical reaction taking place in this instance.

Alternately in many cases we use chemical vapour deposition so that the thin films are formed from gaseous input, gaseous materials and the precipitate of the chemical reaction is essentially the required material. So what we need to ensure in both these cases is that you know the required process conditions are maintained and optimized so that a smooth and continuous film of uniform thickness and required thickness can be formed for the applications in hand.

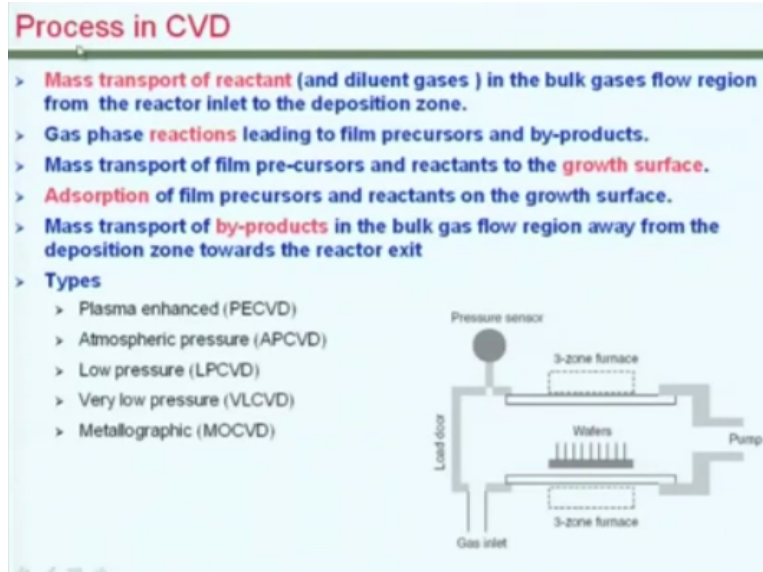
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One of the common example for physical vapour deposition is known as sputtering. In this case what is done is that we create plasma and energized ions would hit the cathode and we keep the source material which is known as the target at the cathode and when these ions hit the source material atoms get displaced and due to the potential difference between the cathode and anode those atoms would be, you know towards the wafer kept at the anode.

So to ensure that we have a useful creation of ions we need to make sure that it is within an vacuum chamber and the film will essentially grow on the wafer.

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In the case of CVD chemical vapour deposition on the other hand, the reactants are essentially you know in the gaseous form. Obviously when it is in the gaseous form it is easier to control their purity under various factors and hence the films formed by CVD are usually superior in quality. So in CVD we need to carry these reactants and make sure that the reactions take place and the products of those reactions would stick to the surface and grow as a film.

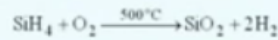
So to do that they have to you know adhere to the surface and as well as the by-products of the reaction should be in the gaseous form and they should be taken out. So the inlet and there are a number of wafers and we have to ensure the process conditions including temperature, pressure etc are maintained and the products of the reaction goes out. There are several variants of chemical vapour deposition. The quite often we talk about PECVD or LPCVD in the context of microsystems.

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LPCVD of Si Compounds

CVD is used to form SiO_2 layers that are much thicker in relatively very short times than thermal oxides.

SiO_2 can be deposited from reacting silane and oxygen in LPCVD reactor at 300 to 500°C where



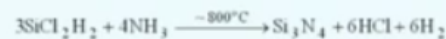
SiO_2 can also be LPCVD deposited by decomposing dichlorosilane



SiO_2 can also be LPCVD deposited by from tetraethyl orthosilicate (TEOS or $\text{Si}(\text{OC}_2\text{H}_5)_4$) by vaporizing this from a liquid source,

Si_3N_4 can be LPCVD or PECVD process.

In the LPCVD process, dichlorosilane and ammonia react according to the reaction



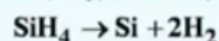
And the silicon compounds such as silicon dioxide and silicon nitride can be formed by using LPCVD. In LPCVD we use silane and oxygen and you keep the, you know maintain the temperatures at obviously at the low pressure and to form the oxide filler. It is also possible to use dichlorosilane to form silicon dioxide filler.

There are ways of getting silicon nitride either by LPCVD or PECVD, in this here what we see is an example in which silicon nitride is formed from dichlorosilane at 800 degree centigrade. So it is possible to create to form silicon compounds starting from different materials using LPCVD techniques.

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Polysilicon

- > Polysilicon comprises of small crystallites of single crystal silicon, separated by grain boundaries.
- > This is also used in MEMS and microelectronics for electrode formation and as a conductor or high-value resistor, depending on its doping level (must be highly doped to increase conductivity).
- > When doped, resistivity 500-525 $\mu\Omega/\text{cm}$
- > Polysilicon is commonly used for MOSFET Gate electrode:
- > Poly can form ohmic contact with Si.
- > Easy to pattern
- > Carried out at low pressure (200mTorr to 1000mTorr) by pyrolytic decomposition of silane (SiH_4), in the temperature range 500-625°C



- > Most common low-pressure processes used for polysilicon
- > Pressures between 0.2 and 1.0 Torr using 100% silane.

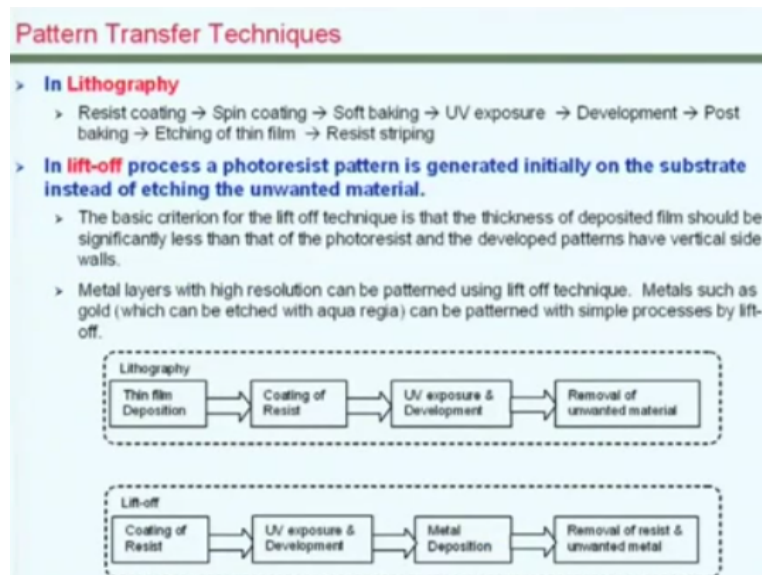
It is also possible to form the polycrystalline silicon required for the structural material by LPCVD technique. Polycrystalline silicon are usually which is usually known as polysilicon

comprises of small crystallites of silica and with grain boundaries. So it is not a single crystal silicon from one end to the other, there are these grain boundaries of which are essentially you know a sort of defects in the crystal structure.

This is a very useful material in MEMS as you have seen in the previous example it is a good material for forming structures and these structures can be you know, the conductivity of these structures can be controlled by doping the silicon. So in a sense we do not necessarily need to add another metal layer for forming electrodes on these layers. So by doping polysilicon we can that itself would work as a useful electrode in many practical applications.

Obviously, polysilicon is also used in MOSFET for MOSFETs and other Siemens technologies for various applications and poly can form a good ohmic contact with silicon and is easy to pattern and has various applications. It is deposited by LPCVD by the decomposition of silane at a temperature range which is very close to excess of 600 degrees in most instances. This is the most common process for the deposition of polysilicon for these applications.

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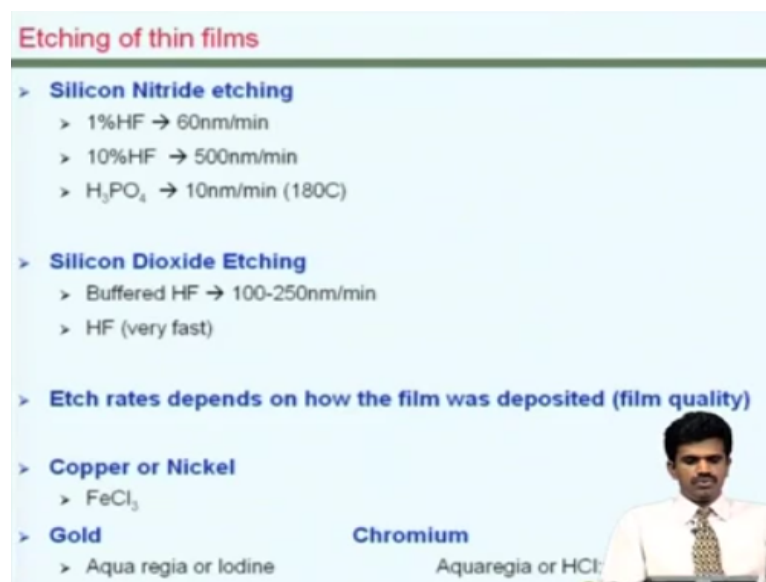


In order to pattern these materials, usually lithography is used. Lithography is consists of several process steps. You need to first coat the surface with a resist material which is usually done by spin coating and a soft baking step is required before the UV exposure so that the film is attached to the surface reasonably and after exposure, it is developed and then a post baking step is performed so that during the etching of the thin film that does not go away and finally you would want to remove the resist by stripping or ashy.

In lift-off on the other hand the sequence of events is marginally modified. As you could see from here the film that is to be etched is deposited before pattern transfer in lithography based steps whereas in lift-off approach we start with the resist which is developed and after the resist is developed the target film is deposited and since there are steps between the surface and the top surface of the resist where it is remaining.

We make use of the step and possible undercuts in the resist while it is developed. We can have a discontinuity between the metal films sitting on top of the resist and on the surface of the wafer and when the resist is removed by dissolving it in organic solvents the metal film sitting on top of the resist will go away and hence we will have a patterned metal film realised. Both these techniques could be used for microsystems applications.

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Etching of thin films

- > **Silicon Nitride etching**
 - > 1%HF → 60nm/min
 - > 10%HF → 500nm/min
 - > H_3PO_4 → 10nm/min (180C)
- > **Silicon Dioxide Etching**
 - > Buffered HF → 100-250nm/min
 - > HF (very fast)
- > **Etch rates depends on how the film was deposited (film quality)**
- > **Copper or Nickel**
 - > FeCl_3
- > **Gold**
 - > Aqua regia or Iodine
- > **Chromium**
 - > Aqua regia or HCl

In lithography, as I mentioned it involves the etching of thin films. Silicon nitride can be etched by phosphoric acid or to some extent is also possible by HF at various concentrations. We can etch silicon dioxide using HF solutions. This edge rates of these would depend on how the film itself was deposited in a sense the quality of the thin film. For metals such as copper, ferric chloride could be used for gold and chromium aqua regia could be used for the etching.

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Doped regions

- > For doping of semiconductors, controlled quantities of impurity atoms are introduced into the selected regions of the surface through masks on the top of the wafer.
- > Diffusion and Ion implantation are common methods for this.
- > Used as etch stop layers
- > N and P regions can be formed for active semiconductors
- > Diffusion

- > Wafer placed in a high temp furnace and a carrier gas is passed. Boron and phosphorous are commonly used dopants
- > The deposited wafer is heated in a furnace for drive in, oxidising or inert gas to redistribute dopants in the wafer to desired depth
- > Silicon dioxide is used as the masking layer

Phosphorus Diffusion

Make	Tempress
Temperature Range	800-1200 °C
Dopant Source	POCl ₃
Bubbler Gas	Nitrogen (0.4 ltr/min)
Carrier Gas	Nitrogen (4 ltr/min)
Flow rate of Oxygen	0.6 l/min

Boron Diffusion

Make	Tempress
Temperature Range	900-1200 °C
Dopant Source	Boron Nitride Disc
Process Ambient	Nitrogen
Flow rate of N ₂	4 ltr/min

I have mentioned that the polysilicon layer will have to be doped. Doping is very common procedure in building integrated circuits. What we do is that we add N or P type impurities onto the semiconductor. There are 2 common techniques for doping, one is known as diffusion and the second is ion implantation. In diffusion the wafer is placed in a high temperature furnace with the carrier gas and which will carry the boron or phosphorus as the case may be and after this is deposited on the surface of the wafer.

These are driven in and essentially diffused into the bulk of the wafer to the required thickness by controlling the process parameters at this stage. Silicon dioxide is usually used as a masking layer for diffusion purposes. A typical process parameters for diffusion of phosphorus and boron are listed in these tables. So you could see the source material would be in the form of a disc and we carry nitrogen, we use nitrogen carrier gas in both these cases.

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Surface Micromachining

> Structural layer

- > A layer of thin film material that comprises a mechanical device.
- > This layer is deposited on the sacrificial layer, and then released by etching it away.

> Sacrificial Layer

- > A layer of material that is deposited between the structural layer and the substrate to provide mechanical separation and isolation between them.
- > This is removed after the mechanical components on the structural layer are fully formed, by release etch. This approach facilitates the free movement of the structural layer with respect to the substrate.

> But of course, these materials should be chemically distinct..

- > So that suitable etchant can be selected to remove the sacrificial layer without removing the structural layer AND the substrate etc.



So in building microstructures using surface micromachining, we have a structural layer which is a thin film material and that forms the mechanical device. We also have, this layer is essentially deposited above the sacrificial layer. The sacrificial layer in this case in this example it was SiO_2 . This was deposited before the structural layer so that there is a separation between the substrate and the structural layer and it also, it is obviously removed during the step called release etch.

After release etch, the structure should remain intact. There are several new answers to be taken care of to build successful structures by these. It is not just looking at all those unit steps that we have seen so far. First of course is that the chemical that you are using for removing the silicon dioxide or the sacrificial layer in a more general sense, should not significantly affect the polysilicon as a structural layer, silicon as a substrate in these examples. So we need to identify one suitable chemical for this purpose.

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Detailed Process Steps in Surface Micromachining

> Sacrificial Layer deposition and etching

- > LPCVD of PSG 2μm
- > PSG by adding phosphorous to SiO₂ → improved etch rate
 - > Controlled window taper
 - > Easier to make poly layer
- > PSG is densified at 950°C for 30min
 - > Conductive (phosphorous goes up as dopant)
 - > Windows in the base layer for anchoring structures.



And we can also do this by suitably choosing the quality and composition of the layers that we are using. For example, the sacrificial layer used is an LPCVD, phosphorus added SiO₂ so that it is much more easier to etch it at you know and so at the etch process become much quicker. This phosphorus silicate glass is densified so that when we deposit the structural layer, you get a good surface to begin with on which the polysilicon could be deposited.

So this phosphorus in this can be used also to dope the polysilicon later. We also need to pattern these to form anchors between anchors for the structural layer to the surface.

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> Deposition of structural material by CVD (or sputtering – PVD)

- > Poly Si : LPCVD (25-150 Pa) in a furnace at 600°C from pure Silane

$$\text{SiH}_4 \rightarrow \text{Si} + 2\text{H}_2$$
- > Typical process conditions: 605°C; 73 Pa (550 mTorr); Flow rate : 125 sccm
- > Deposition rate: 100Å/min.
- > To make the structure conductive, dopants are introduced
 - > Along with silane or by ion implantation.
- > Structures are patterned by RIE in SF₆ plasma
- > Selective etching of spacer material
 - > Structures are freed from substrate by undercutting of the sacrificial layer
 - > Immersed in HF solution to remove sacrificial layer
 - > PSG is removed by concentrated/ dilute / buffered HF
 - > To shorten etch time, extra apertures are usually provided in the structure.
 - > Thicker layers etch faster.

The structural layer is also, is usually formed by CVD. It can also be formed by sputtering. In CVD as I mentioned earlier, we use LPCVD and we use silane for this purpose. To make the structure conductive these dopants are introduced and that means the polysilicon conductive

and hence it can work as electrode by itself. Usually structures are formed by what is known as a reactive ion etching which is a dry etching process, we will talk about it a little later.


It is also possible to form these by you know etching, various etching techniques and finally the spacer material which is the sacrificial layer is to be removed and you should remember that this layer is in fact below the structural layer and hence a lot of care has to be taken in doing this etching. The phosphorus silicate glass used in this instance could be removed using buffered HF.

And you know to shorten the etch time what we normally do is that when there are large area structures we provide extra holes on the structural layer so that the H becomes faster and obviously if the thickness of this layer is higher that rate would be faster reason obviously is that the reagents can go through a far more, more easily when there is higher gap between the structural layer and the substrate material.

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Material Pairs

- > **Poly/SiO₂**
 - > LPCVD deposited poly as structural layer;
 - > Thermal or LPCVD oxide as sacrificial layer
 - > Oxide dissolves in HF, and not poly.
 - > Both materials are used in IC fabrication.
 - > Deposition and etching technologies are matured
 - > Material systems are compatible with IC processing
 - > Poly has good mechanical properties. Its electrical properties can be improved by doping
 - > Nitride can be used in this system for insulation
- > **Silicon Nitride/Poly-Silicon**
 - > LPCVD nitride is used as structural layer; Poly Si as sacrificial layer
 - > EDP or KOH to dissolve poly.



The material pairs used for the sacrificial and structural layer have to be chosen as I mentioned based on chemistry and based on their other properties. Poly SIO₂ pair that we have discussed about is a very good combination for many applications. We also see examples in which silicon nitride and poly silicon are used in this particular case you know nitrate is used as the structural layer and poly silicon as a sacrificial layer.

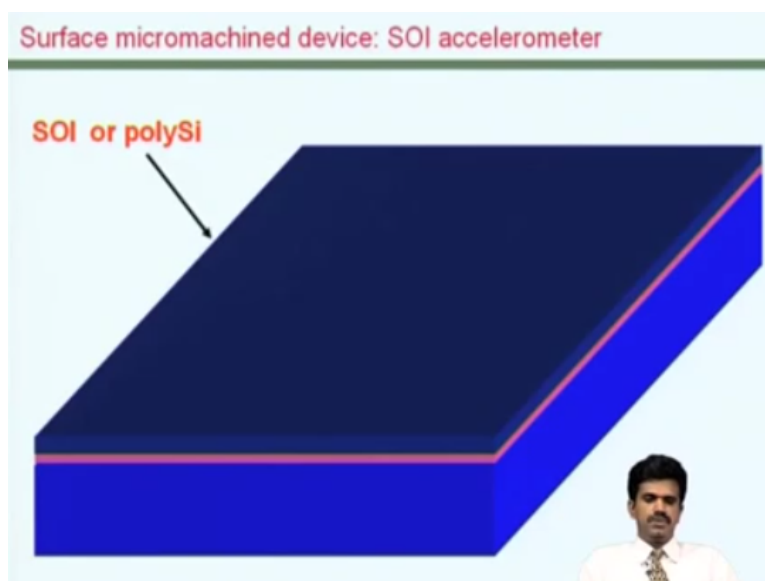
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Additional material Pairs

- > **Tungsten/SiO₂**
 - > CVD tungsten as the structural layer; Oxide as sacrificial layer
 - > HF for etchant
- > **Polyimide/Aluminum**
 - > Polyimide as structural layer, aluminum as sacrificial layer
 - > Acid based etchants to etch aluminum
 - > Polyimide has small elastic modulus
 - > Can take large strains
 - > Both can be fabricated at low temperatures <400°C
- > **Other possible structural materials :**
 - > Al, SiO₂, Si₃N₄, Silicon oxynitride, polyimide, diamond, SiC, sputtered Si, GaAs, Tungsten, a-Si:H, Ni, W

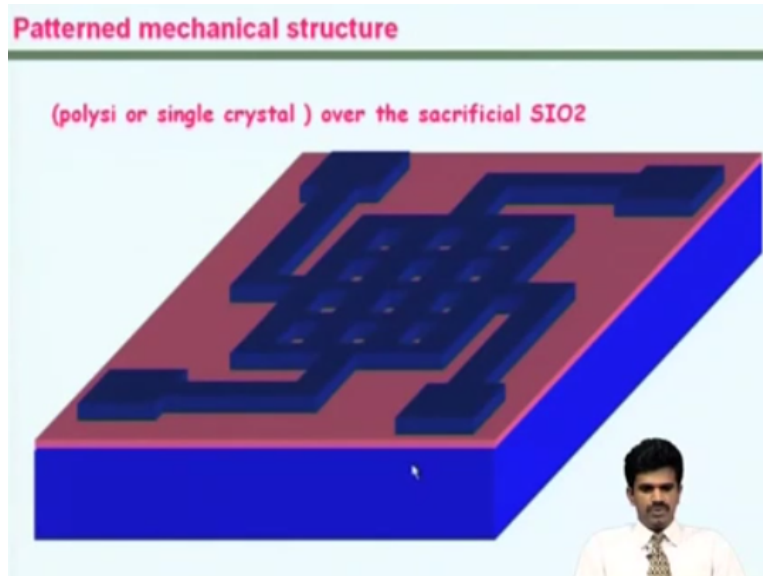
You can also see tungsten or polyamide or other metallic films used as the structural layer. Essentially, we need to make sure that the release etch, the final etching of the sacrificial layer is under control and is far easier and does not affect the remaining structure, the structural layer and the substrate material.

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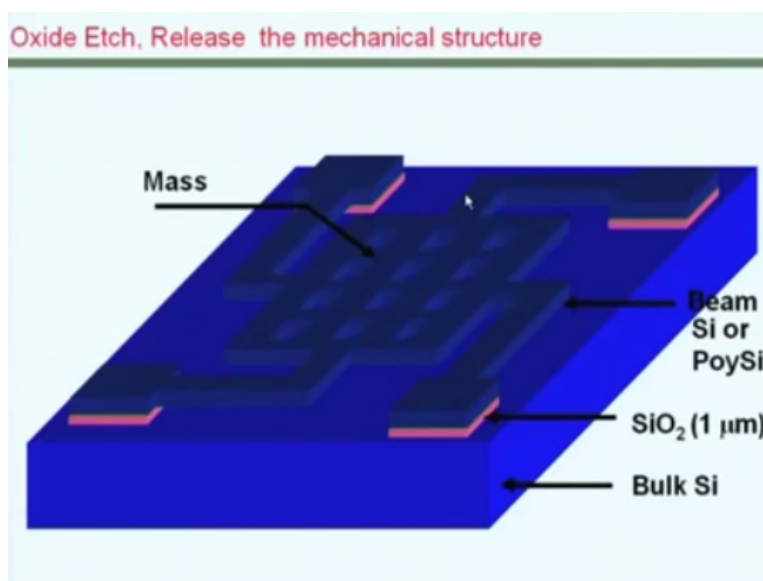
You see one more example of microstructure fabricated using in this case using an SOI. It could also be done for a similar configuration as you have seen previously. In SOI, what we have is an intermediate outside layer between 2 silicon layers.

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First the top silicon layer is patterned and as you could see these large holes which are essentially there to help in etching the silicon dioxide later.

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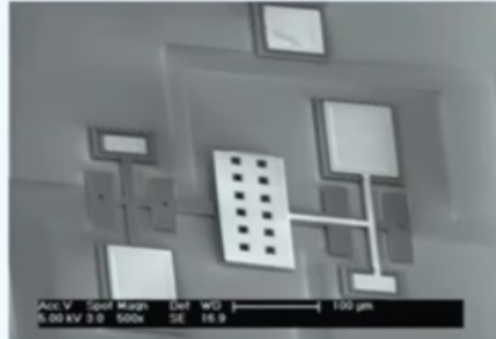


And then the outside we need this as etched by this release etch and was then we need to add the electrodes for the conducting pads in this case.

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Removal of Sacrificial Material

- > Removal of sacrificial layer below a large area structure is difficult.
- > Etch holes are provided to improve etch characteristics



The inclusion of those holes are essential in building microstructures especially those involving large areas and should be freestanding. These are typically called etch holes and they should typically have reasonably large area so that the reagents can go in through them and react with the sacrificial layer beneath the plate on the top.

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Stress in Thin film

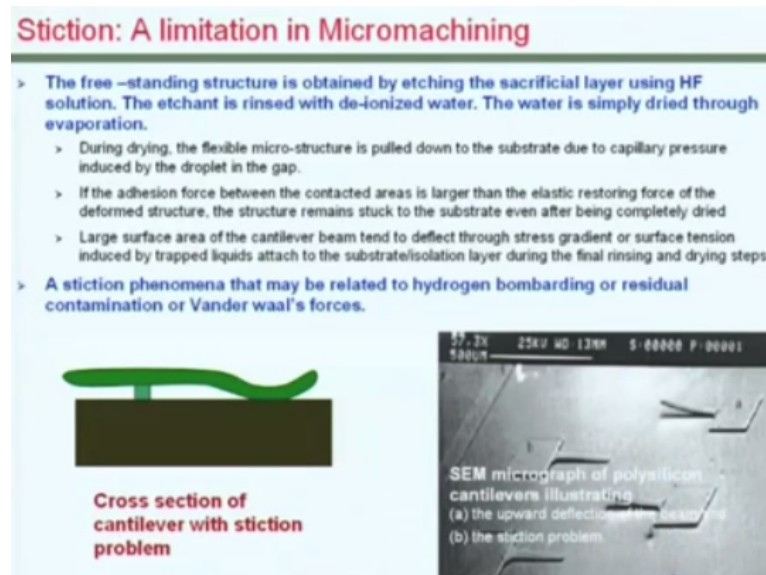
- > **Stress can be due to**
 - > Mismatch of thermal expansion itself
 - > Non-uniform plastic deformation
 - > Substitutional / interstitial impurities
 - > Growth process
- > **It causes**
 - > Film cracking
 - > Delamination
 - > Void formation
- > **Special cases**
 - > Al films are usually stress free
 - > Tungsten accumulates more stress when sputter deposited

One another critical aspect that should be looked at in choosing the pairs of materials is the stress in thin film. Stress is developed due to mismatch of thermal expansion coefficients of these films. It can also be caused due to non-uniform deformation of these layers or impurities or by the growth process by itself. It can cause film cracking, delamination or even formation of voids.

There are some interesting special cases in thin films technology which for example in

aluminium films are usually stress free. So the stress that is developed in the films can in fact bend the structures significantly. It can also cause delamination or peeling off of films. So this has to be engineered properly during the deposition process so that the structures would remain intact especially after releasing.

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Another important aspect in the context of building microstructures by surface micromachining is known as stiction. The freestanding structures that we would expect to get after the release, after removal of the sacrificial layer may fall down and stick with the surface if the processes are not performed well.

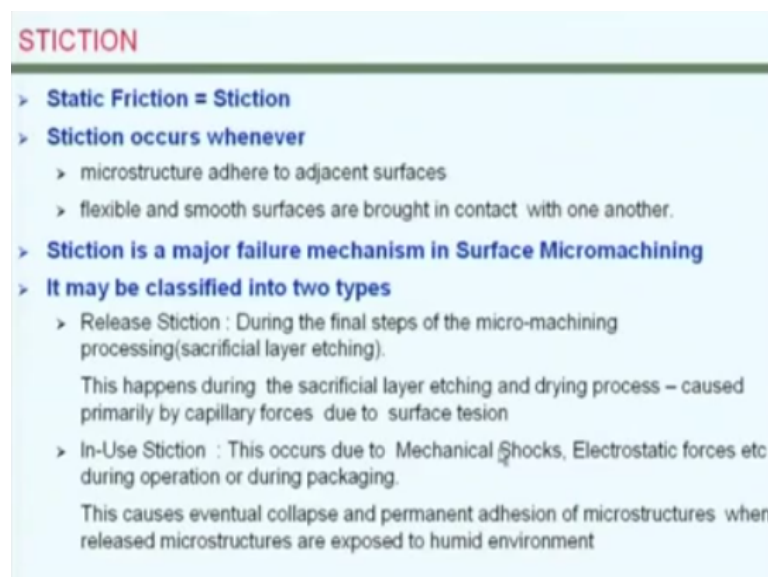
The reason is that when we etch the silicon dioxide in were in chemicals, it is possible that a part or some droplets of those liquids remain trapped in the small gap between the structural layer and the substrate. When we try to dry them what happens is from the surface of this bubble or these drops atoms or molecules go away but due to the surface tension and the adhesion between the water and the structures, the drop would remain attached to both top and bottom surfaces.

On top of the drop is the structural layer below the drop is the substrate by itself. So as we continue to heat the drop size would of course shrink down but what would happen is that when it becomes very small and not high enough, it pulls in the structure because of the adhesion force between the drop and the structure. Eventually, the drop may go away if you heat but by that time the structure would have come in perfect contact with the substrate itself.

Then what would happen, what we have is our 2 very smooth surfaces in continuous contact. This is like 2 glass plates in contact. If you try to remove them by applying a force away from each other it is almost impossible to do that. We need some kind of shear force separate this. This is due to the surface level attraction forces and hence because of that this structure would remain attached to the surface, the wafer surface and it is almost impossible to remove it in to displace it without damaging it.

So stiction is a serious limitation in micromachining if the processes were turned the way we talk so far. You could see on the example on the right side several microstructures have sort of you know slipped in and remain attached to the substrate by itself and it is extremely difficult to leave them out to make them freestanding.

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STICTION

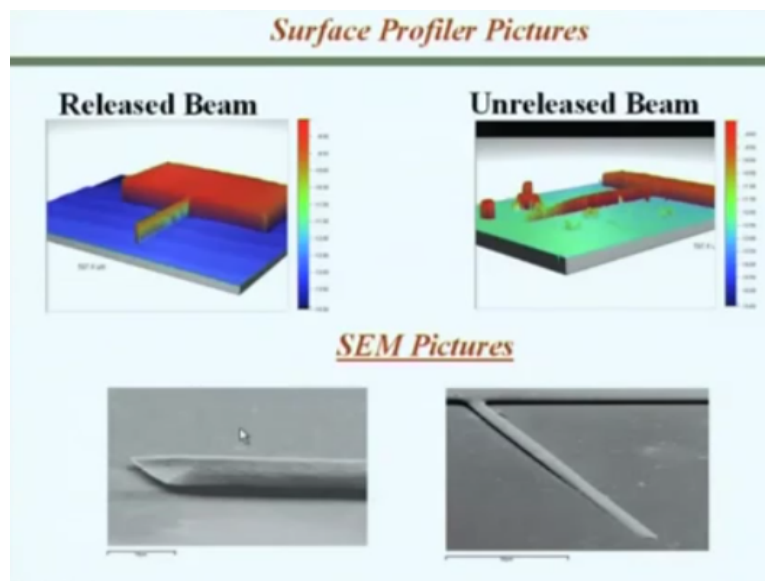
- **Static Friction = Stiction**
- **Stiction occurs whenever**
 - microstructure adhere to adjacent surfaces
 - flexible and smooth surfaces are brought in contact with one another.
- **Stiction is a major failure mechanism in Surface Micromachining**
- **It may be classified into two types**
 - **Release Stiction** : During the final steps of the micro-machining processing(sacrificial layer etching).
This happens during the sacrificial layer etching and drying process – caused primarily by capillary forces due to surface tension
 - **In-Use Stiction** : This occurs due to Mechanical Shocks, Electrostatic forces etc during operation or during packaging.
This causes eventual collapse and permanent adhesion of microstructures when released microstructures are exposed to humid environment

Stiction is therefore a short form for static friction and it occurs when microstructures adhere to each other and when there is a flexible and smooth surface in contact. As I mentioned this is a major failure mechanism. The way I had explained, the stiction happens during the release. It is also possible that these conditions are met during the operation of the micro structure, that is called the in-use stiction.

It can happen due to electrostatic forces or mechanical shocks. When you have electrostatic release, for example an RF switch. There are electrodes and when you apply a potential due to the electrostatic force, the top electrode would come in contact with the bottom and if care is not taken these may stick. This can also happen in devices such as accelerometers due to

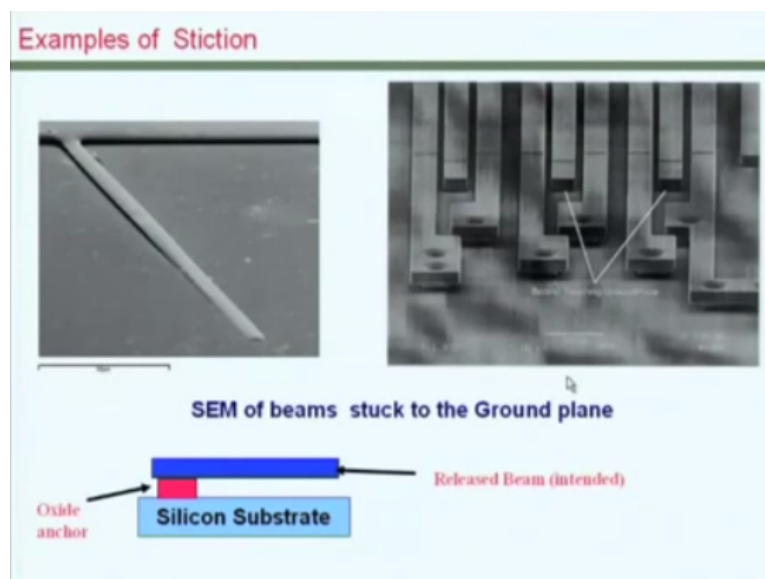
mechanical shocks. So in all these cases stiction causes collapse and almost permanent adhesion of microstructures even if they are released.

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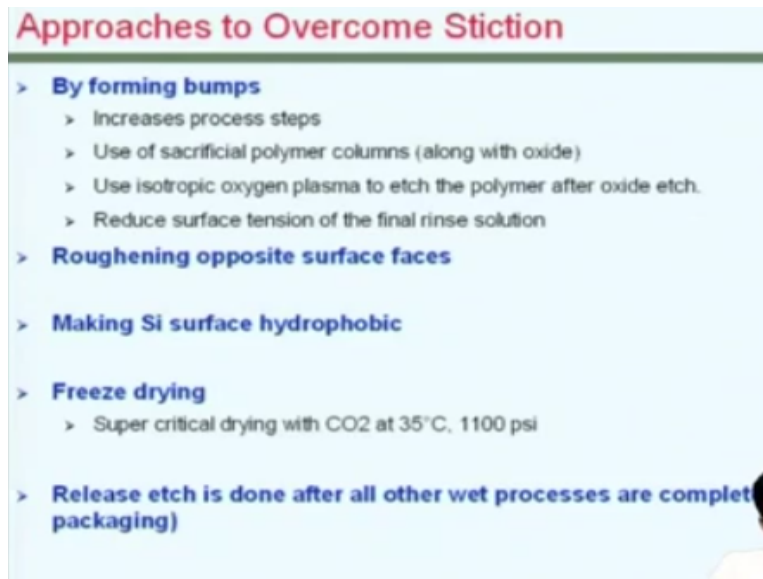
It is also shown in the images here when beam is not released properly in terms of profiler pictures or in terms of SEM pictures.

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It can also happen that some parts of the device would have come up all right but others may fail due to stiction.

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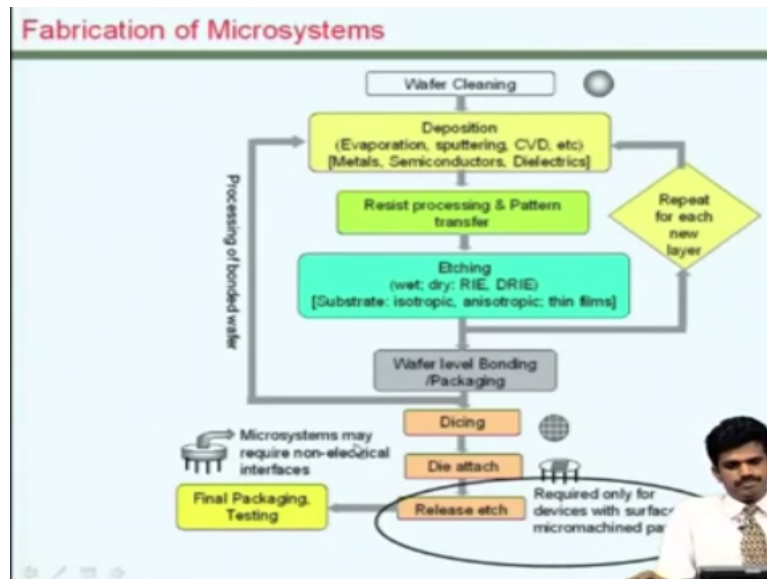


There are several approaches to avoid stiction in surface micromachine. One of the simple ways is to prevent having smooth surface contact. Simplest way could be to have bumps on either on the surfaces so that there is no surface to surface contact over a large area so that the restraining forces of those structures can pull back the small contact that may happen or these short bumps or other structures.

It is also possible to reduce or avoid stiction by roughening the surface. When you roughen the surface, the surface attraction force from the liquid to the surface could be modified and hence the chances of pulling in, the chances of you know sticking on would be far less. You can also make the silicon wafer hydrophobic so that the water droplets on stick to it.

But one of the commercially successful approaches is based on supercritical drying using carbon dioxide. I will explain this in a little detail in subsequent slides. The release etch is usually done after all the other processes are completed, why, after it is released these delicate microstructures are freestanding and hence cannot be subjected to significant forces which are usually required during agitation or other process steps.

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And hence in the process flow that you have seen, release etch is taken out and kept separately during the packaging related steps. So this is not usually done when the full wafer is handed as you may recall. During all these process steps, we keep the full wafer which may consist of several microsystems but it may not be practical to work with them beyond through this dicing step particularly if the microstructure is already released here.

And hence when there are microstructures, the release step is usually done much later unless this is strengthened by some other way. As you could see in this case release is done after dicing and attaching that to the die base, so that no more liquid processing is required in the fabrication cycle for the microsystem.

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Use of CPD to Avoid Stiction

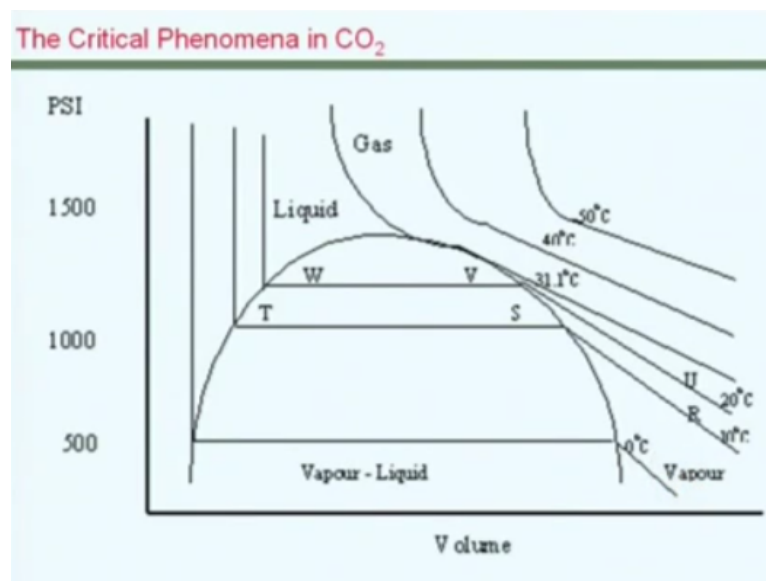
- If a liquid was heated in a closed system so that the Critical Pressure could be attained, at the Critical Temperature, any visible meniscus would disappear, the surface tension would be zero and it would not be possible to distinguish between the properties of a liquid or gas.
- We therefore have continuity of state. Above this temperature the gas cannot be liquefied by the application of pressure and strictly speaking a substance should only be classified as a gas above its Critical Temperature, below this temperature where it could possibly be liquefied by the application of pressure, it is more precisely termed a vapour.

Now let us talk about the critical point drying that I mentioned to avoid stiction. As I

mentioned when the droplet is dried the surface tension is causing the structure to collapse and this is happening because of the processes involved in drying. So what is done here is that we exceed the critical pressure and critical temperature so that there is no chance of having a surface film which would essentially cause this surface tension to exist.

To ensure this continuity a state, we need to identify materials which have critical temperature and critical pressure that could be under control.

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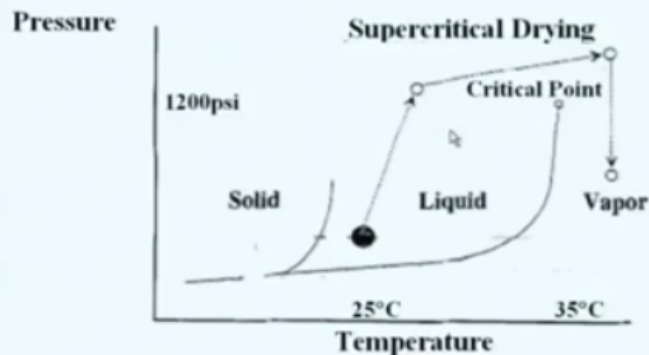
Now what is really happening when we do that. If you look at the pressure versus volume curves at various temperatures, these are called isothermal curves. As the volume is changed as the material, if you look at the curves at lower temperatures 0, 10 or 20 degrees, when you change the volume as long as it is in the gaseous form there is a corresponding change in the pressure.

But once there is a liquid vapour to liquid transformation taking place there is a sudden reduction in volume, it is a liquid and after that it is vertical because changing the pressure would not change the volume as much almost negligible. So these curves would remain vertical whereas at temperatures above the critical point, this continuous transition or continuous change would remain. There is no discontinuity with these horizontal point lines.

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Supercritical Drying with CO₂

For CO₂ supercritical region is for temperature above 31.1°C and pressures above 72.8 Atmospheres (1072 psi)



And hence for materials such as in this particular instance carbon dioxide which has a critical temperature of 31.1 degrees and a critical pressure of 1072 psi. If we have this at this pressure in excess of this pressure and temperature, the liquid to vapour transformation is taking place without a significant change in the pressures internal and external pressures.

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Super Critical Drying

For CO₂ supercritical region is for temperature above 31.1°C and pressures above 72.8 Atmospheres (1072 psi)

Super critical Drying steps:

- After HF etch, the structure is rinsed in DI water without letting them dry
- The water is exchanged with methanol by dilution
- The wafer is then transferred to pressure vessel in which the methanol is replaced by liquid CO₂ at 25°C and 1200psi
- The contents of the pressure vessel are then heated to 35°C and CO₂ is vented at temperature above 35°C (ensuring that it only exits in gaseous form)

And that is called supercritical drying. To perform supercritical drying, we have this after this HF etch, the structure is, you know cleaned by rinsing in DI water and it is exchanged with methanol by several steps. This wafer will then be transformed into a pressure vessel where this kind of pressure could be applied and then heated to temperatures so above the critical temperature.

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CRITICAL CONSTANTS

Substance	Critical Temp. °C	Critical Pressure P.S.I
Hydrogen	-234.5	294
Oxygen	-118	735
Nitrogen	-146	485
Carbon Dioxide	+31.1	1072
Carbon Monoxide	+141.1	528
Water	+374	3212

And the transformation liquid to gas transformation takes place. Look at various materials various, let us say materials and their critical temperature and pressure we could see that carbon dioxide has good advantage because the temperatures are well under control.

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In-use Stiction and methods to Overcome

- **Mechanical Shocks, Electrostatic forces etc during operation or during packaging can also cause stiction.**
 - For example, as the sensitivity of micromechanical accelerometer is increased, the stiffness of the proof mass suspension will have to be lower. As a consequence the mechanical shock required to bring the mechanical elements into contact with each other will decrease.
- **In-use stiction can also occur when released micro-structures are exposed to humid environment.**
 - Water vapor can condense and the water droplets, formed in narrow gaps present between these surfaces, exert an attractive force by pulling the microstructure toward the substrate. This causes eventual collapse and permanent adhesion of microstructures

So the stiction whether when if it is happening due to the release etch it can be avoided by using CO₂ based critical drying approach. As I mentioned, there are instances when you know the stiction happening due to the operation. For this we need to look at other approaches for their avoidance.

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Other Approaches for Reducing of Stiction

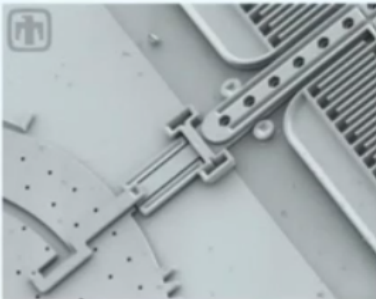
- **Reducing adhesion Energy by providing hydrophobic surface coating**
 - This can eliminate water mediated adhesion.. Weakly adhesive material such as fluorinated polymer (eg PTFE) still has a surface tension of about 20mJ/ m² . (note that an adhesion energy of 100J/m² is high enough to counter balance restoring elastic force).
- **Reducing the Geometrical area contact.**
 - This is done using bumps and side-wall spacers, side-wall-spacing, supports on substrate .
- **Increase surface roughness**
- **References**
 - Niels Tas et.al, " Stiction in Surface micromachining", *J. Micromech. Micreng.*, Vol6,pp. 385-397, 1996.
 - Chang-Jim Kim et.al., "Comparative Evaluation of Drying Techniques for Surface Micromachining" *Sensors and Actuators-A* 64, pp.17-26, 1998.
 - Lingbo Zhu et.al., "Lotus Effect Surface for prevention of Microelectromechanical Systems (MEMS) Stiction", 2005 *IEEE Electronic Compon Technology Conference*, pp1798-1801

So we can look at as I mentioned having hydrophobic surfaces, having geometries with reduced areas or increasing surface roughness.

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Examples

- **Microstructures fabricated with surface Micromachining**
- **Complex structures require dry etching techniques**
- **Note that all these can have large lateral dimensions, but relatively small "thickness"**



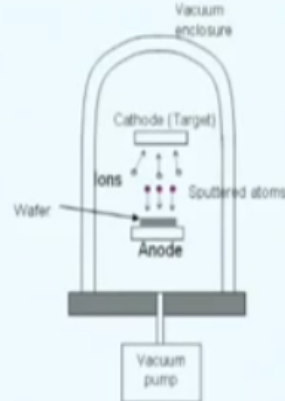
Several interesting looking complex, microstructures can be formed by surface micromachining. As I mentioned earlier, dry etching techniques are important for their successful completion. But you should also note that the vertical dimension the thickness of these structures are far less compared to the overall area of the geometry that you have here.

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Recall Sputtering

> A physical phenomenon involving

- > The **creation of plasma** by discharge of neutral gas such as helium
- > Acceleration of ions via a **potential gradient** and the bombardment of a 'target' or cathode
- > Through **momentum transfer** atoms near the surface of the target metal become volatile and are transported as vapors to a substrate



You note that in sputtering, we have these ions hitting the target kept at the cathode which displaces the atoms. We can make use of this in the plasma environment, we can make use of this to keep our substrate over here and remove material from this.

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Dry Etching Techniques

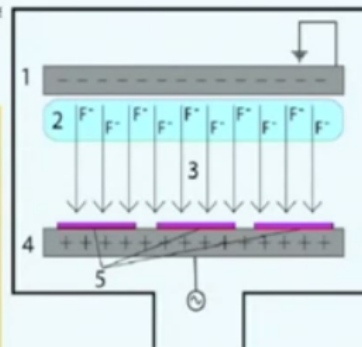
> Material removal for IC's , MEMS

- > By physical
 - > By ion bombardment
- > By chemical
 - > Chemical reaction through a reactive species
- > Or Combination

> Plasma etch

Steps involved in RIE Etching

1. Reactive etching species are generated by electron/molecule collisions
2. Etchant species diffuse through stagnant region to the surface of the film to be etched
3. Etchant species adsorb onto surface
4. Reaction takes place
5. Etched product desorbs from the surface
6. Etch products diffuse back into bulk gas and removed by vacuum



And that is what is done in dry etch. In reactive ion etching, we also make sure that the ions that are formed are also reactive so that we can bring in the selectivity aspect. It does not remove from everywhere on the wafer surface. It would only remove from parts that you would actually want. So a selective etching is possible by what is known as reactive ion etching.

So these etching species that are formed would go through and displace the atoms and hence we effectively get a etch and notice that in this step the no liquids used so there is no question

of stiction and associated problems.

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Reactive Ion Etching (RIE)

- > Wet etching causes undercut
- > Unidirectional etching is possible with RIE
- > High fidelity pattern transfer

Material Being Etched	Etching Chemistry
Deep Si trench	$\text{HBr}/\text{NF}_3/\text{O}_2/\text{SF}_6$
Shallow Si trench	$\text{HBr}/\text{Cl}_2/\text{O}_2$
Poly Si	$\text{HBr}/\text{Cl}_2/\text{O}_2$, HBr/O_2 , BCl_3/Cl_2 , SF_6
Al	BCl_3/Cl_2 , $\text{SiCl}_4/\text{Cl}_2$, HBr/Cl_2
AlSiCu	$\text{BCl}_3/\text{Cl}_2/\text{N}_2$
W	SF_6 only, NF_3/Cl_2
TiW	SF_6 only
WSi_2 , TiSi_2 , CoSi_2	$\text{CCl}_2\text{F}_2/\text{NF}_3$, CF_4/Cl_2 , $\text{Cl}_2/\text{N}_2/\text{C}_2\text{F}_6$
SiO_2	$\text{CF}_4/\text{CHF}_3/\text{Ar}$, C_2F_6 , C_3F_8 , $\text{C}_4\text{F}_8/\text{CO}$, C_3F_8 , CH_2F_2
Si_3N_4	CHF_3/O_2 , CH_2F_2 , CH_2CHF_2

Table taken from Semiconductor Devices - Physics and Technology by S.M. Sze, (pg. 440)

http://www.ee.byu.edu/clearroom/vie_etching.ppt

Hence reactive ion etching is popular. Various materials can be etched by suitably choosing the etch chemistry, the gas is present within the plasma so that the ions go and displace the required material from the surface of the wafer.

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Integration with Electronics

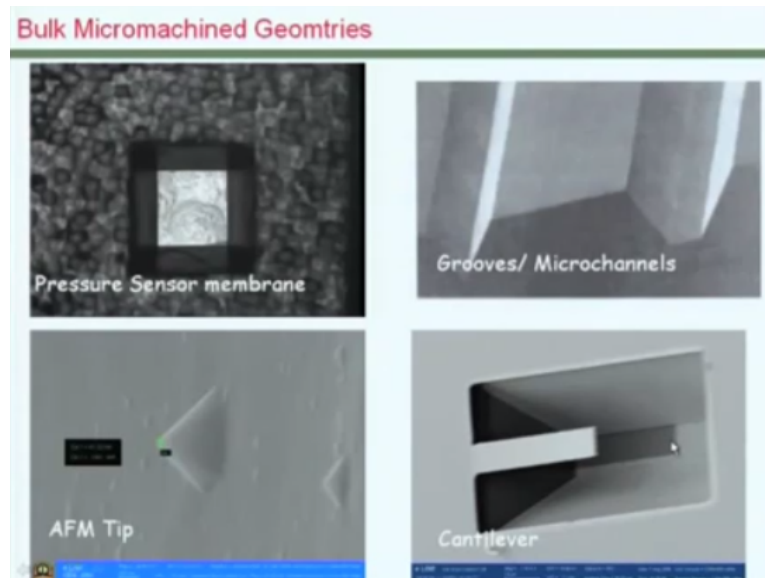
- > **CMOS First**
- > **MEMS First**
- > Notice that in both cases, electronics are integrated on chip
- > It is also possible to have the electronics in a separate die and integrate these on a package (Multi-chip modules)
- > Thicker structures and closed cavities can be formed by **Wafer bonding techniques**

These microstructures formed by surface micromachining can be integrated on wafer with electronics. It can be done by first building the electronics or in some cases, it could also be done by first building the microstructure. The process compatibility becomes critical in deciding, in choosing the order in which these process steps are performed.

It is also possible in many instances to have the MEMS alone in one chip, one die and the

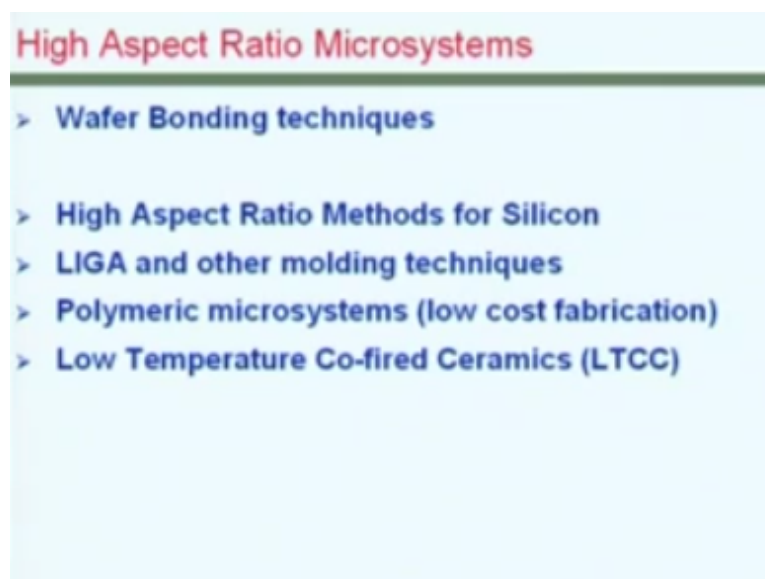
electronics separately in another day and these are packaged within what is called a multi-chip module. But in both cases, in these cases as you could see the vertical dimension is usually very small and when you really want to have large vertical structures, we would need to look at wafer bonding and other approaches for the completion of micro devices.

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These will be discussed in other lectures. One more approach which is even more popular than surface micromachining is known as bulk micromachining. In bulk micromachining, we can build cavities or in other words diaphragms or membranes or channels or cantilevers above large cavities or tips. These will be discussed in a separate lecture.

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It is also possible to build high aspect ratio microstructures by using as I mentioned wafer bonding techniques. There are several other techniques based on silicon. There are also

several molding based techniques especially for polymeric microsystems. It is also possible to use low-temperature co-fired ceramics to build microsystems. These will be again discussed in another lecture.

So I would like to conclude by saying that several microstructures, simple and even very complicated looking can be fabricated using surface micromachining processes. It consists of several process steps usually involving multiple material layers and we will see many of the other techniques in subsequent lectures. Thank you very much.