Electronic Packaging and Manufacturing
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Lecture – 24
Thermal Management 3: Thermal Resistance

Hello and welcome back to Electronic Packaging and Manufacturing course. If you recall, we were discussing thermal management and cooling strategies ok. So, in the last class rather the last two lectures, since we started discussions on thermal design and cooling, we have been talking about you know first we did a recap of their different modes of heat transfer, and then we talked about the important concepts of heat flux as well as thermal resistance.

We had solved a very simple problem, whereby we demonstrated the use of thermal resistance network in solving problems ok. So, today what we will do is that was a simple exercise that we did. So, today what we will do is we are going to extend that and look at some of the very typical nomenclatures that are used while defining thermal resistance for electronic packages, so that is going to be a concept covered for this lecture thermal resistance for packages ok.

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So, let us move onto the next slide, and let us see what we are talking about.

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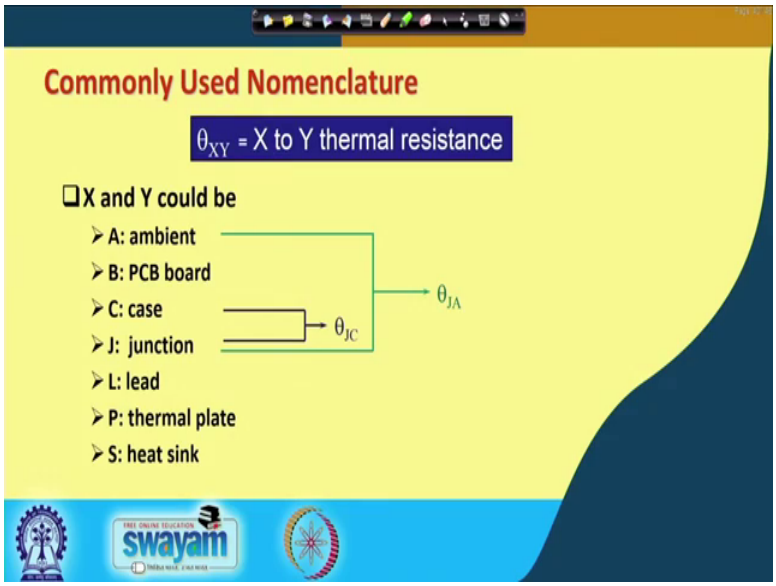

So, this is a commonly used nomenclature. The thermal resistance is typically denoted by the symbol theta ok. The units if you recall is degree C per watt, and theta X Y sub X in this as a subscript X Y means, it is the thermal resistance from point X to point Y ok. And X and Y can assume different values ok. So, X or Y can be the temperature for ambient or the point X and Y can be ambient, it can be board, can be case we are going to look at what case is, junction, lead thermal plate, heat sink, so several of those ok.

So, therefore for example if you are talking about the thermal resistance between the junction, which is a point within the piece of silicon microchip, and that is denoted by J for junction, and A is ambient, then the thermal resistance is going to be theta JA ok. Similarly, if there is a thermal resistance from the junction to what is called the case, and we will look at what cases, then we will call it theta JC that is theta junction to case alright.

So, you know in a few slides, we are going to see examples of these what is and then what is junction, what is board, what is case, what is ambient will become what is sink will become a little more clear alright. So, this is theta, and this is typical nomenclature. So, let us say somebody said what is theta JC, if you are a thermal design and many people will ask for any new package that is designed any package architecture, somebody say (Refer Time: 03:34) what is the theta JC for this package. And you will say oh theta JC, I think that is typically around 1.1 degree C per watt, so oh is it so ok.

What is what is case two ambient, and you would say maybe like 2 degrees C per watt ok, so something like that alright.

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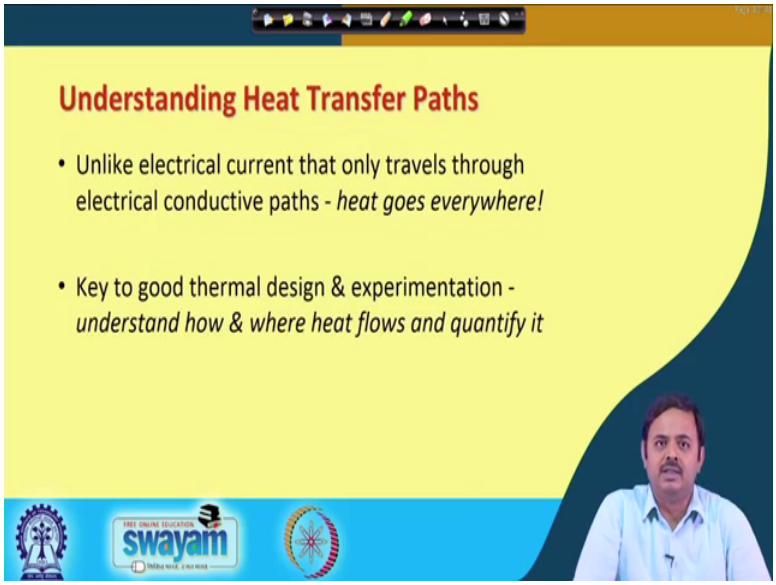

So, now the thing is you know when we talk about thermal resistance, and we are going to use thermal resistance network to solve problems. It is very important to understand where all the heat is going, how many paths does the heat have. So, it is generated at a certain point in this case the microprocessor, from there where does it go.

And let us see you say from there, it finally goes to the amp atmosphere goes to the ambient that is where it is dissipated fine. But, while going there what are the paths it can take, does it have only one path to go or can it have multiple paths ok. For example, in the small problem that we solved in the last lecture, we did we considered only one single heat flow path from the junction to the thermal interface material to the copper plate and then to the ambient ok.

Now, there could have been a parallel path from the junction to the package, to the substrate, to the motherboard, then to the ambient ok. So, these are then two parallel paths. And then there can be multiple ones, we will see some of those. So, what I am trying to say is it is very important to understand the heat transfer paths. What are the different routes, the heat the thermal energy can take while flowing from point A to point B ok.

Now, unlike electrical current that travels only through electric electrical conductive paths, heat goes everywhere ok. Now, probably the electrical engineers is not probably say this is technically not correct, because even if it is an electrical insulator, there will still be some teeny mini movement of electrons and all. But, you know for heat as long as it is there is a medium, there will be heat transfer either by conduction or convection.

And even if there is no medium, there can be heat transfer through radiation ok. So, heat goes everywhere you cannot say, because there is no perfect insulator. You can have a material with very very low thermal conductivity a solid material, but still there will be some amount of heat ok. And then we have to we have to take a judgment as to whether we want to neglect it or we still want to consider it. So, to key to good thermal design and experimentation is to understand how and where heat flows and to quantify it, so which is again trying to identify through all what all paths can the heat flow from its point of generation to the final point of dissipation ok, so that is the case. Then let us move on to the next slide.

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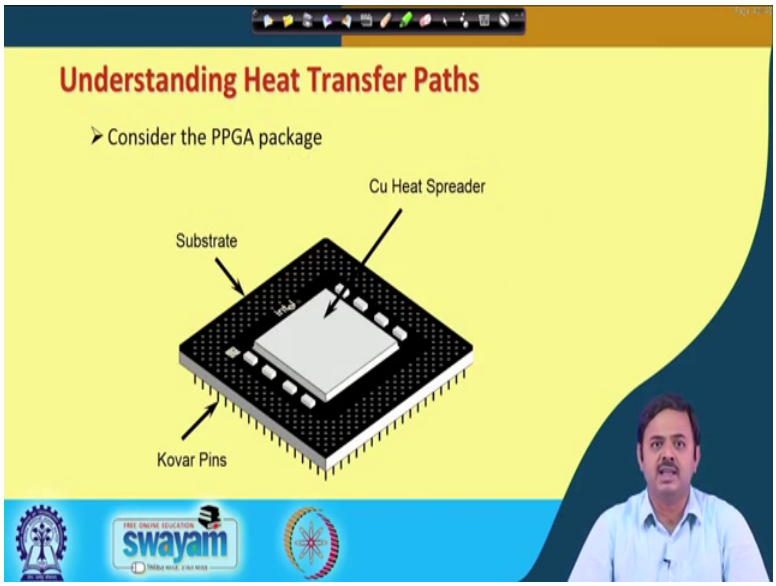

And we will look at one of a simple package, as you can see this is a pin grid array, it is a pin grid array. It is it is a very old Intel package, it is a schematic of that. And what you see is you cannot see the piece of silicon inside, because it is covered with a copper heat spreader, heat spreader is like a plate ok. And we will see a schematic in the cross sectional schematic in the next direction in the next slide ok. So, this is the substrate or

the chip carrier onto which the chip is bonded, typically flip chip bonded, and with a copper spreader on top ok. And then this substrate has pins, so the attachment to the from the substrate to the motherboard is through a pin grid array alright.

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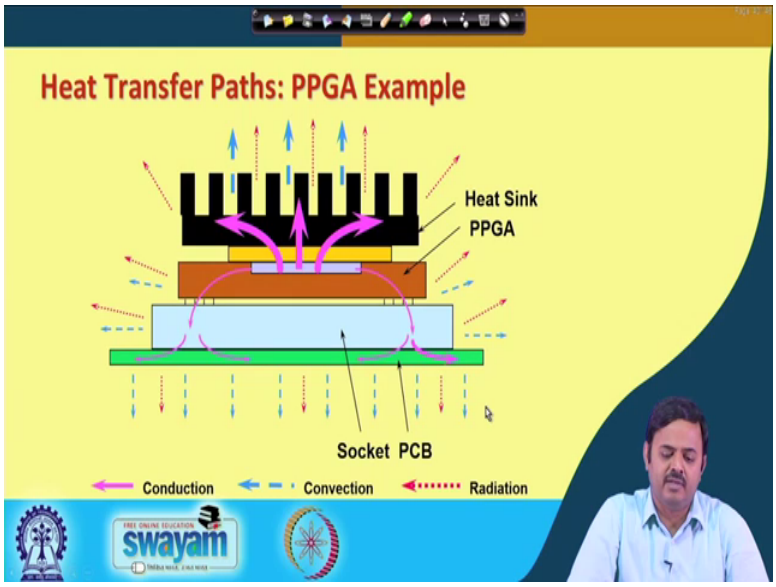

So, if you look at this plastic pin grid array package, what will I have? If I look at the cross section now, what I have is the following. What we saw before was this piece of silicon, which is denoted by gray. And then a piece of copper on the top, and then what has come out as orange is really this substrate ok. Now, between the I mean between the silicon and the substrate, there will be you know the solder balls so on and so forth, which I have not shown ok.

So, this is a piece of silicon resting on a substrate, and then there is a copper plate on top. And the substrate, then with the pins goes to the socket, which is denoted by this light blue, and which in turn is attached to the motherboard denoted by green or the circuit board denoted by green ok. So, socket PCB the pin grid array package, the piece of silicon which is a microchip, and the copper spreader.

And then on top of that typically we place what is called a heat sink, and we are going to see some of these in the probably the next lecture ok. So, heat sink we will see that, but that is at this point just consider it to be a medium, which helps in effective heat dissipation efficient heat dissipation, increases the heat transfer rate alright, so this is how it looks like.

Then what are the different paths in which the heat that is generated in this piece of silicon can flow, and you can see that this is extremely complicated ok. It can flow by conduction from this piece of silicon to the copper, and then to the heat sink, and finally from the heat sink to the ambient ok. So, conduction is denoted by pink. And from heat sink to the to the ambient will be by convection, which is denoted by blue.

But, again remember that radiation also occurs ok, it can be a small component, it can you can neglect it, but radiation if any surface is at a temperature above absolute 0, then it is going to emit radiation ok. And then there will be a net radiation heat transfer from that surface to the ambient ok, so that is what is going that is one path. So, from through conduction from the silicon to the heat spreader, then to the heat sink and then by convection to the ambient what else, it can also take a path in the downward direction.

So, there will be some heat that will flow from the silicon to the substrate. And then through the pins into the socket, and then again from the socket to the motherboard all by conduction, so hence denoted by pink. And then from the motherboard to the ambient by convection and a bit of radiation that is another path.

Then you can also say ok, whatever comes to this from the silicon to the substrate part of it will be conducted, but part of it will also go to the side surfaces, and from where it is going to be lost to the ambient by convection and radiation same for the socket. So, you can see it is a very complicated heat transfer path, many parallel paths in which the heat can flow ok. And we have to quantify each of these, and in order to do that I need to have a means to quantify each the thermal resistance offered by each segment in the heat transfer path ok. So, this is the case here.

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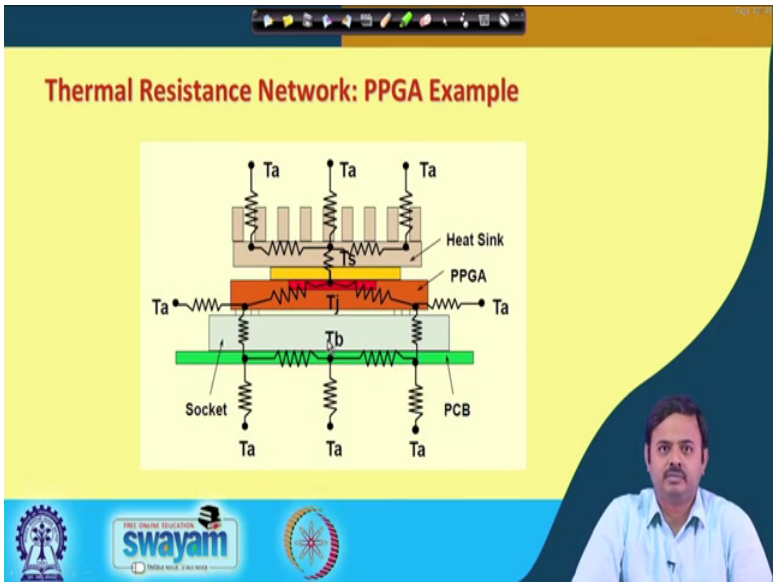

So, if I draw a thermal resistance network, this is how it is going to look like? Extremely complicated as you can see right. So, something that I am not talking about right now, you can see these resistances from this point to this point even the both are in the motherboard ok. There is a resistance from here to here ok, these are something called spreading resistance ok.

Whenever spreading or constriction resistance, whenever heat flows from a smaller area to a larger area apart from just the L over k A, which is the pure conduction resistance 1 D conduction resistance. There is also additional resistance due to spreading ok. We will talk about all these when we solve problems all right. So, this is what it is and so as you can see that if I have to draw a thermal resistance network for a package like this with a heat sink on top as shown here, the thermal resistance network can be very very complicated.

You see lots of resistances some in series, some in parallel, so on and so forth. And you have to come up with an equivalent resistance right using the series and parallel rules, which will help you find the temperatures are some of these intermediate points as well as the total heat flow in each of these directions. It is very common that what is very likely I would say that if you do this whole analysis, you will see that the thermal resistance in this downward direction is very very large compared to the upward direction into the heat sink, and that is the whole idea ok.

So, as a result most of the heat may be more than 90 percent, 90 to 95 percent goes in the top direction as shown in this picture, and a lot less comes down in the bottom. But, that may not be the case, if this heat sink was not there, then we do not know what will be the split, it may be 60, 40 instead of 90, 10.

Again whether this heat transfer from the heat sink to the ambient, whether it is by force convection on conversion will also depend the split, because force conversion the thermal resistance is going to be much lower compared to natural convection ok. So, all these play a lot of importance ok. And therefore, what did we start by saying that it is very important to identify the heat flow paths, and only then can we come up with an accurate thermal resistance network, which is going to help us quantify the heat flow in different directions ok.

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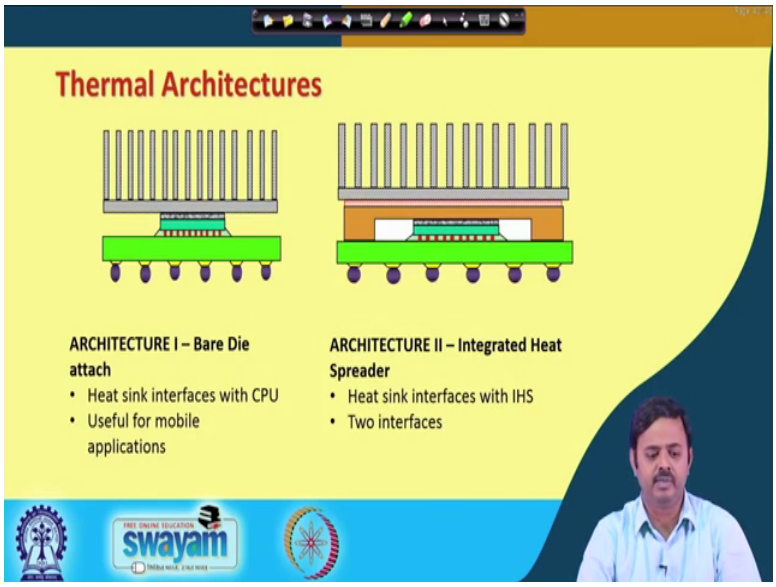

So, now let us look into what is called thermal architecture ok. So, there are two very common thermal architectures for a silicon in the computing world. So, one is called the bare die attached, and one is called the integrated heat spreader ok. So, the first one I am going to talk about is bare die attached. So, here the silicon is this green portion is this one ok, as you can see it is flip chip bonded onto this substrate correct.

So, this red elongated spheres as you can see elongated circles as you can see are the solder balls, it is a cross section. And then what is around the solder ball is that under fill epoxy, if you recall ok. The silicon is bonded onto the substrate flip-chip bonded, and

this is under fill epoxy ok. The substrate in turn will have ball grid array, and it will be attached to the motherboard using this ball grid array ok. So, it is ball grid array from flip-chip bonded with BGA from the silicon to the substrate. And again from the substrate to the motherboard, which is not shown here ok.

Now, what happens is why is it called bare die attached, because the heat sink is directly attached on to the silicon. The heat sink as you can see, which has bass and what these are called fins, we will see this in the next lecture. So, this fin heat sink is directly placed on the silicon. And in this case more correctly on the backside of the silicon, because this is a flip chip bonded ok.

And the issue is that again as we were talking about yesterday, in the last lecture sorry that you know no two surfaces can be perfectly bonded, because these are solid surfaces there is nothing called absolutely flat surface. So, therefore in order to fill in the voids, we need a thermal interface material, and that is what is shown over here ok. So, the heat sink is placed on the piece of silicon with a layer of thermal interface material in between ok.

So, this is useful in mobile applications, mobile as in when I say mobile applications, it is not strictly mobile phones, it also means laptop, computers. And I will say primarily laptop, computers. Actually, this is not absolutely true, we will see that later. In a laptop there is typically not a heat saying that that goes right on the silicon, there is something else called heat pipe, we will talk about that later. But, bare die attach means that there is a heat sink or whatever is a cooling solution directly bonded on to the silicon with of course a layer of thermal interface material in between.

The other one is the integrated heat spreader architecture -2, where what happens is above the silicon you have what is called a heat spreader. It is typically a copper plate or sometimes also you can also call it many people call it the lid l i d lid ok. So, it is in the form of a copper plate, which is bent at the edges in the form of u. And inside this is the piece of silicon. And again between the copper and the silicon, you have a layer of interface material ok. And then the heat sink is placed on this integrated heat spreader ok.

And again we have a second layer of interface material, which is shown by this hashed red lines over here ok. So, what is the difference over here, there is only one layer of interface material, and many a times we call it TIM-1. Over here there are two layers of

interface material, one between the silicon and the heat spreader which is called TIM-1, and then between the heat spreader and the heat sink which is called TIM-2. So, two interfaces, therefore two layers of interface materials ok.

But, I also want to say at this point is again thinking about the industry, and the way it works. So, if have the semiconductor chip manufacturing companies Intel, AMD ok, and then we have these companies who actually sell the final product the final computer, which we call the OEM, and these include Dell, HP, Apple, and so on and so forth ok, Toshiba, Sony, Fujitsu all these companies.

So, what happens is Intel or AMD the microprocessor company, in case of architecture-1 sells this part sells the silicon, sells up to here the silicon bonded onto the substrate. But, in case of architecture-2, it sells the silicon on the substrate and with the heat spreader attached onto it ok. And the remaining thermal solution what kind of heat sink, what kind of thermal interface material, in the second layer etcetera or in this case the first layer that will be determined by the OEM. The Dell's and HP's of the world ok. Intel or AMD can provide a guidance, but final decision as to what goes into the product lies with the computer equipment manufacturers not the microprocessor manufacturer, so that is also important to know apart from architectures, who controls what, and who designs what is something that is that we should know ok.

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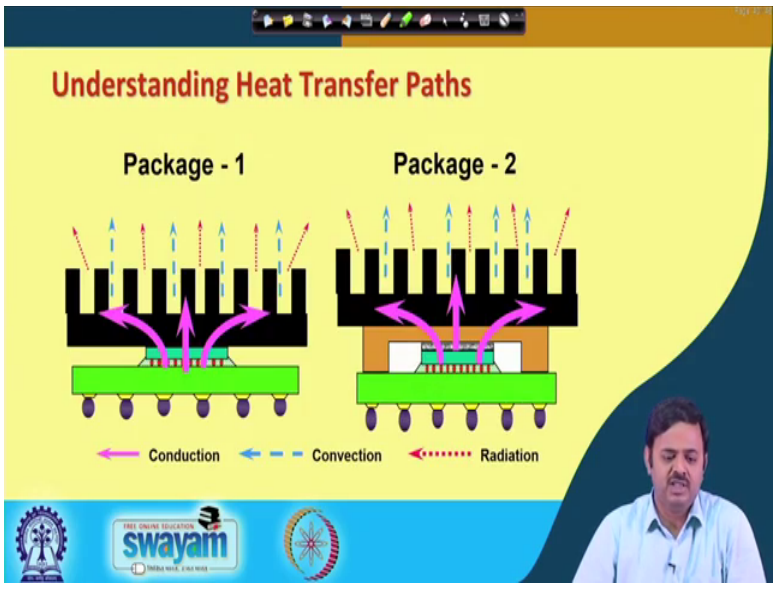

So, now if you look at both of these architectures architecture-1, architecture-2, and at this point what we are saying is we will neglect the heat transfer to the bottom. We will assume that majority of the heat flows in the direction of the heat sink, and what flows in the other direction towards the board, towards the socket, sorry from the substrate to the motherboard is negligible.

If that is the case, then these are the heat flow paths from the silicon it is generated ok. This is where the wall read area that is where it is going to be generated, and then it goes up, and then by convection and radiation from the heat sink to the ambient. Except that in this case in the conduction path, you will have the silicon and TIM-1 over here you will have silicon TIM-1, heat spreader TIM-2, then heat sink yeah.

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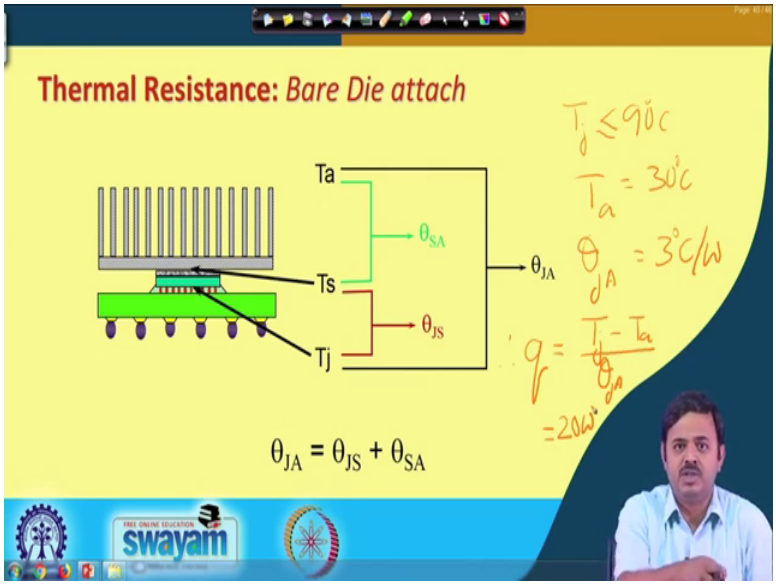

So, if I do the bare die attach, these are the three temperatures that we talked about ok. T j we have already discussed, T junction that is inside this piece of silicon that is the hottest temperature that is because that is where the heat is getting generated so T j. Typically, if somebody is for example Intel or AMD is selling this my trouble, they will say T j cannot exceed 100 degree centigrade or T j cannot exceed 80 degree centigrade. So, these are all specified T j max, that limit is set. And so the thermal solution designer, now has to come up with the thermal solution such that to ensure that the T j does not exceed that maximum allowable limit ok. So, T j very important temperature value.

What next T s what is the temperature at the heat sink base that is T s. And then finally, T a which is T ambient all right. So, assuming these three points that junction, the sink, and the ambient. We can define the resistance from junction to sink, so theta JS, a thermal resistance from sink to ambient, which is theta SA. And since these are all in series, we can say that theta JS plus theta SA is theta JA ok.

So, now therefore think about it if you can quantify theta JA, what is the junction to ambient resistance? Let us say I say it is 3 degree C per watt ok. And then I tell you that you know my ambient condition is 30 degrees. And my theta J sorry my T j cannot exceed 90 degree C T j max is 90 degree C in an ambient of 30. Then what is the maximum T j minus T a I can have that is 60 degrees 90 minus 30.

So, then what is the amount maximum amount of heat that can be dissipated in this path, that is going to be 60 degrees which is T j minus T a divided by theta JA, so 60 degrees divided by 3 degree C per watt so or 20 watts alright. So, what I am trying to say is let us say you are given a problem, and where you are told that T j must be less than equal to 90 degrees C. T ambient is 30 degrees C. And theta JA is 3 degrees C per watt. What is q therefore? q is therefore T j minus T a divided by theta JA, and that comes to 20 watts.

So, therefore the thermal designer is going to put the ball back in the coat of the electrical designer and say, you know what if this is what you are talking about have done these calculations, and if this is the limits, these are the limits that you are going to set that in namely that jump T j cannot exceed 90 degrees in the 30 degree ambient.

Then I am unable to cool with the current solution, the maximum that I am maximum power that I can dissipate. So, maximum cooling that I can provide is 20 watts, is that enough? So, the TDP the thermal design power is 20 watts. So, whatever architecture you do in this piece of silicon make sure that the power dissipation under any workload does not exceed 20 watts. Otherwise, this thermal solution is not going to work or you have to relax this T j limit and make it less 100 degrees, 105 degrees ok.

So, this is how you know the correspondence between the electrical and thermal engineers go clear bare die attach. So, packet with IHS example, similar thing except now here, we have the another additional temperature. We also have what is called the case temperature T c remember I say that I am going to define what c is the case is this is what the case temperature is, it is a temperature on the surface of the heat spreader T c

ok. So, this heat spreader comes with different names integrated heat spreader is the most technically correct name, but people use words like lid, people use words like case alright.

So, and these are not unjustified names, because apart from what is called spreading the heat, and giving it more surface area for dissipation what it does is the heat spreader also protects the silicon inside from external factors right, so that way is also a keys or a lid right ok. So, in this case, what happens? The four temperatures junction, case, sink, and ambient, but they are practical it is very difficult to measure both the case and the sink, because they are very close to each other. And what separates them is a layer of interface material ok.

So, in this case however, if I have to draw the theta resistance, if I to write down the thermal resistances, I would have a theta JC, I will have a theta CS, I will have a theta SA, and the sum total of that them is going to be theta junction to ambient ok. So, again here also if I am able to calculate these resistances, then I can given the temperature constraints. I can define what is going to be the maximum power that can be dissipated, and therefore what is going to be the TDP that this package can is able to withstand alright.

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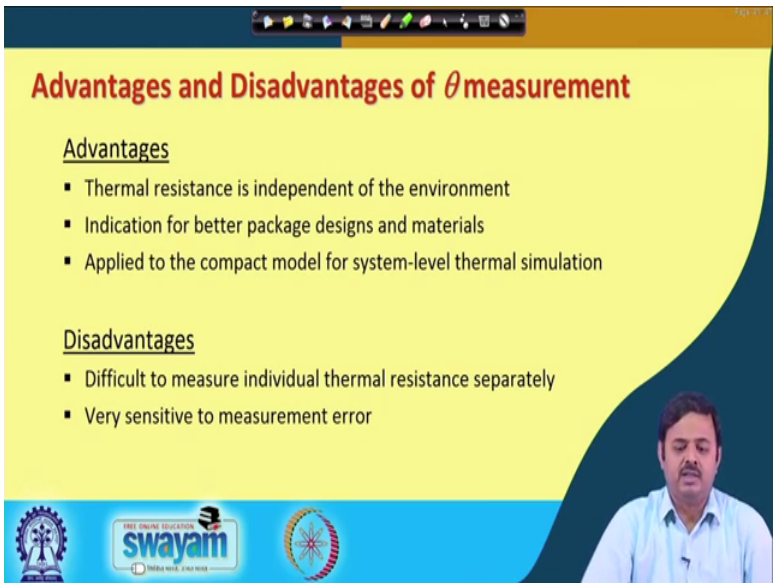

So, sometimes theta can be calculated, sometimes theta is measured ok, you know how much power you are putting in, and then you measure the temperatures and determine

what is theta ok. The advantage is thermal resistance is independent of environment, it does not depend on the temperature not fully correct I would say, but except especially for radiation, and even for natural convection ok. Because thermal resistance especially if it is h, the h for natural convection just depend on the temperature difference between the hot and the surface and the cold ambient alright. But, more or less it is in a in a given range, it is more or less can be assumed to be independent or very weak dependence on the other factors ok.

Indication for better package designs and materials because, if you can measure it, you can say oh this term this theta is very low, which means this is a good thermal the thermal solution is very good ok. And it is very good as we saw that this is a very useful tool to make quick estimations, system level thermal simulations. If you want to go for system level thermal simulation ok, we will see that later. I am doing a modeling of the entire motherboard with all these components, are we going to model each of these every layer of the interface material every heat sink no, we would just put this package at the place, and define a thermal resistance in both directions towards to the ambient, to the board ok.

Now, what are the disadvantages? It is very difficult to measure these thermal resistances separately, because sometimes these temperatures can be so close, also where do you put the thermocouple. So, the measurement is not easy. And it is very sensitive to measurement error.

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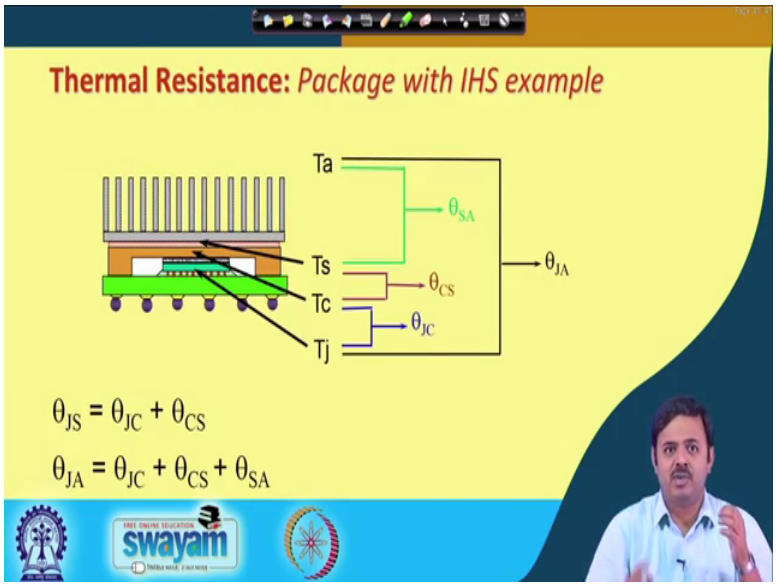

Think about if I want to do measure the temp in the previous slide, if I want to measure the temperature of the sync T s, and T c its impossible ok, where do you put the thermocouples are going to collide with each other ok. So, there are certain disadvantages, but all said and done theta is widely theta JC, theta CA, theta JA, theta JS these are widely used parameters in the electronics packaging industry ok. People use it, engineers practicing engineers use it day-in and day-out.

And when I say practicing engineers, these are not that of course the thermal engineers do come up with these values. So, they think they have to think a lot more, they have to worry about conduction convection radiation how can I do this, how can I increase heat transfer coefficient all that stuff that is their job. But, their final aim is to reduce theta as much as possible.

And then give this value to the non-thermal engineers, who are then going to use this value for their package level model, system level models to determine, what is the maximum power that they can you know put in into this piece of silicon so on and so forth ok. From that point of view, this is very very useful ok.

So, thank you very much that is all I wanted to cover for this lecture just to recap, we covered the concept, in the last class we talked about what is thermal resistance. And we did a small exercise problem. Today, we went deeper into actual package architectures, and looked at what are the different thermal resistances, what is the different heat flow

paths, and what kind how complicated a thermal resistant network can become and so on ok. So, while discussing all these we talked about a cooling solution called a heat sink what is the heat sink, we are going to take it up in the next lecture.

Thank you very much.