Electronic Packaging and Manufacturing
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Lecture – 15
Advanced Packaging

Hello welcome back. So, what we will do today is in the last lecture we had kind of come to a reasonable end on the basics of first level packaging right. So, today what we shall do is, we are going to look at some of these concepts of in what we call advanced packaging which is you know taking the conventional first level packaging and looking at some you know some of the more modern day designs. So, as I said this is a very vast and very fast evolving field where people are continuously innovating to come for coming out with newer and newer designs newer and newer configurations, trying to fit in more number of components and devices within a certain space constraint.

So, all these actually form the motivation for these advanced packaging concepts that we are going to talk about today. We are only going to talk about some of them which have become more popular and just trying to say that what we will see is just tip of the iceberg maybe because as I have repeatedly said there are 100s of engine hundred I will say thousands of engineers who are working around the clock on this field of electronic packaging and just on this first and second level packaging, all right.

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So, advanced packaging that is the concepts that we are going to cover today. And under that we will talk about some new designs and especially some of the very popular terms that are used today.

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So, to start with why is advanced packaging required today, all right. So, this is for there is an incessant continuous need for faster, lighter, cheaper and better electronics ok. And primarily many of the advanced packaging that we are going to see today is due to be due to the second reason which is which is shrinkage in footprint and form factor. So, the amount we are always looking for sleeker, thinner, lighter, smaller device smaller gadgets whether we are talking about Smartphone's, we are talking about laptops, tablets or even otherwise even TV's where probably the screen size goes up, but you need the third dimension which is the thickness it does go down ok.

So, this calls for the need for advanced designs and methods now the picture that I am showing over here is something called a 3D stacking of dies and as you can see we had talked about wire bonding as part of our discussions and what we see here are actually three such pieces of silicon. So, three such components with their own circuitry inside stacked on each other right and we see this periphery from the periphery these wire bonds coming out ok.

So, you see this, this is this particular example or picture that we see is where there is a logic die and two types of memory dies and these are kind of 3D stacked or put above

one above the other to in a high performance product alright. So, we will talk about this in more details when we come to stacking of dies ok.

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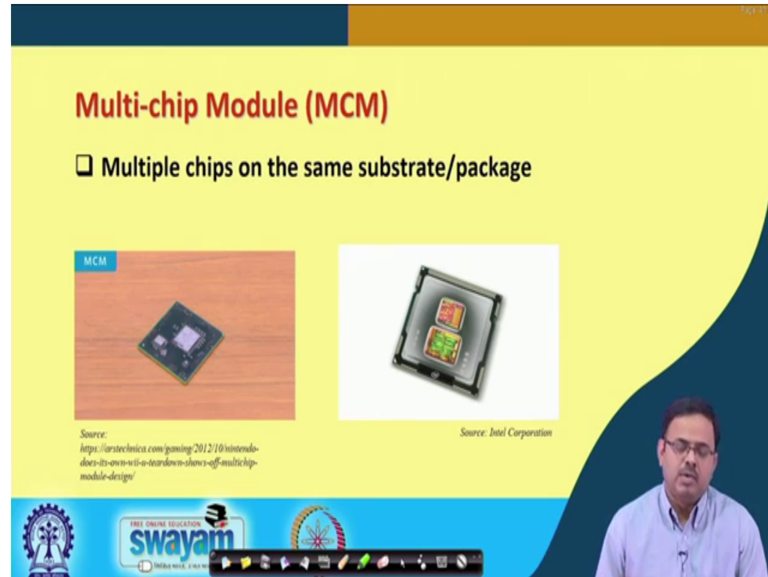

So, the first concept that we are going to talk about is something called multi chip modules ok. So, what is multi chip module? As the name suggests itself these are multiple chips on a single substrate, see all this file even the small props that I have brought in these lectures on the pictures that we have seen it is always one package and one major component on that.

And typically we have seen CPUs ok, now look at the picture on the left and also kind of an artist's impression on the right hand side. What we see are multiple dies or multiple pieces of silicon on the same package alright. The first one is the v which is a gaming device from the nintendo and you see that there are two pieces of silicon the ones that are particularly what you see in the color gray that is a real picture, that is a real package with two important components on the same package. And the connections, interconnections between these two components are through the you know wiring layers in this substrate which is an organic substrate fr 4 and that is what we see over there alright.

On the right hand side is an Intel MCM. So, what you see over here this is not a picture this is kind of a rendition, but this is actually how it looks like of course, if you if you look from the top what you see here this is a substrate with an integrated heat spreader on

top, we are going to talk about heat spreaders when we come to thermal management discussions. But inside the heat spreader or IHS as we call it what we see are two silicon architectures or two two silicon components and this one is the CPU the processor and graphics. So, CPU plus GPU may be right. And that this is a little bit of an artist's impression because it is trying to show the circuitry inside ok. So, that is why this you see these circuits inside the architecture, but this is an actual product ok. So, these multi chip modules are there in real products today ok.

So, instead of having two separate packages one for the CPU one for the graphics you have it integrated right on the same substrate. What is the advantage? Of course, it is you can accommodate more number of important components in a smaller footprint or area. Secondly, the communication the interconnection between these two important chips happen over a shorter electrical length, I mean think about it if this was on the right hands on the left hand side or on the right hand side even.

If both these components had their own individual packages then what would have been the path for communication between the two, if the CPU has to talk to graphics. The signals have to pass from the CPU and the silicon bumps in the BGA onto the substrate wiring traces on the substrate and then through the socket whether it is a pin grid array or if it is a ball grid array direct attached on the motherboard whatever it is through another layer of interconnections into the motherboard.

Then through the motherboard and then another layer of interactions to the substrate of the second die and then inside the substrate through another layer of interconnect to the chip the second chip right. But now what we are doing is instead of having you know chip 1 to the substrate 1 to the motherboard, then substrate 2 to chip. And at each level or interface you have one layer of interconnect, you just have connection between these two's through the wiring traces inside this piece of silicon.

And of course, there are two levels of interconnects, but I have definitely gotten rid of number 1: two additional levels of interconnections which is between the motherboard and the substrate that is one. And number 2, the electrical paths have become significantly shorter because they are on the same substrate ok. So, that is MCM and various configurations of MCM across a various range of products are available commercially available in the products today.

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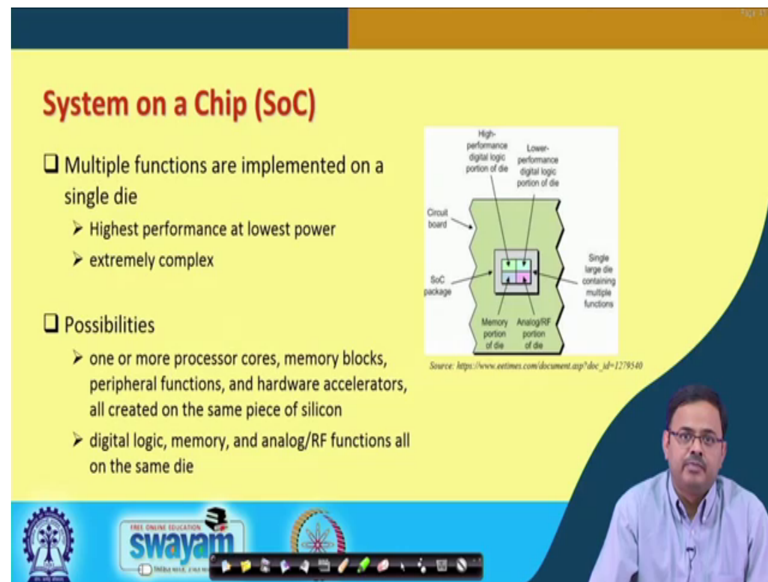

The next one is called System on a Chip SoC and ok, I am going to talk about several MCM we started with the MCM we are now talking about a SoC now. It s not like they have kind of I mean all these have evolved parallel it is not like it was first MCM, then SoC then SiP which I am going to talk about today then poor package on package. So, nothing like that, I mean these advances have been happening almost simultaneously at various configurations.

So, system on a chip as a name suggests it is you know you have a single piece of silicon and you have multiple functionalities inside ok. So therefore, what happens of course, the circuitry becomes very very complex, costly intricate designs all that stuff definitely. But what is happening is if you succeed in doing this then you have the highest performance at the lowest power.

Now, what is system on a chip and what is multiple functions implemented on a single die? Now, that can vary depending on who you talk to especially in the electrical domain ok. So, if you depending on who you talk to people will say various possibilities. So, one or more processor cores, memory blocks, other functions hardware accelerators all created on the single piece of silicon. So, some people will say this is system on a chip you have processor you have memory storage you have some other functions maybe say little bit of graphics and a and a variety of stuff ok.

Now, somebody may say that oh digital logic memory and analog functions all on the same piece of silicon, that is another way very varied functions multiple functions on the same piece of silicon ok. So, where are its possibilities, but the overall SoC what it means is having multiple functionalities and many a times diverse functionalities on the same piece of silicon.

See today we talk about multi core architecture in CPU, you have dual started with dual core, quad core, octa core, but primarily what each of these cores and the functionalities are not very different right. But on the other hand if you have let us say on die memory, on chip memory then that is very different than you know processing. Now that being said; however, there is static ram actually on the CPU when we talk about core and cache; cache is actually static RAM used for storage of you means yet storage of data if you think of data storage actually the first level is your cache, the next level is your Dynamic RAM DDR and now of course, you also have you know flash memory and then finally is your hard disk right.

So, that is why when you sorry I am probably (Refer Time: 11:07) a little bit talking a bit about architecture in very Layman and Novice term, but many a times you will see that for if you while doing your computations, if you are referring to some file which we have not used for a long time then what happens is the processor has to go back to the hard disk to retrieve that data. And that takes a lot of time and then if there is some data that is stored right away in the cache or even in the memory the response is much faster. So, there is something called latency ok, but forget that, but what I am trying to say and now what data gets stored where that is where the architecture comes in. That is where these thousands of smart, extremely smart and sharp people doing VLSI design and architecture so it is not easy all right.

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System in Package (SiP)

- Chip-scale package (CSP) devices mounted on a common substrate used to connect them all together.
- Substrate and its components then placed in a single package
- Possibilities
  - can include analog, digital, and radio frequency (RF) dice in the same package, where each die is implemented using that domain's most appropriate technology process

Next one is system in package alright. So, system in package are typically chip scale packages or devices mounted on a common substrate and the substrate kind of connection. So, in many a way it is like a multi chip module and the substrate and its components are placed in a single package ok. So, you see these pictures over here and the schematic from that so this is actually I have referred to this article, it actually shows you quite a bit. But as you can see there is a memory die there is a radio frequency analog die there are smaller dies, but they are all on a substrate that finally goes on the motherboard and you see two of those who were on in the second picture. And third picture also you see memory processor and various other various other you know various other components on the same substrate right.

So, in a way SiP and multi chip module are not very different except that in sip all these the individual packages also as you can see over here this is a package, this can have a silicon inside this is also a package with a silicon inside ok. So, there is a there can be substrates on the substrate and then into the motherboard that is also possible. The other thing is these are all chip scale packages, instead of just silicon which is what we saw in multi chip module; these are actually chip scale package devices; chip scale packages ok. So, that is the difference between MCM and SiP. In many ways they are similar, but MCM is multi chip it is just piece of silicon on the same substrate here these are chip scale packages on the same substrate and the package itself has its own substrate ok. So, that is the difference alright.

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So, next what we will go forward is what is called the multi dimensional integration. See, so far whatever we were talking about whether its chip scale, whether its system in package these were all in the same plane and there will be a little height difference. For example, if you talk about the multi chip module the two pieces of silicon can have a difference in height, but nothing more than that, the connections are still on the same plane on the substrate, but when you come to integration this is what is called 2.5D integration. So, what happens is first of all you know a system in package substrate.

And then you want to put further dies on them and the problem is the fact that these wiring traces these tracks or wiring tracks as we call are very different. So, therefore, if you just put one on the top of other then it will be there will be a lot of mismatch. So, therefore, what happens is in 2.5D integration there is something called an interposer made of silicon which is placed between the substrate and the die. And this silicon interposer which is the intermediate link what it has is, what is called a through silicon via TSV ok. So, through silicon via's help in number 1, for you know for transmission of signals that is 1 bu, also for conduction of heat ok.

So, that is kind of 2.5 to integration. So, it helps in increase in capacity and performance, but more importantly it overcomes a problem of mismatch in the wiring tracks, if you suddenly have a very thin wire and then I certainly think wire then it becomes difficult I mean this right it is like you know if you in your plumbing system you have very thin

pipe and then a very thick pipe then there is a mismatch especially at the junctions there will be a lot of these in fluid mechanics terms there will be a lot of you know sudden expansion and therefore, pressure losses or even sudden contractions right. It's a, like for example, you are driving a car on a wide road and suddenly you have to enter a narrow lane. So, of course, there will be a kind of bottleneck and traffic jam over there. So, smooth flow of traffic will be hampered. So, same case here, if your wiring traces where they connect have a lot of mismatch in terms of the wiring of the tracks and its dimensions.

Then it will impact the flow of signal and signal integrity. So, in order to overcome that what we have is this interposer layer way through silicon vias that kind of kind of you know helps us neutralize or overcome this mismatch and kind of reduces the signal integrity issues to as to a large extent ok. So, what you see on the right hand side is Xilinx Virtex 7. So, you can look up this so this is actually a 2.5D device. You see this you have a silicon interposer and then silicon interposer in turn has this C 4 bumps and then it goes to the package substrate and the package has this larger bumps which goes into the motherboard. So, you see here you have four of these FPGA flip chip PGA pin (Refer Time: 17:59) dies ok.

Flip the pin grids are at the top and then you have a silicon interposer and then you have this C 4 bumps which we saw in ball grid array in flip chip controlled collapse chip connect if you recall C 4 and then you have the package substrate and then the BGA balls. It can be PGA also, it does not this last level of interconnect can be ball grid array can be land grid array can be pin grid array, but you see this and if you do take a zoom view what you see is you have this micro bumps at the first level and then you have the through silicon via's and then you have the larger bumps over here; so this interposer kind of helps in overcoming the mismatch between the smaller bumps and the larger bumps.

So, what it is essentially doing is let us say these two dies that we see here this one and this one they need to talk to each other. In the earlier case what would have happened smaller ball to the larger ball to the substrate through these traces and again to the next one, but now through this interposer they can talk to each other ok. So, that is 2.5D integration alright. Then we come to 3D integration so that is you know; obviously, the next step what is 3 dimensional integration, alright.

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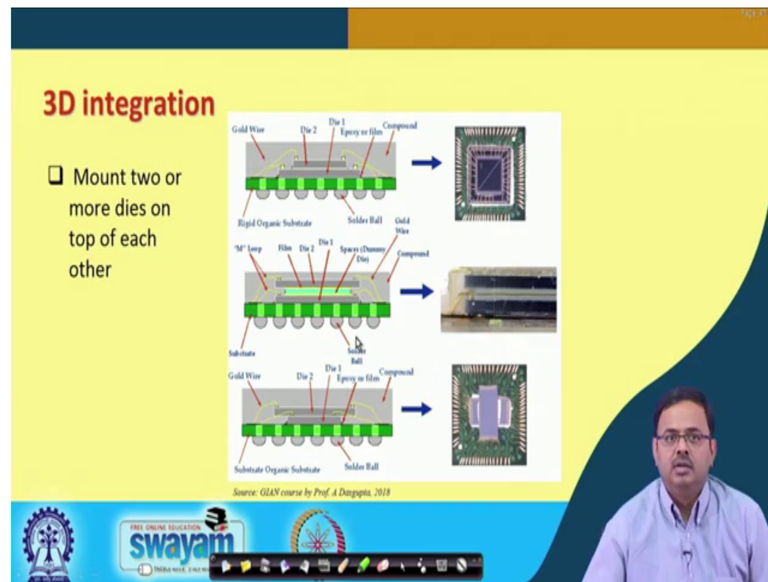

So, here two or more dies are mounted on top of each other. So, here again this has kind of evolved. The first one you see there are two dies one on top of each other and both are kind of peripheral dies peripheral connections and wire bonded, see that. So, die 1 is the larger one, die 2 is the smaller one and the two are kind of connected with each other there is a kind of an interface compound that connects die 1 and die 2.

And then the die 1 is connected to the package substrate it can and the substrate in turn has the solder bumps or solid balls or solder bumps on the underside which will be bonded on the motherboard onto the motherboard. And if you look at the top view you see these are two separate dies and two levels of wire bonding; one for the lower one one for the higher one ok. The next one that you see is again two dies, but here die 1 and die 2 are more or less of the same dimensions and between the two there is a dummy die or a spacer die ok. That is required so that you can route this wiring traces on the two sides alright.

And the third one is where it is like an inverted freedom it is a smaller die at the bottom and the larger die at the top and they are all in a molded compound as I shown and you see some pictures also. The other thing is on the lower one it can also be two different aspect ratios as you can see on the picture on the right hand side. So, the dies are of similar dimensions, but they are orthogonal to each other the first one is like this but the

second one is like this instead of right on top of each other like this these are orthogonal ok. So, that is 3D integration as you can see here alright.

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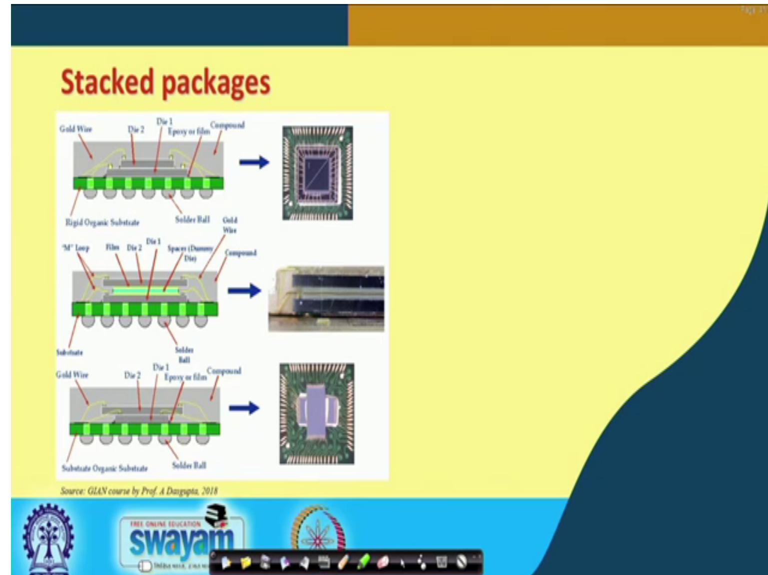

So, now let me mention something over here, when you come to 3D stacking it is also possible that the first layer of for the die 1 in this case that can be, that does not necessarily have to be a wire bonded wire bonded silicon, it can be a flip chip bonded as well. So, the first one can be a ball read flip chip ball grid array on the flip chip bonded device on the substrate and then what comes on top can be wire bonded ok. These days people are also talking about two levels or two layers of already you know solder bondings alright. So, that is possible. Now, I want to give you a real example from my own experience, this was not I was not directly involved one of my colleagues where it was involved; its my very good friend doctor Anand Deshpande.

So, when we were working together at Intel Anand was in a different group and they used to look at this 3D package the design etcetera and he did a very nice optimization problem. So, let us say you have take a very simple case, you have identical dies like this same architecture and you want to stack them on top of each other. How will you do it? Alright now, every silly piece of silicon that has its own architecture inside there will be areas of high concentration there will be the course there will be this areas of activity if I may call it so.

Now, but these are also areas where there is maximum heat generation and this gives rise to localized hot spots. Now, let us say you have an n layered stacking of such dies one on top of the one on top of each other. So, an electrical engineer would say that you know you just stack them identically on top of each other.

Because then if you look at two cores; for example, there will be have the lowest electrical distance in between them they will just align one on top of each other, electrical performance would be wonderful. The thermal engineer will say that is the worst design you are lining up the hotspots, I will just have a single area along the 3D stacking where the entire heat will be generated, it will be a nightmare for me to dissipate the heat and in no time will your temperatures just shoot up.

If you want a good thermal design place and you have two dies place these hot spots I mean farthest away from each other ok. Now, that would be a very good thermal design, but not the best electrical design rather probably among the worst electrical designs. So, how do you come to a compromise? So, this is where he did this multidisciplinary optimization problem he solved this coming up with this algorithm first of all defining these objective functions and then doing this MDO or Multidisciplinary Optimization.

And this work actually he went and presented in an I EEE conference, I think there is many years back I think 2009 or 10 probably and they won the best paper award alright. So, I am just telling you some of these research challenges that come because of these stacked packages. So, thermal design of stack dies is also a very very important parameter of course, coming up with the packaging technologies how to do it its a very very challenging. But thereafter it is not just electrical connections, but even the other consequences that one must remember and later on we are also going to talk about soldered ball solder joint reliability the mechanical stresses etcetera. So, all these have to be considered very very carefully alright.

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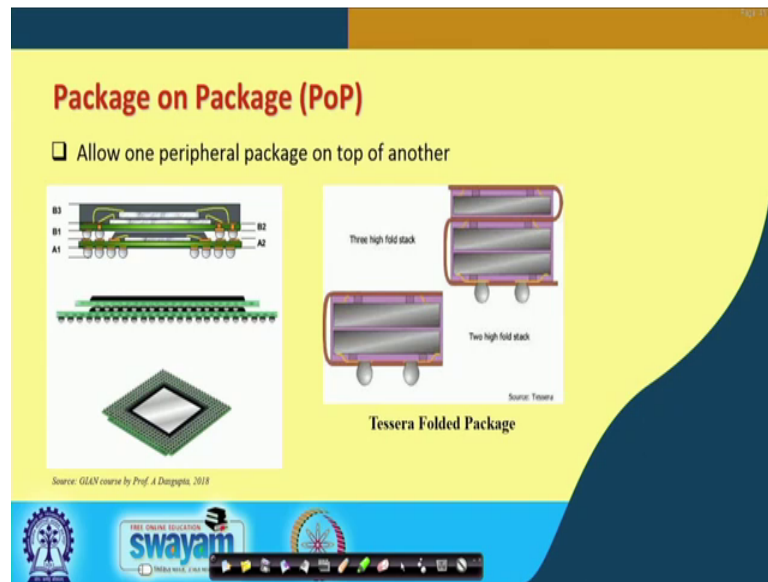

Next we are going to talk about package on package. So, these are actually see if we were these days tack stacking die on top of each other. Now can you stack packages on top of each other, how will you do that? So, in that case for example, look at this picture on the left hand side, the lower one is the package this is a substrate the A 2 with a silicon inside plastic molding all that and that substrate has its own soldered balls or solder bumps at the bottom which is going to get connected on the motherboard. The one at the top you can see that package and substrate also has its solder balls, but those are actually connected on soldered bumps on the periphery of the first package all right.

So, therefore, outside the footprint of the silicon and the chip carrier, and the molded plastic as shown in this picture you have these solder pads on the top side of the substrate. And these solder pads are for the solder bumps for the package that come on top for the substrate of the upper package and this is a complex configuration where the top package actually has standardized, two stacking right two chip stacking. So, this is both 3D stacking of dies in the top package and then package on package configuration it is called pop loosely. So, what are the things that we talked about? We talked about MCM we talked about SoC system on a chip we talked about sip system in package we are talking about pop which is package on package and in the middle we also talked about 2.5D and 3D stacking alright. So, look at this configuration very nice as you can see over here and then sometimes you know these substrates can be flexible.

So, that you can have these folded packages I am showing this Tessera folded package and you see the substrate actually, it was a common substrate which is folded through two right angled bends. And this is how the two packages are now stacked on top of each other its package on package, but on actually on a common substrate which have been kind of given this u shaped turned or bends right and then this is three high these are three packages because it is on a common flexible bendable substrate which can be folded ok. So, you see the there is so many possibilities and there are many new designs that are coming up alright. If time permits towards the end of this course we will talk about some of these advanced topics, and maybe if I get time I will talk about some of the newer advances that are happening today.

But that being said I mean these are all what I am talking about they are all conceived and matured within the last 10 years or so. Maybe, 15 years some of these multi chip model may be a little old, but that also when it came to actual production, they are not very old alright.

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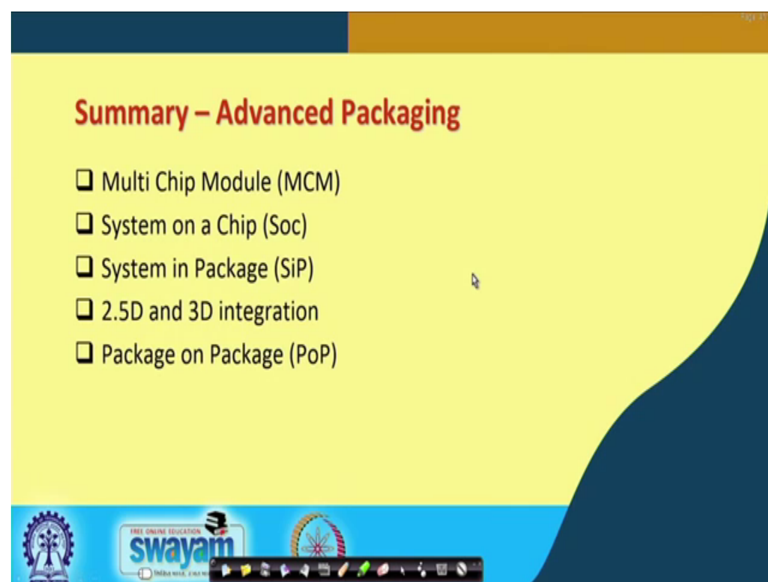

So, that kind of summarizes brings us to the end of this lecture. And to summarize we talked about advanced packaging, multi chip module system on a chip system in package multi dimensional integration. And finally, package on package ok.

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So, these are some references as you can see you will get them packaged in the book of Dally and Tummala we have talked about before. Essentials of Electronic Packaging, the book by Vishwanda vishwanadham that came out in 2011 it is a very nice one again single author one has nice continuity. And you also see these integration technologies especially from Rajan Chanchani. There is a nice its a book chapter, but gives you a very nice configuration it is a book called materials for advanced packaging and especially for stacking and all this is a very good read alright.

So, thank you very much that kind of now actually brings us to the end of first level packaging, and good that we also got some time to discuss about some advanced concepts. So, this kind of wraps up our discussion on first level packaging and we will go over to second level packaging which is going to talk about motherboards circuit cards and so on and so forth from the next lecture onwards. Have a nice day.