Electronic Packaging and Manufacturing
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Lecture – 10
Area array packages - III

Welcome back to the course on Electronic Packaging and Manufacturing. And we will take off from where we left last time. We had talked about in the last lecture; we have talked about ball grid array packages. So, today what we will do is we will look into the next kind type of package or kind of package any array packages again it is called the LGA or the land grid array ok.

So, the concepts that will cover today, we will start with land grid array and then we are going to talk about some other package configurations, and finally go to something called chip scale package or and define what is called a package efficiency or packaging efficiency ok.

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So, these are the concepts that we are going to cover today starting with LGA or land grid array ok.

So, what is LGA? So, what we will do is first we will look at the definition and see what we are talking about.

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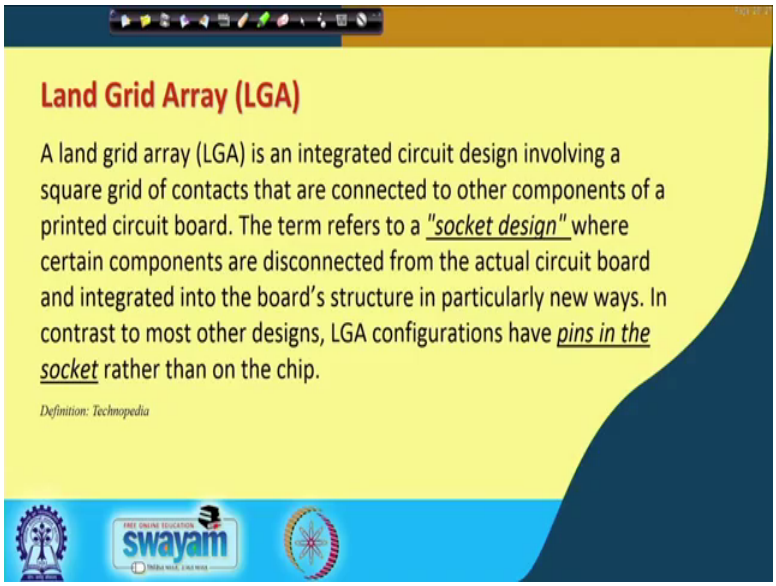

So, a land grid array this is a definition from something called technopedia let me first read this. A land grid array or LGA is an integrated circuit design involving a square grid of contacts ok. Its typically it is square it is not necessary that it has to be a square ok. These contacts that are connected to the other components of the printed circuit board; so if you look at just this first sentence, this is applicable to pin grid array this is applicable to ball grid array.

Now, this is where the differentiate differentiating feature of LGA comes in he term which means LGA refers to a socket design where the certain components are disconnected from the actual circuit board and integrated into the board structure in particularly new ways. So, typically what we have seen some features or components, what we have seen in a package is removed from there and put in the socket ok.

The sentence is still not very clear except that we understand in English what it means. Third one in contrast to most other designs LGA configurations have pins in the socket rather than on the chip now this makes it clear. The pins or the interconnections are in the socket instead of on the package or the chip carriers ok. So, far what did we see? When we looked at a PGA right the pins were connected to the package on the underside like this.

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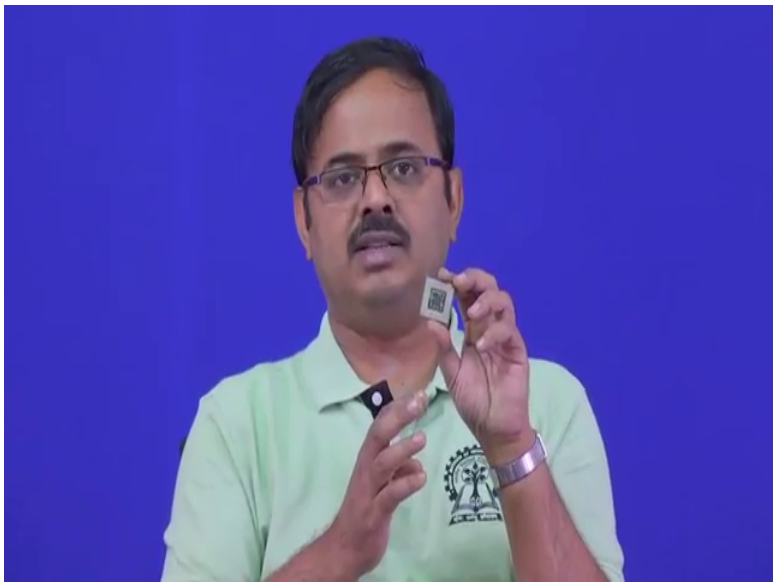

When we look at a BGA it was the same, it instead of pins it was soldered ball which was in turn connected to the solder pads on the motherboard.

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But when we talk of LGA these connections in this case pins again are also called lands are attached not on the package side, but on the motherboard side. So, that is the major difference.

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If you look at this picture it probably is a little more clear. The package side which is shown on the left what do we see? What we see there are pads on the package side these are not pins like a PGA, these are not soldered balls like a BGA. But these are just plated pads correct. And on the right hand side what you see is the socket and the socket has these pins I do not know how clear it is from this picture, but its a socket that has the pins coming out from it ok.

In a plane normal to the motherboard and those pins are going to make a contact with the corresponding pads on the package side. On this package side a pin over here is going to make a connection with a pad on this package side. The picture that you see on the right is a is a I was known as the Intel 771 socket, it was a land grid array socket and it was used in some of Intel's Pentium microprocessors LGA land grid array.

Now, how does this connection happen? I will otherwise the next picture I am going to show you is this where what you see is this is a one connector coming out of the socket this is an FEA finite element analysis. What you see coming out of here is one of the lands and this is one configuration this is it is not like it has to be like this, but this is how it is, and probably this plot I may be a little off. But probably this shows the stress there is a plot of the stress that is inside this at different points in this land ok.

Now, what we will do is we will try to go to the whiteboard and I will try to draw how a land grid array looks like.

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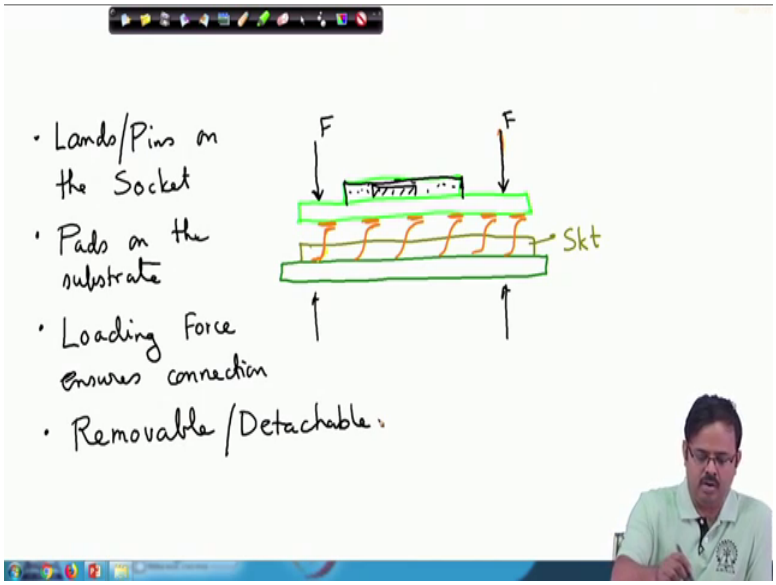

So, let us say this is my motherboard again I am drawing a connection here, and then I will use a different green to denote the packet side ok. And then this has your whatever the silicon sitting inside and then maybe this is the plastic package whatever. Now what do we do with the connections? The package side is going to have these pads; in pin grid array we saw of pins coming out of the package, in ball grid array we had solid balls coming out of the package, but in land grid array we just have what you call these pads.

Now, this is my socket, from the sockets what I will have sorry I will choose a different colour. From the socket side we have this connector pins or lands coming out. So, now, what happens is, in a land grid array sorry let me in a land grid array you put some force and as a result what happens is, these lands press against these pads and the connection is made. And once you remove this loading force then of course, the connection becomes loose and this package can be removed ok.

So, what did we see? So, lands or pins on the socket and pads on the substrate. Second is loading force ensures connection and this arrangement like pin grid array is removable or detachable alright. So, let us go back and again take a look at these two pictures and see what we just talked about. And here now you see this lever there is a kind of a cover at the top. So, this lever leads to the loading force as you pull it down the package is pressed against the socket and the connections are made alright.

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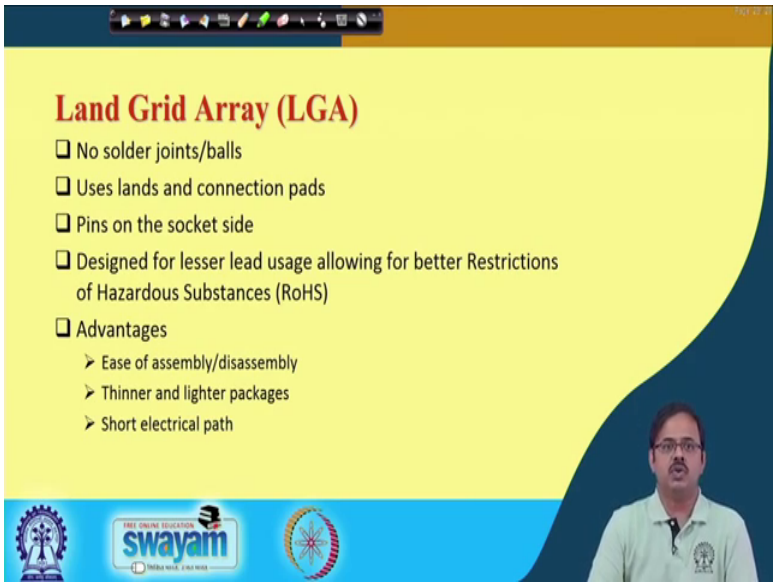

So, what you see is those are the joints or balls uses lands and connection pads. The pins or the lands are on the socket side. And the other thing that I want to tell you is a land grid array compared to a solder or a PGA these land pins are very thin very much more delicate compared to the pins of a pin of a PGA ok. But this leads to lower use of led if you think about solder and all this looks leads to lower use of lead, and so it can be designed for something called wrest better RoHS. RoHS stands for restrictions of hazardous substances ok.

We are going to discuss this later, but now also maybe I can make a mention over here. That this solder typically consisted of led and now what happens is over the last decade there has been a push even more than a decade I would say, there has been a push to go towards led free solder ok.

Therefore, new solder compounds new materials are being synthesized, material scientists have been thinking about various formulations of coming up with lead free solder. You can you can imagine the impact of this you know there is I mean the amount of electronic products substances. And therefore, connections is enormous across the world, now we have to change everything its a humongous task.

So, but the industry is gearing up to that and I think right now we are almost they are all most almost all new products today are made of led free solders ok. So, restrictions of hazardous substances that becomes important from environmental point of view, and to

this end LGA when it first came up this was a major advantage that is you know even if you have to let use leads lead solder, the amount of lead that we are using is smaller.

The advantages; these are thinner compared to PGS. So, therefore, against shorter electrical paths, Its thinner and lighter packages LGA is allow for that and ease of assembly disassembly which we talked about. That is an advantage of any of these pin type of interconnections whether it is LGA or PGA and a disadvantage for a connection like BGA or ball grid array.

So, that is LGA.

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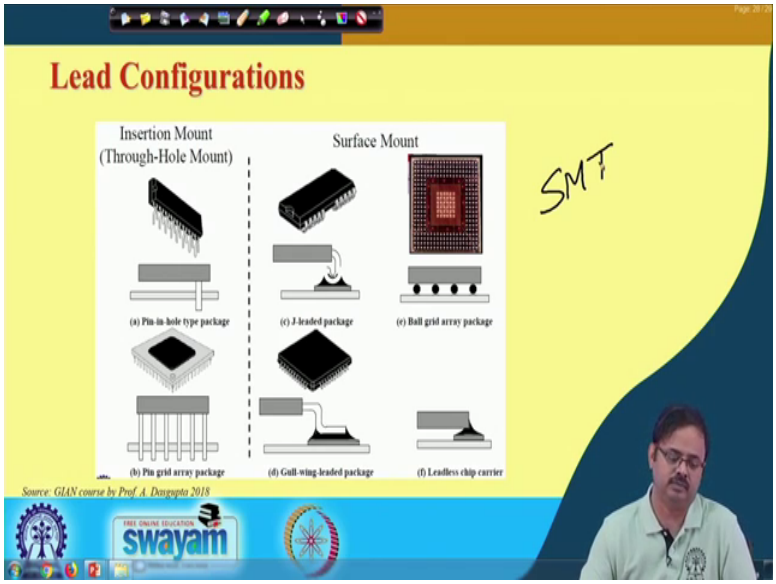

Next we are going to talk about some other lead configurations ok. That was lead pb the element. Here lead is lead as an interconnect we have to keep all these in mind. Lead free solder this is lead configurations and then you also have the lid which is a cover ok. So, whenever I use this word just be careful because they are all similar sounding and every time I may not be spelling it out, but just keep in mind be conscious and try to make out in what context I am using it ok. So, this is lead configurations in terms of interconnection connections.

Insertion mount. So, through hole mount we have seen this before, you see this kind of package over here the connectors come out only from one side of the package ok. Now it could have been a serial 111111, but to give it better mechanical rigidity and stability you

see that this connection takes a bend towards the left towards the right sorry the next one takes a bend towards the left and so, you have this criss cross 1 like this, 2 like this, then 3 like this, 4 like this ok.

So, 1 like this, 2 like this and then these pins go to corresponding holes on the motherboard. So, pin in hole type package we have seen this before and PGA which is pin grid array package ok. So, again this is configuration in terms of we have discussed this before, in terms of the interconnection method this is pin in hole the others are surface mount. So, we had discussed this before now again.

Now, we know; what is a ball grid array that is the surface mount technology ok. Pin grid array also when used with a socket like this its a surface mount technology because you of course, it goes through instead of holes on the motherboard it who goes into the holes on the socket and now the rest of the motherboard is available to put more components and the backside can also be used is typically not used, because this is a very high density package typically it is not used, but can be used it is available alright. J lead package, gull wing leaded package, leadless chip carrier we have discussed all this before and now we have added on surface mount what is known as the ball grid array.

So, as you see the BGA is connected on the on this side of the motherboard. So, it is mounted on the surface and each of these as said before also presents the reverse side of the surface for placement of other components. So, that is the advantage of surface mount technology. Surface mount technology is also often called SMT surface mount technology very commonly used term.

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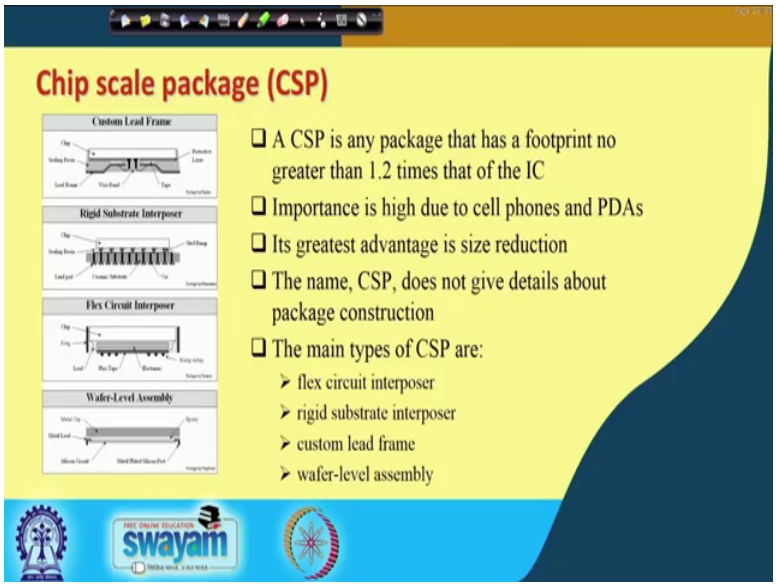

Let us move on to the next slide, this one is known as the chip scale package what is the chip scale package or CSP? We will just briefly discuss each of these a little bit. The CSP stands for a Chip Scale Package means that the size of the chip is comparable to the size of the package. The package is less than 1.2times the size of the IC.

Let me take this example again, this damaged package that I showed before while exhibiting ball grid array. Here what you see this shining part in the centre that is a silicon chip this is a silicon and then this green square that is the package. So, you see that the package is significantly larger than the piece of silicon correct. So, if you want large number of interconnects, then you need a larger package you need more number of solder balls or pins or lands ok. Chip scale package on the other hand the package is less than or equal to 1.2 times the size of the integrated circuit which is the piece of silicon with all the circuits inside ok.

So; obviously, it cannot be used in high end servers where or even high end desktops or even any of the computers like laptops. But however, if you think of the personal digital assistants the cell phones the tablets. So, here these see chip scale packages are important why? Because of two reasons; one is first of all chip scale package is possible because these are nearly not those high density packages, these and these do not have as many features or as much of computing horsepower. So, that part is good it allows for that it does not require that amount and why we put it is? Because these are products where

there is severe space crunch ok. There is not enough space to accommodate a large number of components. So, here if we can come up with chip scale packages it helps ok.

So, the greatest advantage is size reduction no questions about that. However, CSP just the terms CSP chip scale package does not give you apart from this does not give you much idea about what is the construction. So, there are several types of CSPs as we see here, I am not going to talk in details about each of these ok. Maybe if time permits we can come back, but CSP these are different kinds of you know advanced packaging techniques, the course this course is very fundamental. So, we will not go to the advanced packaging technologies, but these are some of the examples where chip scale packages are possible.

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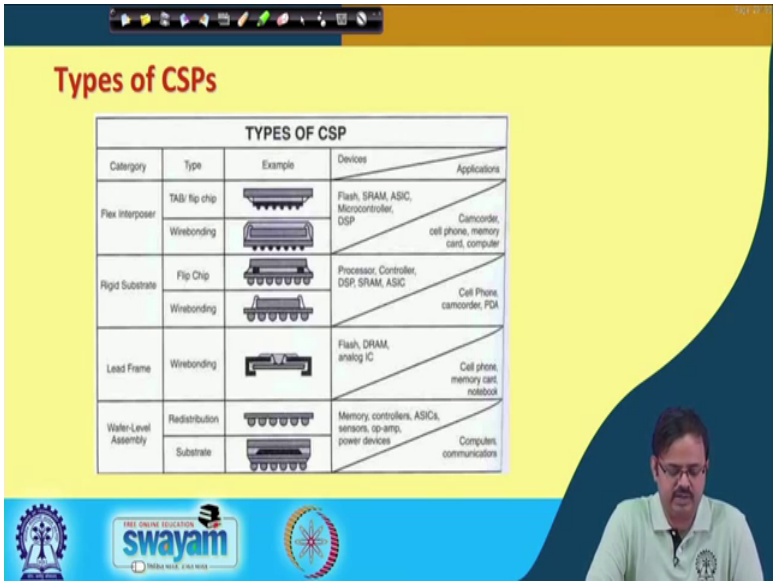

These are also types of CSPs again the same things that are being shown here several examples; flex interposer, rigid, substrate, lead frame and wafer level. Wafer level just let just let me tell you just give you a brief idea of what wafer level is.

Here actually the interconnections whether it is soldered balls or whatever happens right on the wafer, it is even before dicing the wafer into small dice ok. And then along with that it is after that after this assembly it is cut and put on the package or on the motherboard that is called wafer level assembly alright. So, we are as I said I will just flash this I will keep this on the on the slide, by the way this I forgot to mention the

source this is from the book from Rao Tummala fundamentals of packaging; fundamental or microelectronics packaging sorry.

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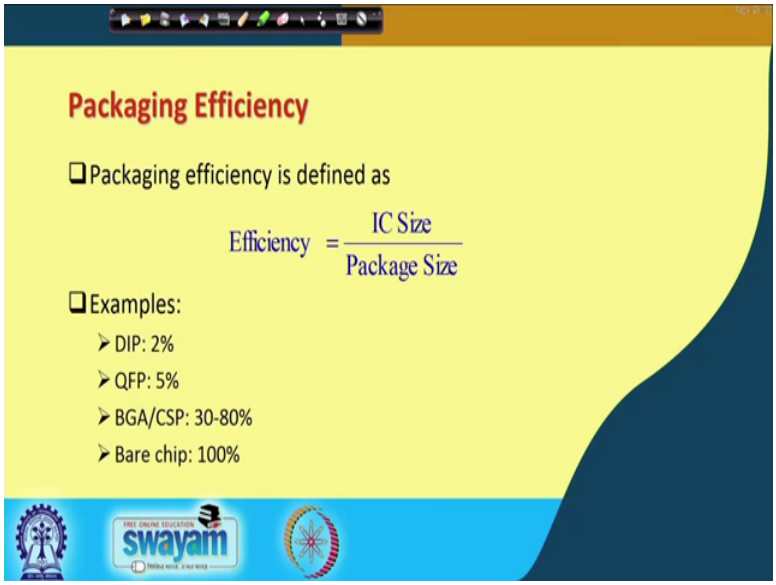

So, there is a definition of what is called a packaging or there is a there is a expression called packaging efficiency, which is this efficiency is IC size over package size ok. And if you look at some of this is a dual inline package that is the huge. The package IC is only 2 percent of the package size, quad flat pack 5 percent. If you go to ball grid array or CSP that is 30 to 80 percent CSP especially as I said 1.2 times.

So, it has to be bit more than 80 percent and bare chip if you just take it and put it on the motherboard no substrate nothing, direct bonding of the piece of silicon directly on the motherboard that is 100 percent. That typically as of now if you are wondering how is it possible because from the chip I have to take out these connections to wire bonding on the on the leads.

So, till now whatever we have discussed a bare chip with 100 percent packaging efficiency, we have not seen and based on the technologies we have discussed so, far it is not possible, but in the next class we are going to talk about a technology called flip chip. And in there we will see that how a bare chip bare chip connection directly on the motherboard is possible and in which case the packaging efficiency would be 100 percent.

So, that kind of brings us to the end of this lecture.

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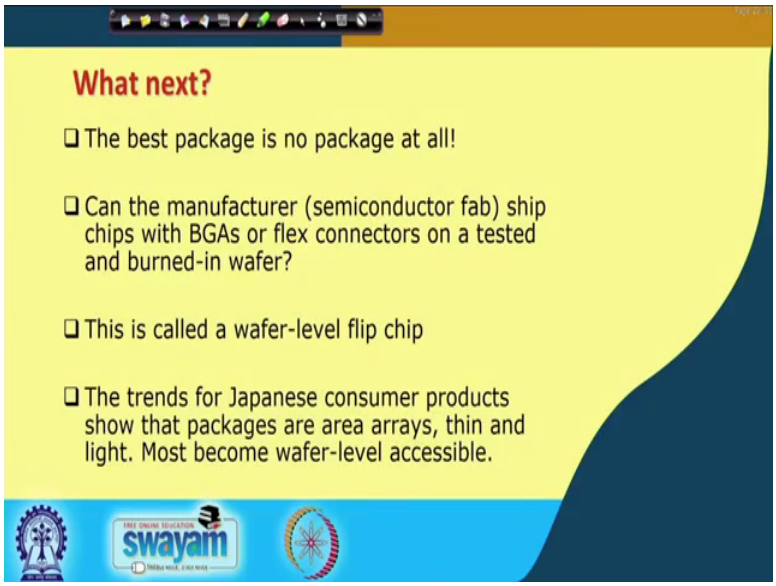

What next? The best package is no package at all ok; so the kind of manufacturer ship that chips with BGA flex connectors on the test and burnt in wafer. So, as I was talking about, can you have the connections directly on the wafer? And this is called a wafer level flip chip ok. So, that looks like a trend right now on has been a trend actually for some years ok.

So, we will discuss a bit about this especially when we talk about flip chip alright. So, for now thank you very much and we will continue this in the next lecture.

Thank you.