

**Indian Institute of Technology Kanpur**

**National Programme on Technology Enhanced Learning (NPTEL)**

**Course Title**

**Manufacturing Process Technology- Part- 2**

**Module- 03**

**Silicon growth & Crystallography**

**by**

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Hello and welcome to this manufacturing process technology part 2 module 3. We were talking about the various silicon structures particularly at the crystal level and how you are representing some of the structures. Let us now talk about another issue which is regarding the first, a very important issue in silicon which is how to grow these crystals, you know, so that you can make single crystalline silicon wafer.

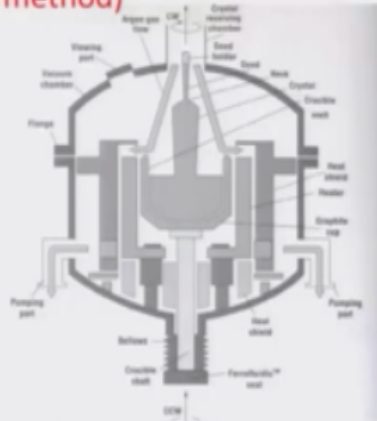
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## Single Crystalline silicon formulation (Czochralski's growth method)

- Single crystal silicon is formulated with Czochralski growth method.
- A small seed crystal with a given orientation is dipped into a highly purified silicon melt.
- The seed is slowly pulled out of the melt while the crucible containing the melt is rotated.
- The material is polycrystalline silicon and is 99.9999% pure.
- The poly is loaded into a fused silica crucible that is contained in an evacuated chamber.
- The chamber is back filled with inert gas and the crucible is heated to 1500 deg. C.
- The seed crystal is a small chemically etched crystal lowered into contact with the melt. This must be carefully oriented since it will serve as the template for growth of the much larger crystal.



So the various processes which are involved in the first process which actually comes into pictures also known as the Czochralski's growth method okay.

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### Czochralski's Growth Method

The diagram illustrates the Czochralski growth method. On the left, a detailed cross-section of the apparatus is shown, including the crucible containing the melt, the seed crystal, the growth interface, and the rotating mechanism. On the right, a schematic shows a blue rectangular block representing the growing crystal. An upward arrow labeled  $Q_2(x)$  indicates heat flow from the crystal towards a temperature  $T_2$ . A downward arrow labeled  $Q_1(x)$  indicates heat flow from a temperature  $T_1$  towards the crystal. Below this schematic, a note states:  $T_1 > T_2$  direction of heat flow is from  $T_1$  to  $T_2$ . At the bottom left, a small diagram shows a cross-section of the crystal with a temperature gradient, and the Fourier's law equation is given as  $Q(x) = -kA \frac{dT}{dx}$ .

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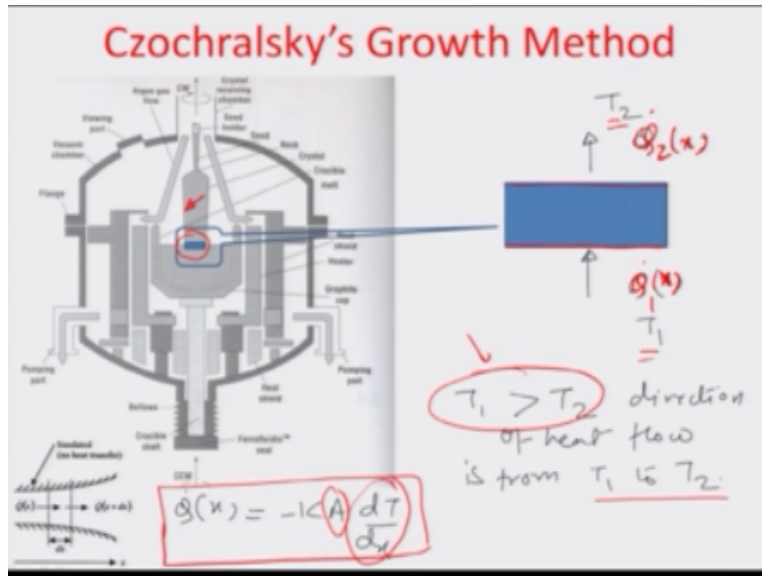
the process of, you know the growth of silicon or when the silicon is converted from melt into solid.

The material that is used is polycrystalline silicon which is 99.99% pure is very, very highly pure the hardly any impurities present and, you know the poly is loaded into this crucible right here which is made up of few silica, and it is able to go at a very, very high temperature. The chamber is back filled with inert gas after it has been evacuated, and is heated up to about 1500°C which is actually the melt point for the polycrystalline silicon.

So as the seed is pulled out there is a tendency of freezing which happens around seed and it creates this kind of a shape right here okay. So as soon as the seed is started to pull out there are some virtue of the shear between the layers of the seed which is a stationary or maybe rotated in the other direction and the melt pool which is actually rotating in a different direction, there is always a tendency of the liquid to cling on to the seeds surface.

And as you pull out the seed there is a change suddenly of the temperature which solidifies what is being pulled out. So that is how this bound right here is created okay, so this is like a silicon bowel which has to be later on trimmed and diced through a wire sewing process creating small, you know 200 to 500 micron thick wafers for single crystalline silicon.

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So if we look at this heat transfer problem really it is about this particular zone which has, which is actually a solid liquid interface where there is a rate of heat which, so this is only a one dimensional analysis very, very simple analysis. Although typically people have shown, you know the heat transfer and the solidification to take place in all three directions. So you have a heat rate at which, let us say  $Q_1 \cdot x$  which is being generated from the solution into the interface.

And there is a  $Q_2 \cdot x$  which is actually the heat flowing out of the interface into the solid side of the silicon which is this side right here okay, of the crystal side. So we can assume the causative temperatures to be  $T_1$  and  $T_2$  on both the surfaces of this interface, and we know that from the Fourier's law that the rate of heat transfer is a function of in a particular direction as a function of  $X$  is proportional to the temperature gradient that exists  $dT/dX$  in that particular direction.

And it is proportional also to the area of the interface across which the heat is flowing. So in this case the area of the interface is really the area of this lower phase as well as the upper phase and they are same to each other. Obviously the heat should flow between, you know from a higher to a lower temperature which means that  $T_1$  is always greater than  $T_2$  which is actually the case because the  $T_1$  is temperature on the liquid side, and  $T_2$  is that on the solid side. And the direction of heat flow obviously ifs from  $T_1$  to  $T_2$  in this particular case.

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Assuming completely no movement heat flow.

$$\dot{Q}_1 = -k_L A \frac{dT}{dx}_L \quad \dot{Q}_2 = -k_S A \frac{dT}{dx}_S$$

*Heat conduction*

$$\dot{Q}_1 - \dot{Q}_2 = \left[ -k_L A \frac{dT}{dx}_L + k_S A \frac{dT}{dx}_S \right] = L \frac{dm}{dt}$$

A is the cross-sectional area of the zone of fusion  
 $\frac{dT}{dx}$  is the thermal gradient in 'x' direction  
 $k_L$  = thermal conductivity of liquid  
 $k_S$  = thermal conductivity of solid

So let us look at the one dimensional heat flow problem. So let us assume completely one dimensional heat flow. The total amount of heat which flows from the liquid  $Q_1$ . okay which I have shown before is given by minus thermal conductivity  $K$  of the liquid melt times of the interface area  $A$  times of  $dT/dX$  which would exist on the liquid side. And that on the other side of the interface which corresponds to the heat loss from the interface into the solid okay, can be represented as  $-K$  solid times of the area  $A$  times of  $dT/dX$  on the solid side okay.

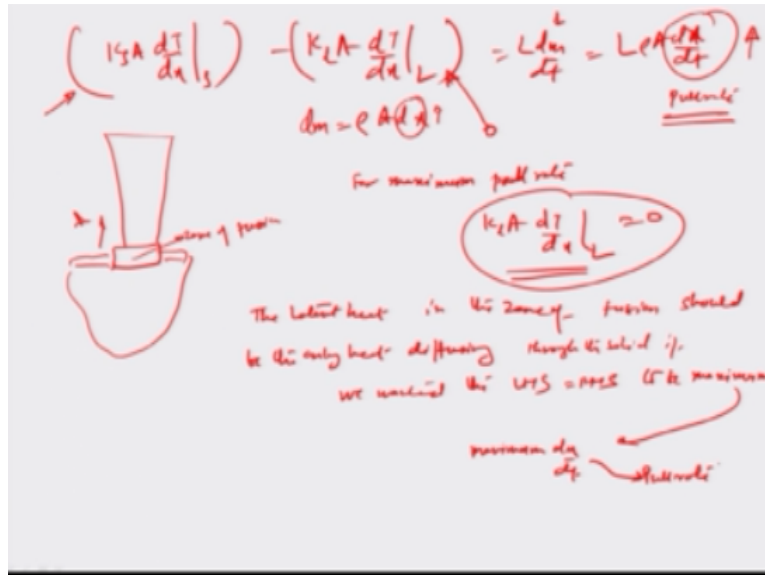
So the total heat flow which would happen in this case is  $Q_1$  coming into the interface  $-Q_2$  which is going out of the interface. In other words we can talk about this as  $-k_L A \frac{dT}{dx}_L + k_S A \frac{dT}{dx}_S$  and if this amount of heat is sort of flowing out you could say that this is the kind of, you know heat which should really be needed for the state conversion. And so, this much amount is actually deployed in making the bond energy of the solid phase over the liquid phase.

And this can be given by simply the rate of mass formulation  $dM/dT$  times of the latent heat of fusion or solidification as you may say. So if we assume in the reverse direction that we are, let us say trying to have a process where by lowering a bowl into the crucible you are melting it. So you essentially giving this much amount of energy right about here for the solid to get converted into liquid.

So this is the latent heat of fusion solidification times of  $dM/dT$  which is the mass rate of formulation okay. So you can say that  $A$  is the cross sectional area of the zone of fusion  $dT/dX$  is

the thermal gradient in X direction, and  $K_L$  is the thermal conductivity of liquid  $K_S$  is thermal conductivity of solid okay.

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So that is how you can place this if we want to change or simplify this equation a little more we write this as  $K_s A dT/dx_s - K_l A dT/dx_l$  okay becomes equal to  $L dM/dT$  where  $DM$  is actually nothing but the density times  $AdX$  assuming  $dX$  is the amount which comes out at a certain instance of time. And so I can actually change this into  $L \rho AdX/dT$ . So having said that if you wanted to really maximize the  $dX/dT$  which is nothing but the pull rate okay, the amount of silicon that you can actually pull out of the melt per unit time okay.

So  $X$  is actually the direction of the heat flow and as I had illustrated earlier here right here, let us say if I was talking about this as a bowl and this is the interface zone and, you know this some kind of a liquid melt boundary. So from the zone of fusion which is here, the pull rate is really in the direction of the heat flow which is this direction. So we can actually just write here that for maximum pull rate.

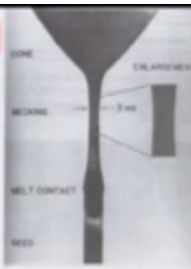
This term right here needs to be zero, so in other words we can say that  $K_l A dT/dx_l$  which is actually the heat coming out of the solution okay is to be zero. Or in other words whatever heat is flowing out is really because of the state conversion that is all what we want for the pull rate to be maximum.



So mathematically again we can write this, you know as that the latent heat in the zone of fusion should be the only heat diffusing through the solid if we wanted the LHS and RHS to be maximum okay, which corresponds to the maximum  $dX/dT$  or the pull rate.

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**Czochralski's Growth Method**



$$V_{max} = \frac{dx}{dt} = \frac{KA}{L} \frac{dT}{dx}$$

$$= \frac{K}{\sigma L} \left. \frac{dT}{dx} \right|_s$$

$V_{max} \propto \left. \frac{dT}{dx} \right|_s$

- In reality, the maximum pull rate is not normally used.
- The crystalline quality is a sensitive function of the pull rate.
- The material near the melt has a very high density of point defects. So quick cooling would help to prevent these defects to go into the forming crystal.
- However, too much gradient may create large thermal stresses and thus dislocations, particularly in larger diameter wafer.

So having said that then we can very easily write the velocity here  $V_{Max}$  as  $dX/dT = KA/L$  where  $L$  is this latent heat of formation the solid times  $dT/dM$  okay or in other words you can actually write this as  $K / \sigma L dT / dx$  of the solid silicon so typically what we see here is that the  $v_{max}$  is  $\propto$  to the temperature gradient on the solid side which means that if I wanted to increase the temperature gradient I would be typically increasing the pull rate which happens but it happens with a certain kind of trade-off.

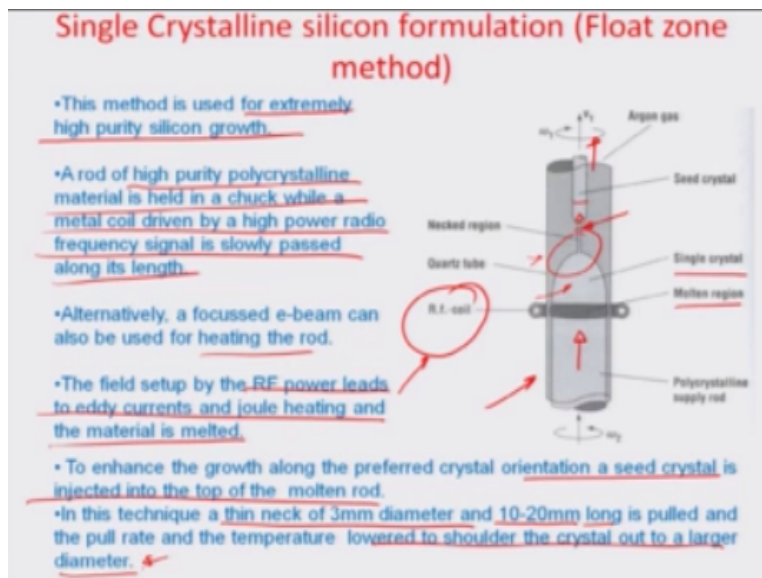
So because in reality the maximum pull rate is not the one which is normally used because you know the crystalline quality formulated we are talking about mind you single crystalline silicon it is a very sensitive function of this pull rate and you can think of that the materials near the melt would have a very high density of point defects and so rapid cooling or quick cooling which is done through increased  $dT/ dx$  you know would prevent these defects to go in formulating the crystal on one hand but may create large thermal stresses.

So there is really a trade-off between how much crystal distortion or lattice distortion you want to have vis-à-vis the pumping in of the defects and so therefore these are the two physical conditions which lead to the arrival at an actual pull rate you know which would be able to

define and what rate you can produce silicon okay, so this again particularly in large diameter wafers is a big problem to determine the very accurate pull rate which can free the material off the thermal stresses of the thermal defects on one hand and also make it free of the point effects which my other ways go in because of a steep.

So which one otherwise go in because of a relatively smaller  $dT / dx$  value so having said that so this we understand is one method of the crystal growth for single crystalline silicon there are many other methods one of them is the float zone method which is illustrated right here where we need not really use a thermal wall or a thermal boundary to heat a mix this.

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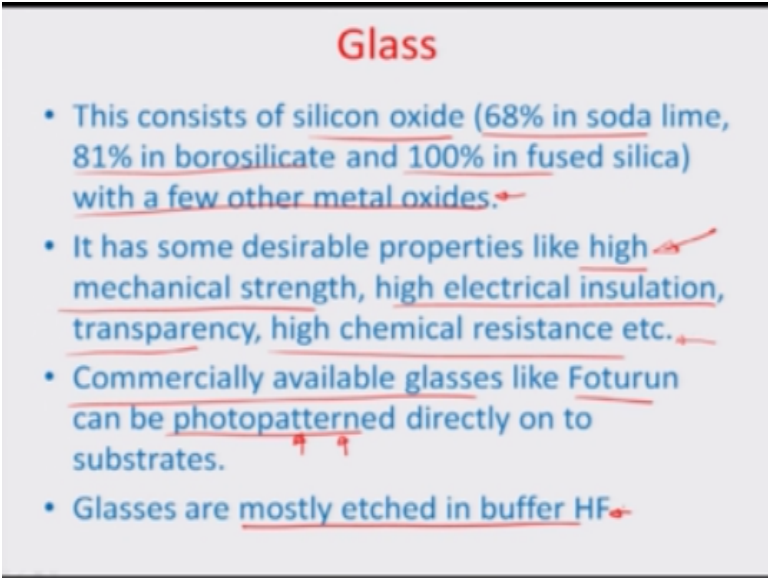
In this case it can be heated through you know in a non-contact means by using some kind of a radio frequency signal and creating eddy currents so that there is a uniform heating to the material okay so you have single crystal material you have again a molten region which is formulated because of an RF coil and there is a quartz tube and there is a neck region, so the seed crystal is lowered somewhere here and there is a fusion of this at this particular zone because of the high heating and you are pushing the rod the polycrystalline rod into this orifice or this cavity

so that more melt is formulated and the melt goes out while the silicon and crystal is pulled and so there are mutually rotated.

So this method is used for extremely high purity silicon growth because the because of the controlled delivery of the molten silicon over the seed and a rod of high purity polycrystalline material is held in a chuck while a metal coil driven by a high-power radiofrequency signal is slowly passed along it is length alternatively a focused e-beam can also be used for heating the rod.

So the field set up by the RF power leads to eddy currents and joule heating and the material is melted to enhance the growth along preferred crystal orientation a seed crystal is injected into the top of the molten rod and in this neck in this technique a thin neck of 3 mm diameter and 22 sorry 10 to 20 meters long 20 mm long is pulled and the pull rate and the temperature lower to shoulder the crystal out to a larger diameter okay. So that is how the float zone method of the formulating the silicon is made.

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**Glass**

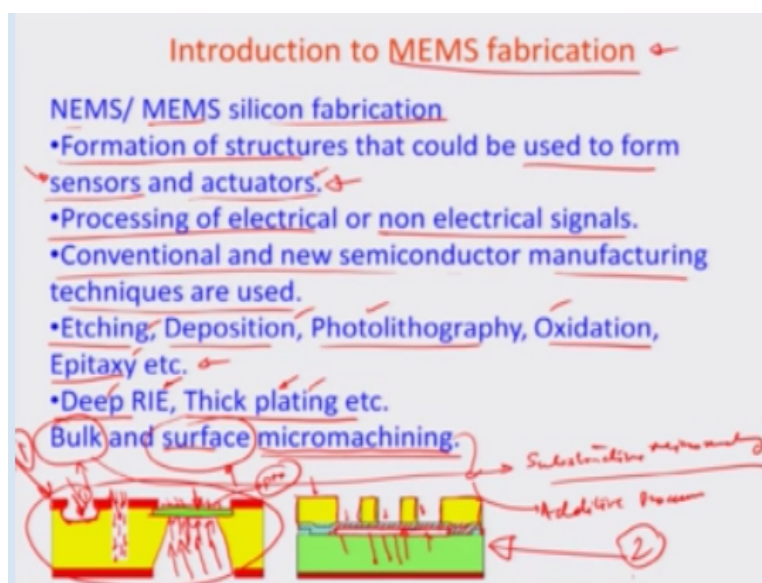
- This consists of silicon oxide (68% in soda lime, 81% in borosilicate and 100% in fused silica) with a few other metal oxides.
- It has some desirable properties like high mechanical strength, high electrical insulation, transparency, high chemical resistance etc.
- Commercially available glasses like Foturun can be photopatterned directly on to substrates.
- Glasses are mostly etched in buffer HF.

I would also talk about little bit about glass because glass is a very important constituent of micro systems fabrication it consists of silicon dioxide which is 68% in soda lime 81% in borosilicate and 100% in fused silica and they have other few metal oxides and sometimes contaminants it has am a desirable property is like high mechanical strength high electrical installation, transparency, chemical resistance which qualifies it to be part of micro systems

particularly when we are talking about the you know the diagnostic micro systems where there is always a conversion of a chemical signal into an optical signal which needs a transparent material to pass through to read out you know.

So there is a they are commercially available glasses like photon which is which can be photo patterned directly I am going to talk about this photo patterning a lot when we start doing photolithography just in a few slides, so they can be directly for the pattern onto the substrate there is like a glass epoxy where you know wherever there is the epoxy bonding takes place by means of you know light of a certain signal glasses are mostly etched in buffer HF and that gives you very controlled you know chemical process where the glasses slowly get dissolved in the buffer as a patch of solution.

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In fact buffer chip is used for a variety of other substrates like even silicon to create some etching action on the on the silicon surface, so now let us come up to the fabrication processes which are the sort of first generation non-traditional processes used with an intention of changing silicon into various shapes and sizes on micro sizing the silicon, so you know in particularly the micro systems or the nano systems silicon fabrication process it involves the formation of structures that could be used to form particularly some sensors and actuators okay.

Because sensors you know typically would be very accurate and so would be the actuators because the masses involved a small so low inertial component would always mean higher

resolution or higher sensitivity and typically these structures would process some electrical or nonelectrical signals which would be associated with sensing or diagnosing certain aspects which are either physical chemical or biological in nature.

And then you know you can use the conventional and new semiconductor manufacturing processes for realizing such systems they may include things like etching deposition photolithography, oxidation, Epitaxy and then there are some specific processes for the micro systems which are including deep reactive ion etching and thick plating, so I am going to focus a lot on some of these techniques okay as we go along and help you to realize that how these micro systems can be formulated using the first generation advanced machining processes.

So when we look at the whole area of micro fabrication there are in fact two different kinds of micro machining which are available one is called bulk micromachining another is called surface micromachining and as the name indicates bulk means it is a subtractive process so you know you can even call it a subtractive micromachining and as you can see here in this first example we are trying to remove material is removed in this area for example or in this area or this area.

So how do we remove it is again another very interesting story that we have an etchant which works selectively, so you have in this particular case some kind of sacrificial layer which has been built up this could be something like a let us say you know a poly silicon layer which is not affected by a particular agent, so whenever we have opened a window in this poly silicon layer the etchant would go inside and it would start affecting the yellow portion which is the normal silicon right.

Similarly you could do the same thing by means of you know a plasma which is actually the fourth state of matter but it is in gaseous form and I am going to teach you a little more bond on the plasma systems as well that how they are formulated or are they manipulated but it is actually fast moving ions and you could go up to a certain depth with a high aspect ratio which is needed and what you also know as deep reactive ion etching okay you could also do the same thing with a let us say a P<sup>++</sup> or you know a very highly doped silicon layer which is reflected by this green region.

And when you are doing the etching you have from the back side here the similar principle as applied in the front you know etching here in this particular module but what happens is that this

etchant goes all the way up to the green layer and stop so typically this P++ layer that we are generating here is a H top layer that means the chemical which is used to etch off can etch off only the yellow but whenever it meets the green the etching stops completely okay.

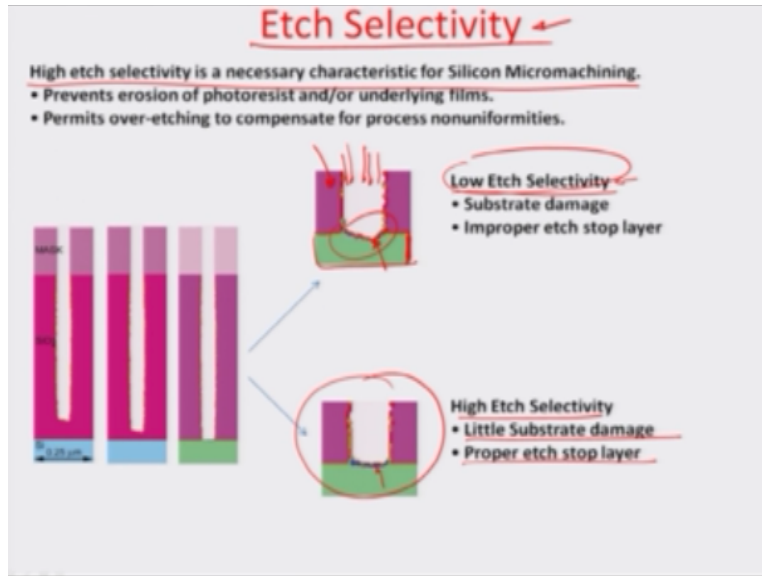
So you are able to release this thin membrane right here represented by the green and you could use it for various purposes like pressure sensors or you know some other means, so all you need to do is to put another piece of layer on the top of this green membrane through MEMS fabrication so that whenever there is a deflection of this membrane due to a ambient pressure on the back end of this green membrane you could be able to get an electrical signal.

And so you could calibrate the pressure with respect to that electrical signal, so these are all subtractive micromachining also known as bulk micromachining in the other hands we have surface micromachining which is more additive in nature, so these are additive processes for example let us say this is an additive process right here is very interesting how you built it so we have some kind of a sacrificial material which is which was initially patterned in this region and the sacrificial material as the name indicates is something which has to be sacrificed that means chemically you're able to dissolve this material out later on.

Let us say if there was a photo resist that we wanted to pattern in this particular region so we would lay out this photo resist and typically deposit another thin film which is represented by this green lines right here okay, so this is another thin film maybe it is a poly silicon material which is either grown in IFPCVD or a LPCVP and I am going to come to these details just in a few you know slides so you deposit this thin film and then sacrifice this material that means you take off this material.

So you have a embedded or a buried channel which is their similarly in this particular case you are generating a deposition at a certain region let us say of gold or some other metal which is generating these pillars you know on the top of it so you essentially not removing subtractive but adding and adding to the surface, so these are additive micromachining processes and that is how you call this domain surface micromachining so it is very clear the bulk is a subtractive process as I showed you in case one here.

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And the surface is a additive process as I showed you in case two here okay, so having said that you have now an idea of what really is this micromachining all about and let us look into the first process which is about chemical etching or you know chemical milling as you can say of these silicon structures, so what I would like to illustrate here is a very important parameter called etch selectivity and this is how we start the etching process obviously I need not define it anymore that the etching is a process of engraving on a material.

So there is a chemical and there is some kind of an impact of dissolution of the material that you know the chemical comes in with and so it is some kind of a you can say a chemical dissolution for example if there was a metal and you were putting an acid on the top of the metal almost immediately it would start affecting the atoms and the molecules on the surface of the metal and it would typically dissolve into the acid and create some kind of salt and you would typically see an area which is engraved or formulated because of such an etching module.

So a higher selectivity is necessary characteristic for silicon micromachining and it prevents erosion of photo resist and underlying films you can see here for example is showing two different cases, so if I have a module which has a low etch selectivity let us say there is a green layer here which is a H top layer that means the agent is not going to affect this layer any more it is only going to affect this purple layer okay so when we are etching this from the top side and the chemical is going down as you can see here the moment the you know material is encountered.

The etching typically should stop but if the material if the asset that is in question or the etchant that is in question has a low at selectivity for this material it will still damaged the material and they will be creating a pitting action on the top of the material surface however if it were having a high selectivity higher selectivity you would have little substrate damage you can see this is more flatter in comparison, to what was here this was eating away into the green material but here you do not find much eating into the green material.

So you have proper edge stop so choosing the in a micro machining process choosing the accurate f-stop to happen would define what is the kind of surface roughness that you are initiating on top of a surface, so I think I am to the end of this module with this I would like to close this particular module and the next module you would like to start doing a little bit of you know what etches what or for example what is selective to what and what would be the basic mechanism for etching in that particular case with that I would like to end this module thank you so much.

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