Advanced Neural Science for Engineers
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Lecture 06
Silicon and Silicon Dioxide

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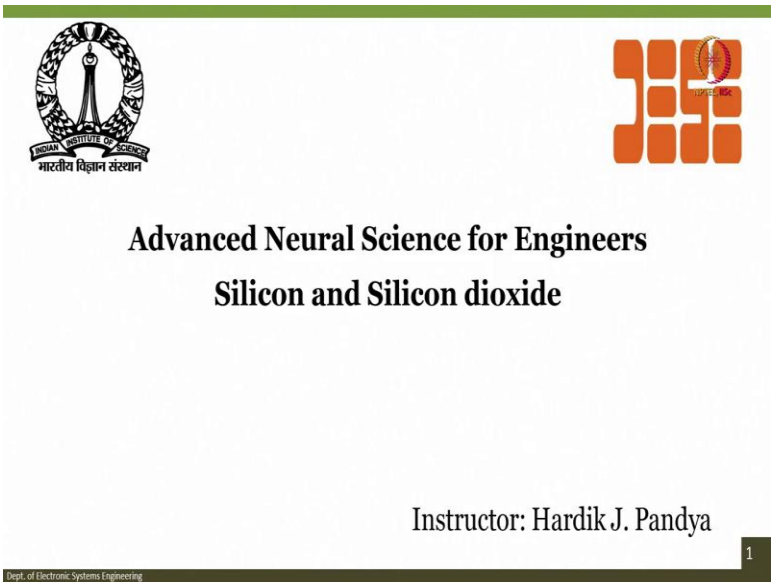

Hi everyone. So, this is the next lecture in the series, where we are understanding the advanced neural science for engineers course. So, we need to understand first of all that what kind of different devices and sensors we can fabricate that can be used for this particular course.

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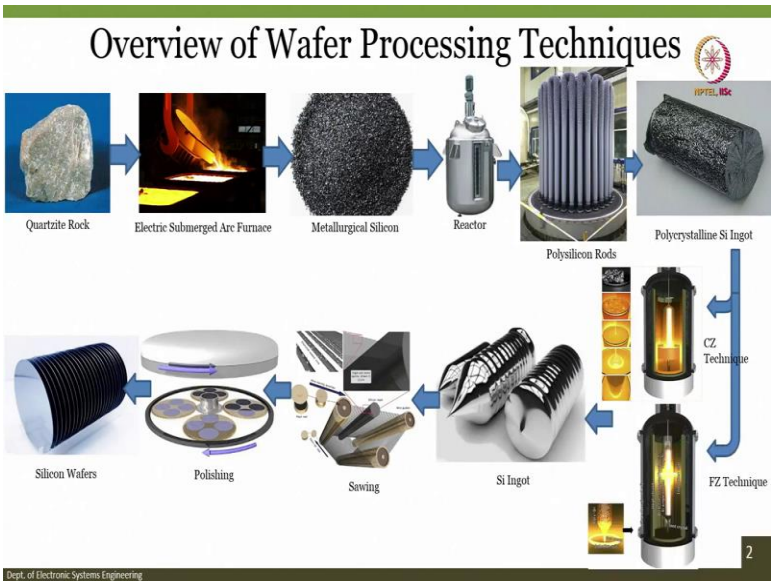

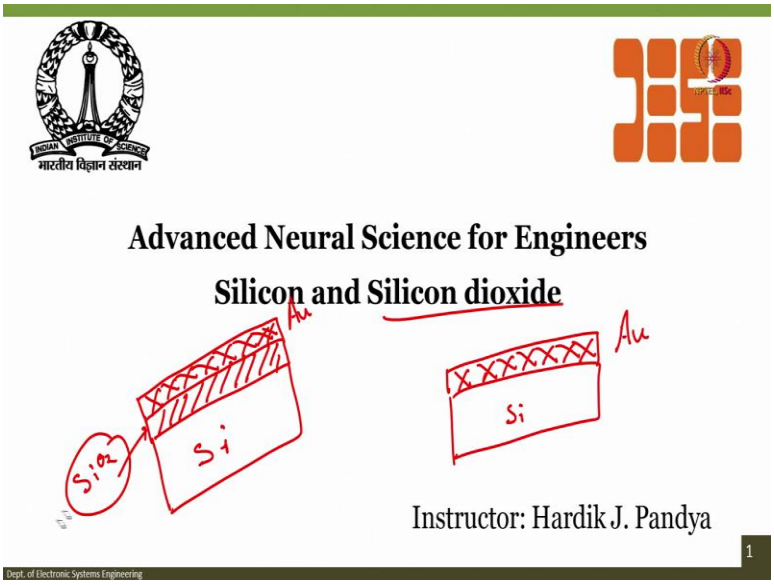

So, we will look into the overview of wafer processing technique, but before that, let me just draw some things for you. So, what we call silicon, the silicon that you see here, I will draw here. So, I asked many of my students when they apply for even PhD, a draw cross section of silicon it is very easy, this is a cross section of silicon how you draw, let us take a cross section, that is it.

So, anyways, the point is, silicon is a substrate, silicon is a semiconductor material and silicon can be used as a substrate what is substrate, substrate is anything over which we are going to fabricate our device is a substrate.

Silicon can be substrate which is semiconductor you can have metal substrates, you can have silicon dioxide, why silicon dioxide there was a reason of having silicon dioxide and not only silicon, silicon is a semiconductor dioxide when you say silicon dioxide there is a oxygen on silicon which is which forms sio2, how it will form sio2 we will go through the through the mechanism, but this is silicon dioxide or oxidized silicon wafer we call it as an oxidized silicon wafer sio2 is an insulator silicon is a semiconductor.

Now, if I directly deposit on silicon a metal this is let us say gold what will happen there will be short circuit there will be short circuit that is why I cannot directly deposit gold on silicon, metal on silicon any metal on silicon. So, what I will do I will have my silicon dioxide layer on silicon over which I will deposit gold.

Now, what will happen? Now, you do not have any short circuit, because you are depositing gold on the insulating material. So, that is how the things are done. Now, this is silicon and silicon dioxide just now, let us focus only on silicon and silicon dioxide, but the question is from where we can have silicon how can we get the silicon wafers.

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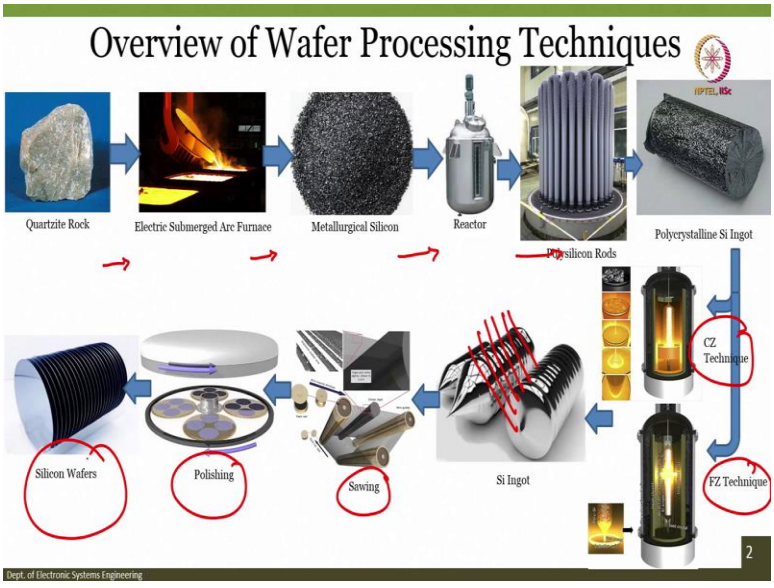

So, there are two different techniques one is called CZ technique also Czochralski technique second is called float zone technique (FZ) float zone technique and Czochralski technique. So, you start from the quad side rock and then you have electric submerged arc furnace, you can get

your metrological silicon then there is a reactor polysilicon rods so polycrystalline Si Ingot, then while using CZ technique either you can fabricate different ingots or using FZ technique and fabricating different ingots.

This is an overview you do not worry about it I will go in details point is that this is the fashion how the silicon wafers are made like this and it goes either through CZ technique or through FZ technique not both and each technique has its advantages and disadvantages or limitations.

Once you have this ingot you do the sawing so, and then polishing, sawing is cutting the silicon ingot into many wafers and then you do the polishing and finally, you have silicon wafers in a stack as you can see here.

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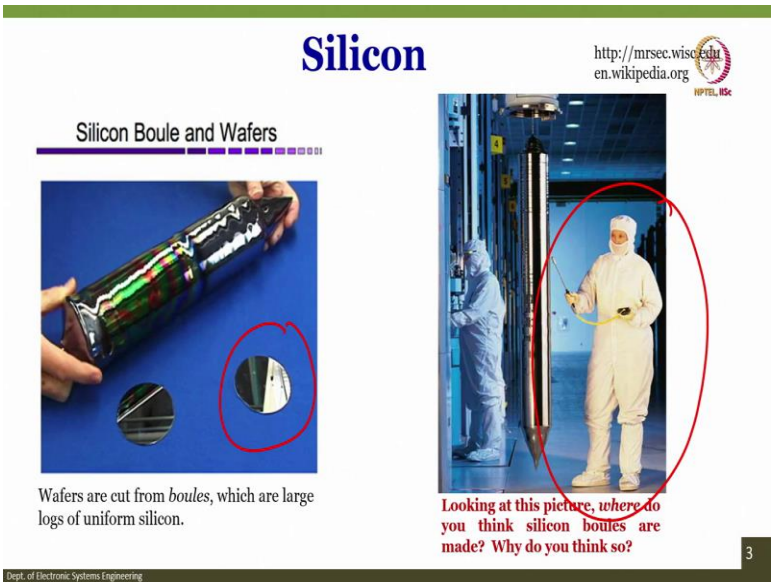

Now, silicon boules and wafers as you can see, we have a silicon boules and wefer, so wafers are cut from boules, which are large logs of uniform silicon. But the question is that looking at this particular image, where do you think Silicon boules are made, and why do you think so?

So, again, what do you see we have already learned in the previous class, what is this a gowning, gowning for what, cleanroom so, this is a cleanroom facility. So, now, if you want to make these

wafers out of this particular boules, you have to use the cleanroom facility. So, and then why cleanroom you already know to avoid any contamination.

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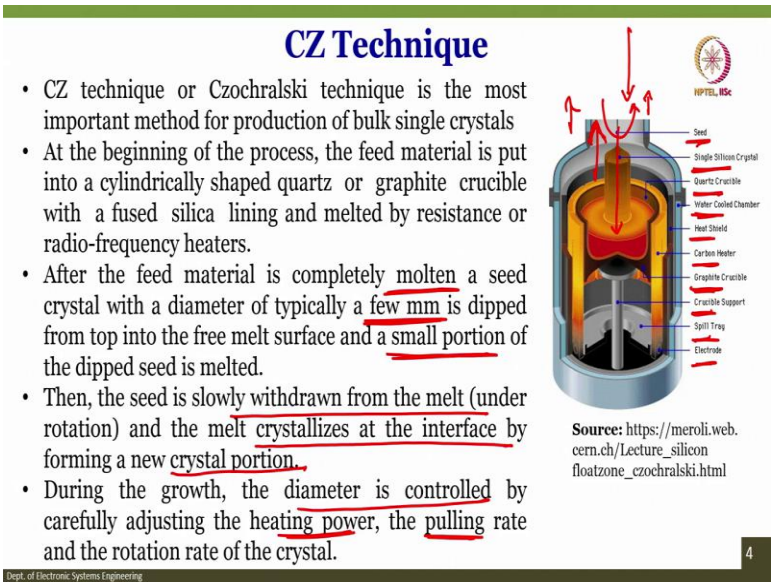

So, let us go for the first technique which is your CZ technique. In CZ technique or Czochralski technique, this is the most important method for production of single crystals and what how the process is done so before the process we should learn how the system looks like because this is one schematic of the system where you have the electrodes at the bottom then there is a spill tray, crucibles support, graphite crucible, carbon heater, heat shield, water cooled chamber, quartz crucible, silicone single crystal and seed crystal.

So, what you do is you keep on heating this silicone single crystal and depending on the seed crystal the rotation happens. I will show it how exactly this works as a video for that, but at the beginning of the process the feed material is put into cylindrical shaped quartz or graphite crucible which is right over here graphite crucible is this one this one.

So, it is the quartz or graphite crucible with a few silica lining and metal resistance so, that it can be heated with a radiofrequency or metal resistance, it can be heated with resistor heaters or it can be it can melted by resistance or it can melted by the radiofrequency heaters.

Now, after the free material is completely molten, which you can see here the seed crystal is slowly pulled up in this direction and the direction of cooling and the direction of the rotation of this the quartz crucible is totally different, it is in opposite direction. So, we will go through that

let us not worry about it right now, the point is that when it is in the molten state, you load the seed crystal and slowly pull it off, when pulling off, rotate it.

So, after the feed material is completely molten as you can see here a seed crystal with a diameter typically a few millimeters is dipped from the top in the free metal surface, a small portion of this deep seed is melted, after that what happens the seed is pulled off here withdrawn from the melt and melt crystallizes at the interface by forming a new crystal portion.

During the growth the diameter of the is controlled by carefully adjusting the heating power pulling rate and the rotation of the crystal like I said rotation of the crystal is faster, pulling rate is also faster then what will happen and the heating power is lower then you have or heating power you can change it then you will have a smaller boule or a crystal formation while if you have slow pulling rate, slow rotation rate, then you can have a bigger diameter correct. So, that is how it is done.

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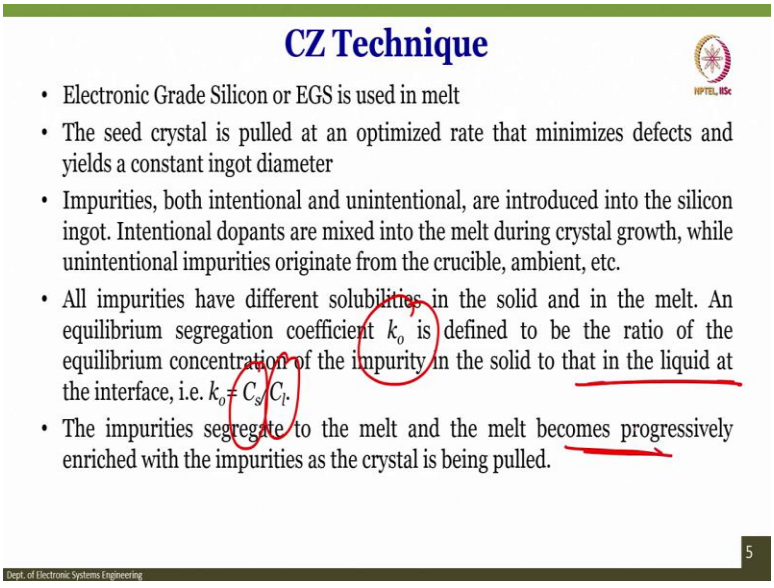

So, CZ technique is electronic grade for use for electronic grade silicon and the seed crystal is pulled at an optimized rate. So, like I said here like you are let us understand it a little bit slowly. So, the seed crystal is placed here once this molten region is there and then it is pulled. Pulled in this direction like this from the hot let us say this is hot to the cold side it is pulled when it is pulled it is also rotated like this.

So, depending on the pulling rate, and depending on the rotation rate, you can change the diameter of the crystal or the wafer and also electronic grade silicone (EGS) is used in this melt.

And what happens is that if you optimize this pulling rate, nd the speed your defects would be minimum your contamination or the defects would be minimum and you can have a constant ingot diameter, what does it mean if I do not have optimized rate my ingot will form like this it is not correct it is form like this uniform correct and the tape it will be like this. So, the rate of optimization the optimization rate for pulling the crystal is very important and so is the rotation speed.

Now, you have understood about extrinsic and intrinsic semiconductors. So, intrinsic semiconductors are semiconductors where there is no contaminants, but when you intentionally contaminate the wafer by doping it, it becomes an extrinsic semiconductor.

So, impurities both intentional and unintentional are introduced into silicon ingot and intentional dopants are mixed into the melt during the crystal growth while undesired impurities originate either from the crucible or from the ambient.

So, these are the different way of how the impurities are added depending on the impurity you can say it is N-type or it is a P-type, boron n if it is there is a p type impurity, phosphorus n type impurity because in boron you create extra holes in phosphorus there is extra electrons.

So, the all impurities have different celebrities in the solid and the melt and equilibrium segregation coefficient k_o is defined to be the ratio of equilibrium concentration of impurity in solid to that out the liquid.

So, if I have concentration C_s by content C_l so solid to liquid ratio, then I can find out the segregation coefficient k_o and impurity segregate the melt and melt becomes progressively enriched with the impurities as the crystal is being pulled. So, again, we can intentionally dope the wafer with either p type or n type material.

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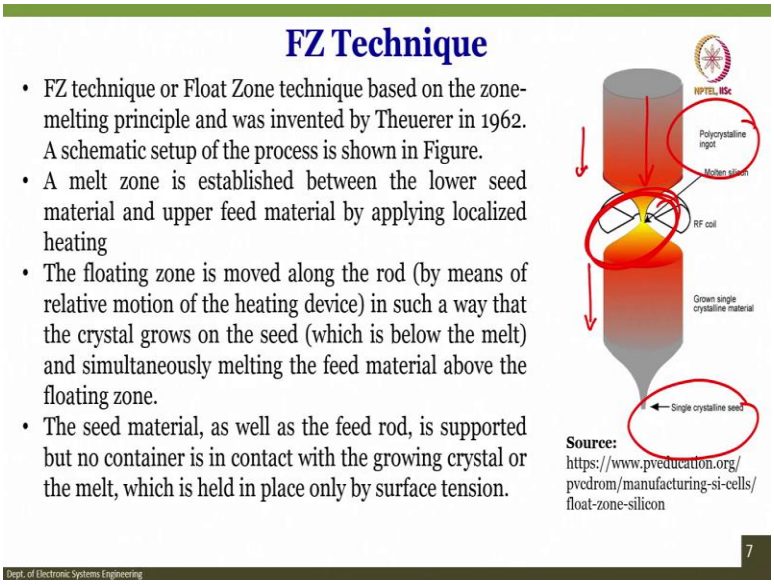

Now, this is from TU Delft, just let us play the video and then you will understand how the CZ technique works. So, you have seen the video now, let us see the FZ technique, you have seen the video so, let us see the FZ technique, in FZ technique, which is also called float zone technique this is different than the CZ technique.

Here based on the zone melting principle that was invented by Theuerer in 1962 the FZ technique works and in this technique, what happens is that the melt zone is established between lower seed material and upper feed material.

So, this is the feed material this is the seed material and there is a molten zone is created with RF heating RF coil is there and then the floating zone is moved. Floating zone is slowly moving along the rod by means of relative motion of heating device in such a way that the crystal grows on the seed.

So, just seed is just below the melt. So, simultaneously melting the feed above their floating zone. So, slowly and gradually as it goes towards the color region the it starts forming the things so you can see here, there is a single crystalline material, this is a polysilicon ingot in the molten zone as I told you that the lower seed material and the upper feed material this is the feed material this is a seed material and how the molten zone is created in this particular region exactly between two by the help of heating and the seed material as well as the feed rod is supported, but no container is in contact with the growth growing crystal or the melt which is held in place only by surface tension.

It is very important thing to understand that nothing is supporting in this case, if you see the CZ technique, there was whole support here in this thing see, but in the FZ technique, there is no support in that particular sense, the seed material as well as feed rod material is supported only by surface tension.

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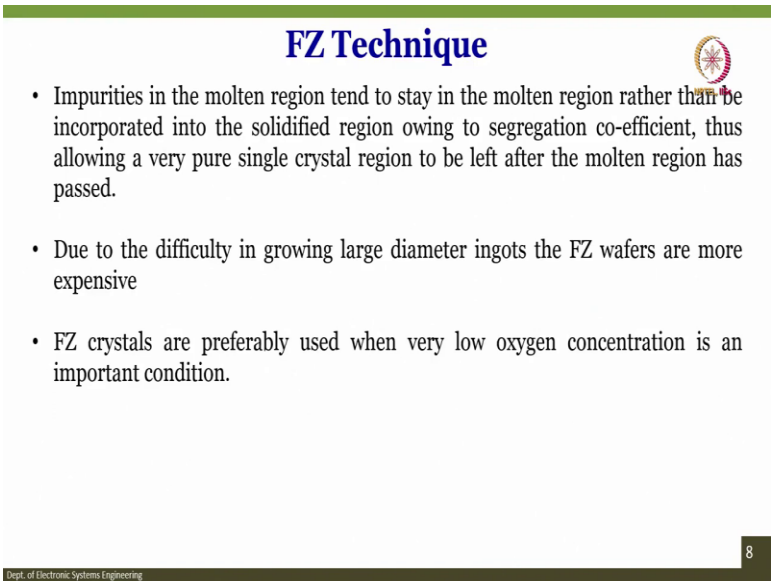

So, the impurities in the molten region thus tend to stay in the molten region rather than be incorporated into the solidified region owing to the segregation co-efficients thus allowing a very pure single crystals to be left after the molten region has passed.

So, that is the advantage of FZ region that you do not find contaminations or the impurities arising due to the technique, intentional impurities is different than the one then then the one that is because of the technique.

So, due to the difficulty in growing larger diameter because you see that in this case, the entire thing is depending on the molten region between the lower seed and the upper seed, you cannot have a bigger diameter wafers or ingots. So, the FZ wafers are more expensive, because the contamination will be extremely low. The FZ crystals are preferably used when very low oxygen concentration is an important condition. So, CZ technique FZ technique both has advantages like I said and limitations.

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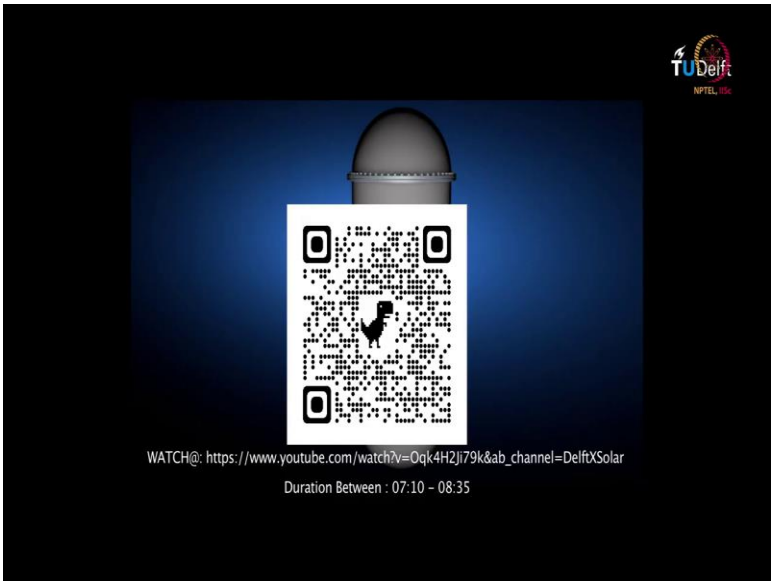

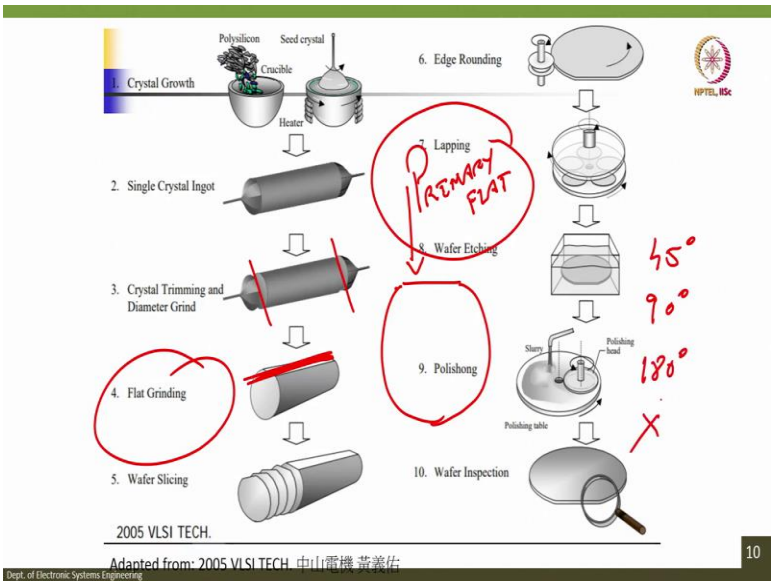

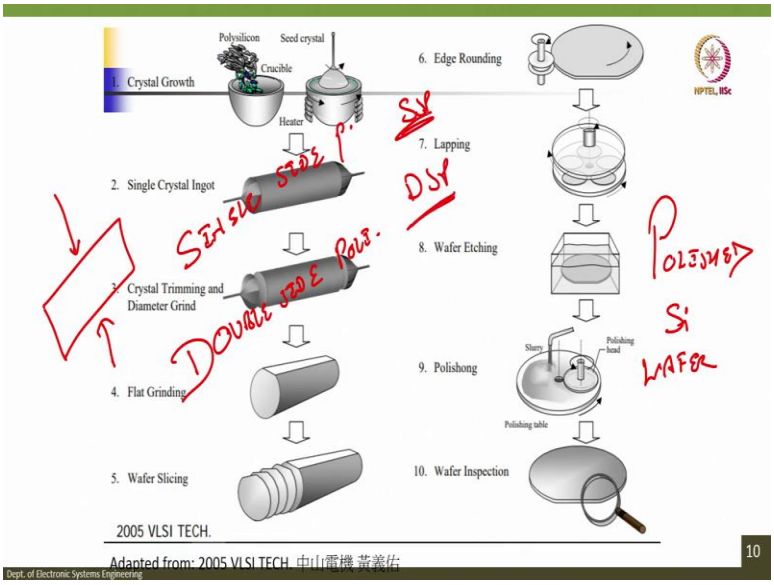

Now, let us see the FZ technique video so you have seen the video of the FZ technique as well. Now, let us understand the ingot, whether it is through CZ or through FZ, how we can create the wafer from the single crystal ingot, that is very important to create a wafer.

So, you start with a polysilicon and once let us let us come here, so once you have this single crystal ingot either through FZ or CZ, the next step is to trim it, trim the corner here, trim it and then to have flat grinding now, when you take any silicon wafer you will have something called one single big flat which we call as a primary flat and this primary flat is by creating a flat grinding here.

There is a reason of having primary flat and then there are secondary flats either at 45 degree or at 90 degree or at 180 degree or there is no secondary flat, depending on how the secondary flat is placed with primary flat, we can distinguish the wafer whether it is n type or p type where is 100 or 111.

So, after crystal trimming and diameter grind there is flat grinding so, to create a flat and then there is a wafer slicing now, when we should have wafer they should be polished. So, first we will go for edge rounding it should be completely round as you can see here and after that you can go for lapping followed by wafer etching followed by polishing.

So, this all thing will create a polished silicon wafe. Now, you will say what is polished silicon wafer, so, I will show you the wafer in the next class, how the polished silicon wafer looks like versus how the non polished silicon wafer looks like.

So, what happens is depending on a single side so let us say this is a cross section of silicon, if both the surfaces are polished, it is called double side polished wafer, if only one side, it is called Single Side polished.

So, SSP, DSP, single side polished, double side polished, silicon wafers the if it is double side polished is costlier compared to single side polished wafer, diameter is larger, it is costlier and also for creating this polishing, before polishing, there are steps like edge rounding, lapping wafer etching and then polishing and then finally, there is wafer inspection. You have a wafer inspection, whether the wafer is correctly developed from the single crystal ingot.

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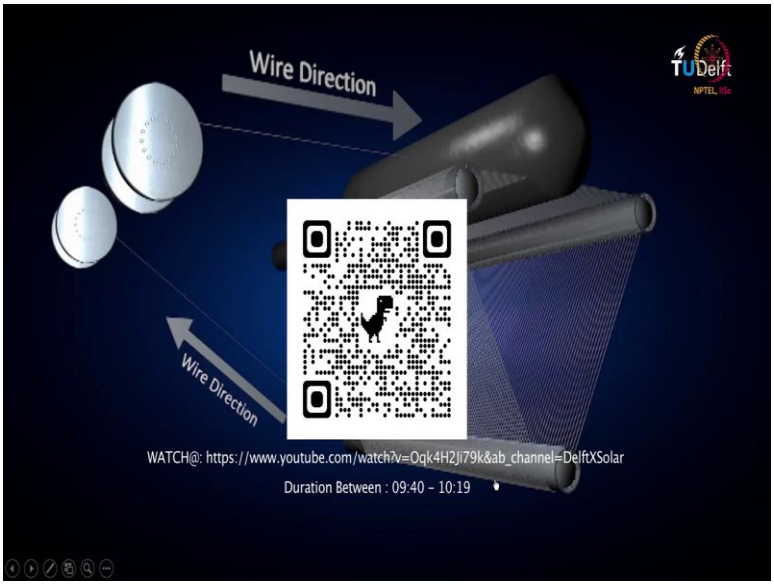

So, this is how the diamond wire, Diamond Coated wires are used to slice the ingot as you can see here it is slicing the ingot and this will create many chips and what happens after that you use this machine for lapping followed by the polishing as we discussed earlier, we want to go more understand more about this you can go to the microchemicals.eu and you will have a lot of interesting videos showing how the lapping mechanism works. This is one of the video from to TU Delft or how the wire direction is there and how the wafers are sliced or the ingot is sliced into the wafers.

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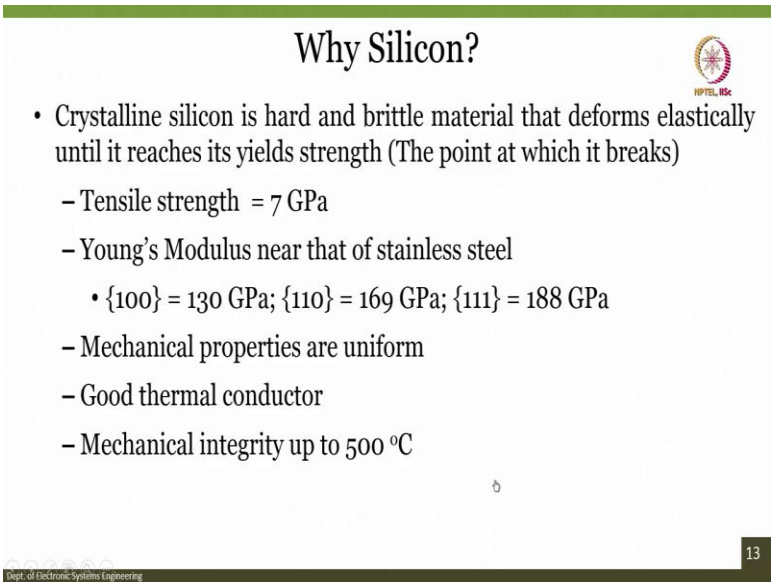

Now, the question is that we have discussed about FZ technique or we have discussed about the CZ technique, but the point is why we are discussing on silicon, can we use other materials as a substrate? So, answer is yes, we can use glass as a substrate, we can use Polymer as a substrate, we can use silicon as a substrate, we can use germanium as a substrate.

So, there are different substrates different materials for different substrates, but if you understand the silicon, then silicon is 90 percent of these devices. Similar devices are made up of silicon. So, single crystalline silicon and is hard and brittle materials that deforms in a CC until it reaches its yield strength.

So, the point at which it starts breaking so, it is hard, but brittle material also the tensile strength is about 7 GPa, Young's modulus about 188 GPa, mechanical properties are uniform, good thermal conductor and mechanical integrity is upto 500 degrees centigrade.

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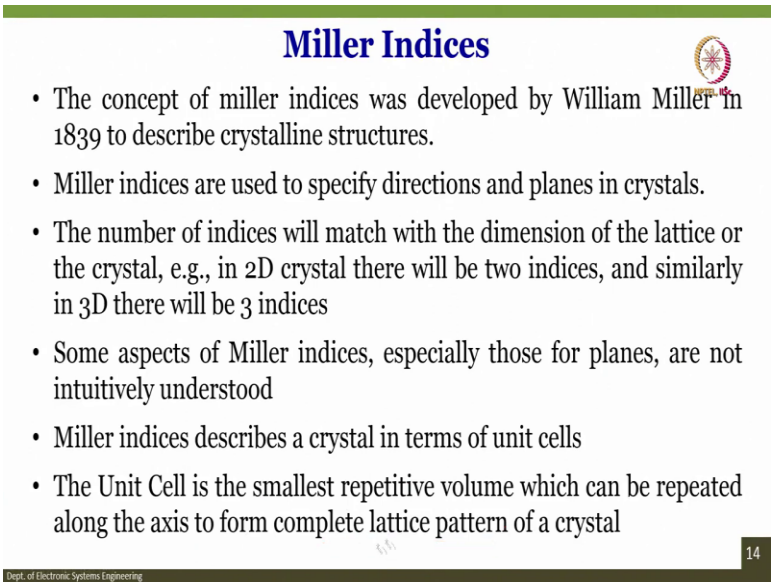

The miller indices if you understand the miller indices how the miller indices are given by William Miller in 1839 helped to define the crystals are described as crystal structures and in miller indices are used to specify the directions and plane in the crystal so, if you understand a unit miller indices is described as crystal in terms of unit cell, how the cells are there.

So, if you see something which is behind my back again on the screen the unit cell is the smallest repetitive volume, which can be repeated along the axis to form complete lattice parameter, lattice pattern and how it is defined.

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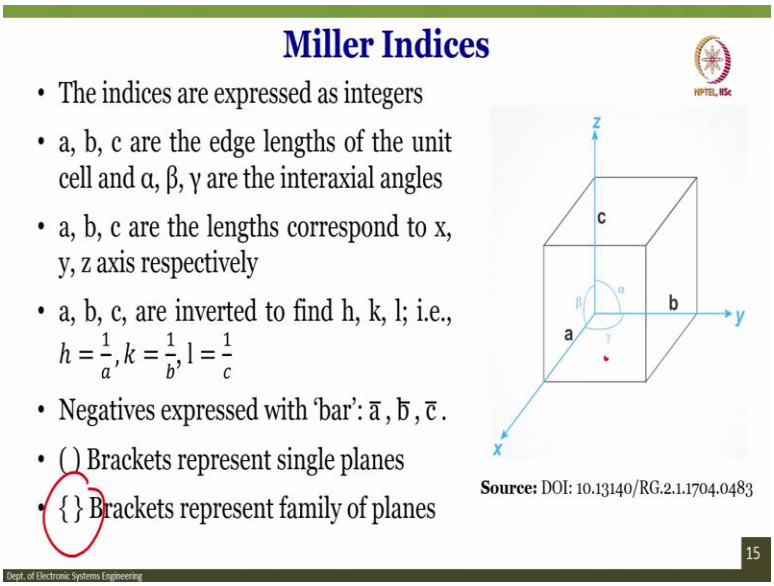

So, it is defined as if you see this particular cube, what you will have is A, B and C and A, B and C are the edge lengths, while the alpha beta and gamma are the interaxial angles. So, what will happen is that the ABC are inverted to find the h, k, l plane and h, k, l plane you can have either if it is negative then this expresses a bar b bar and c bar and the brackets are used for single planes, while the this particular bracket, this curly the bracket are used to familiar planes.

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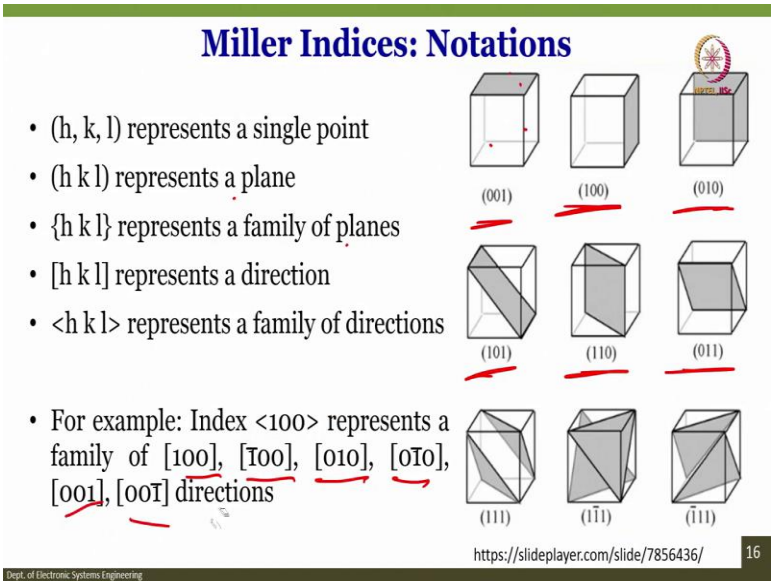

So, what does it mean? So, as for h, k, l represents a single point in this direction you can see it is 001 and here is 100 and here is 010 101 110. You have to define the crystal planes very easily. So, suppose if I write h, so there are different symbols if you write h k l represent single point, but if you write h k l without comas, it represents a plane, but if you write in curly brackets it represents familiar planes, in a square bracket it represent direction, but within this symbol like this, it represents a family of directions. So, depending on what kind of symbol you use, be careful, because 100 like this represents all the family 100 $1\bar{0}0$, 010, $01\bar{0}$, 001, $00\bar{1}$. So, all the family of the 100 can be used.

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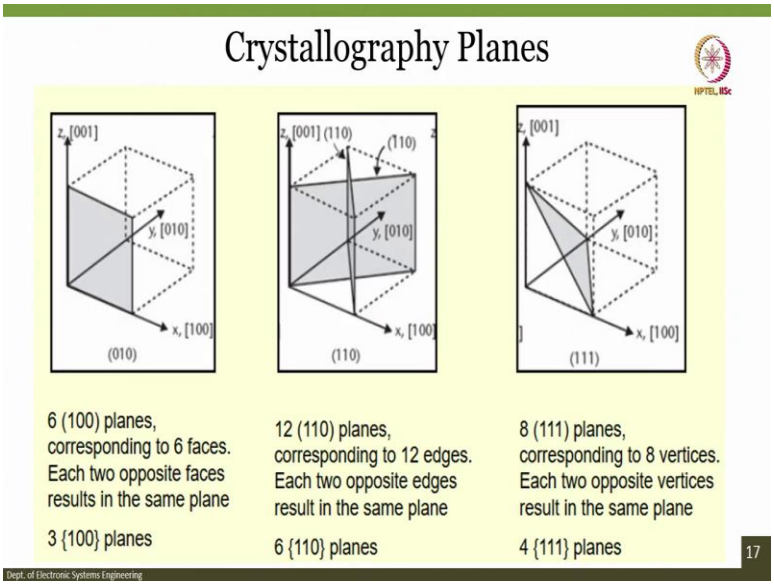

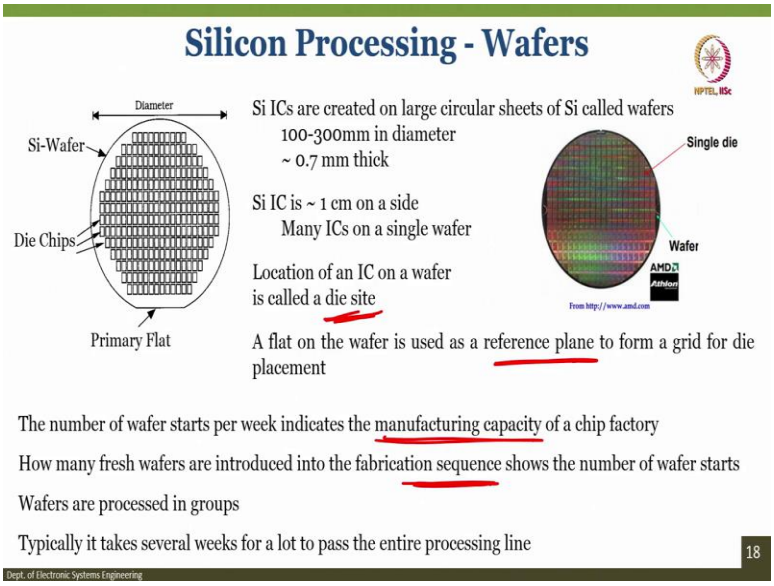

These are crystallographic planes we will take in detail this in the TA class, I do not want to invest too much time on this, but rather that I would like to invest time on understanding what is silicon wafers processing and what is one single chip. So, when you see the final wafer it will come out like this and single die is nothing but a small piece of chip on which all your transistors are fabricated, whether it is CMOS or if it is PMOS, NMOS, even for the FinFET everything is fabricated on silicon wafer.

So, silicon indicator circuits are larger or larger circular sheets of silicon wafers they are fabricated on using silicon wafers as I told you, and the location of an indicator circuit on a wafer is called dye site, which is dye site and a flat on the wafer is used to the reference plane to from the grid from die placement, the number of wafers starts per week indicates a manufacturing capability how many wafers we have started in a week 100 200 400 1000 how many fresh wafers are introduced into fabrication sequence shows the number of the wafers starts. Wafers are processed in groups not individually in the Fab Lab and typically takes several weeks for a lot to process the entire processing line.

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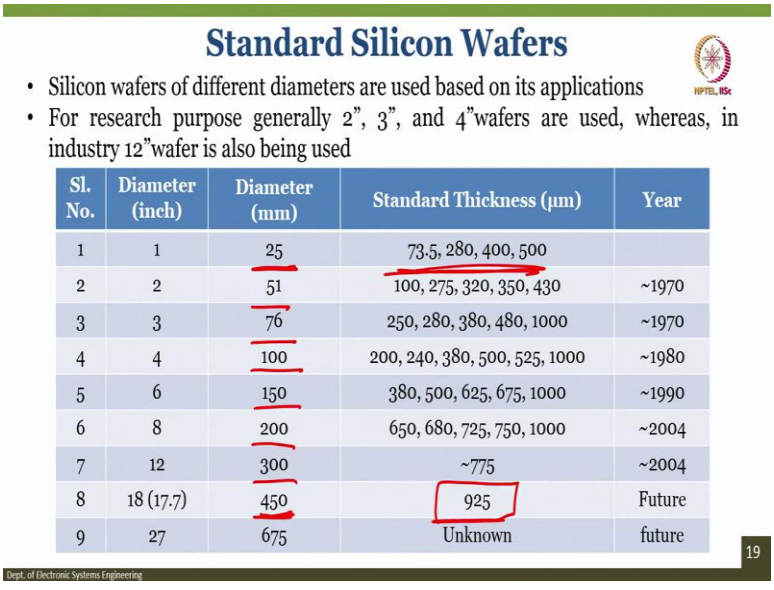

Now, there are several diameter of silicon wafer and now we have reached a way bigger than what is shown here. But, depending on the diameter of the wafer the thickness of the wafer changes, you would need to understand not too much into depth, but to understand that how the diameter and wafer thickness are related.

So, you can see the wafer which is 25 millimeter diameter would have thickness somewhere around this while 51 millimeter, 76, 100 millimeter 150 200 300 millimeter 450 millimeter will have diameter which is increased in size. So, that the 450 millimeter diameter I am sorry this thickness increases correspondingly, not the so, with diameter increase the thickness increases and we have much more bigger wafers now, compared to what is given in the table.

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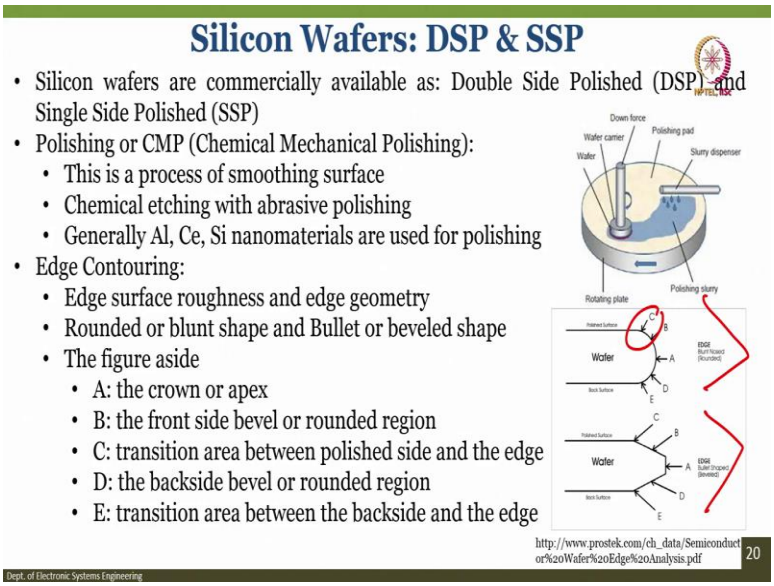

Now, we talk about this DSP and SSP as I told you earlier, either you have single side polished wafer or you have double side polished wafer and the way to polish the wafers is using the polishing mechanism either it is chemical mechanical polishing, or it is just a mechanical polishing. So, this process is used for smoothing of the wafer surface, we know that the smoothing is such that the wafer surface is almost few nanometers in the roughness.

So, it is really smooth and then there is abrasive polishing, chemical etching, there is edge countering. So, edge roughness and edge boundary or geometries understood, rounded or blunt shape or bullet shape our beveled shape, beveled shape I am sorry, beveled shape the different kinds of shapes you can have when you have the boules. It is too different confusing words so it is boules.

So, different shapes you can find out in the ingot on the boules, the figure or side that is ABCD you can see here what does this show ABCDE the A shows the crown or apex, B shows the front

side bevel or rounded region, then you have C with this transition area between polished side and the edge, you can see here the C and then you have D which is a backside, bevel or rounded region. And finally you have E which is transition area between the backside and the edge. So, this is how the things are defined for single side and double side polished.

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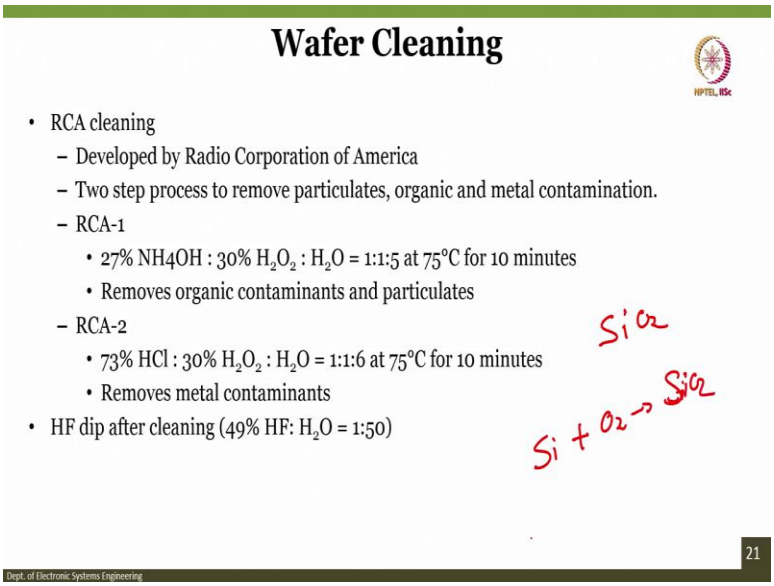

Now, once you have wafer even it is a new wafer, there is a formation of thin silicon dioxide. Why because silicon when reacts with oxygen forms sio2. So, if the oxygen present in the air will also cause a thin layer of silicon dioxide to avoid any kind of oxide when you start the wafer processing, it is important that you clean the wafer that there is something called RCA cleaning RCA-1 and RCA-2 the first RCA-1.

The RCA stands for Radio Corporation of America. And there are two steps to remove the particulates organic and metal contamination. The first step which is RCA-1 involves 27 percentage NH_4OH in the ratio of 30 percentage H_2O_2: H_2O and then is in that particular range we have 1 is to 1 is to is 15 1 is to 1 is to is 5 at 75 degree for 10 minutes you have to dip the wafer and heat it at dip it for 10 minutes and the temperature is about 75 degrees centigrade.

This RCA-1 cleaning will help to remove the organic contaminants and particulates while RCA-2 cleaning which is a mixture of 73 percent HCl is to 30 percent H_2O_2 is to H_2O in the proportion 1 is to 1 is to 6 this again for 10 minutes at 70 degrees centigrade, this will remove any metal

contaminations and then finally, there is an HF dip, HF dip is used to remove the silicon dioxide and thin layer of silicon dioxide it is grown when it is exposed to the air. So, that is a 49 percent HF to H_2O in the in the range of 1 is 50.

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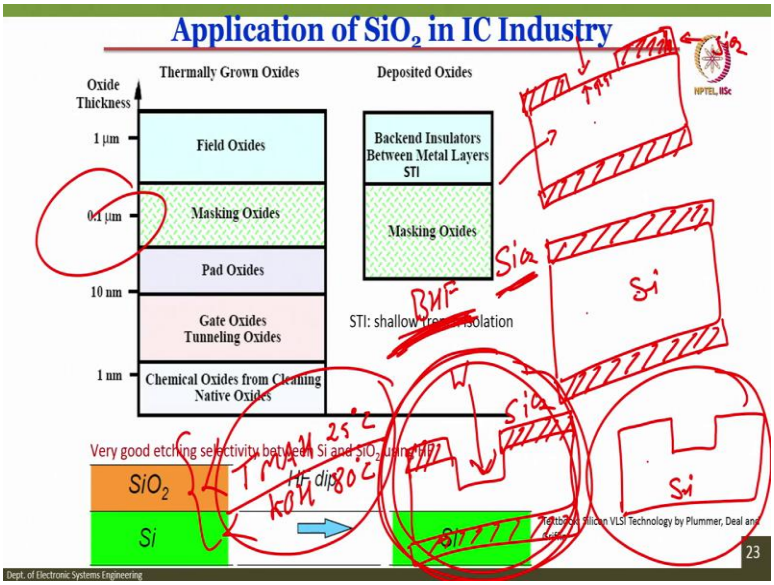

So, let me play this video and then you will understand more about the how the silicon chip from when it starts how the Fab Lab works and how we see the end. Great so, here the next step would be the application of silicon dioxide in IC industries.

So, where exactly the silicon dioxide is used and what is the thickness of silicon dioxide that you require. So, there are two techniques to grow silicon dioxide one is called wet oxidation and second is called dry oxidation. In wet oxygen you use the vapor, water vapor of course, and in dry oxidation you only use the dry oxygen. So, depending on the type of the oxidation the thickness of the oxide on the silicon wafer will change.

Now, if you go for 1 micron to 1 nanometer, 1 nanometer is a native oxide like I said earlier that when you keep the wafer in the air, when it is exposed to where the oxygen there will be a thin layer of oxide that grows on the wafer which is the native oxide, but if you use it for gate it falls somewhere in 10 nanometer we use a masking oxide it can be 0.1 micrometer for field oxides it is 1 micrometer, for masking oxides it is 0.1 micrometer for field oxide it is 1 micrometer, what is field oxide and what is masking oxide.

So, let us understand that these masking oxide the field oxide is. So, this is silicon wafer and let us say that we need to create the pit in silicon wafer like this. So, you end up for etching silicon you can use TMH tetramethylammonium hydroxide or potassium hydroxide this is a 80 degrees centigrade and this is a 25 degrees centigrade either or either or. So, you if you dip the silicon wafer in one of these solution it will start etching but if you dip the silicon wafer then what will happen the thickness will start reducing.

So, what you use is a masking oxide that means, you create, you deposit or you grow the silicon dioxide silicon dioxide on to silicon wafer perform photolithography and when you perform photolithography you just save the silicon dioxide from the backside and in front you protect silicon dioxide in this region and here you can see that this area of the wafer is exposed, this area of the wafer is exposed.

Now, this wafer if I dip it in either TMH or KOH what will happen this will start etching silicon dioxide which is here silicon, silicon dioxide will not get affected sio2 is a masking oxide the rate of etching of silicon dioxide in this solvent which is solvent for etching silicon is extremely slow compared to the silicon.

So, when you dip this wafer into our TMH solution or solution with KOH then this will form the pit as you can see here not like this of course, there is a silicon dioxide here and there is a silicon dioxide here.

Now, once you know the rate of etching you can stop etching you can take out the wafer and rinse it with h2o2 after that, what we wanted we wanted wafer to look like this, silicon wafer. So, you after this silicon is etched you dip this wafer entire wafer into BHF, BHF stands for buffer hydrofluoric acid.

Now, BHF etches silicon dioxide it will not affect silicon. So, if you dip this wafer this one wafer with W entire wafer entire wafer you dip it in BHF then what will happen the oxide will get etched the oxide get etched you have this silicon wafer here.

So, the point that I am making here is that the oxide silicon dioxide which is around 0.1 micrometer can be used as a masking oxide. And for the gate oxide where you use 10 nanometer somewhere around that thickness of the oxide so, the you can see here in this particular image what is called as if I have silicon dioxide on silicon wafer then the if I do HF dip only silicon dioxide gets affected silicon will be protected in a different way we want to show it.

So, very good etching selectivity between Si and SiO_2 to using HF so, HF will not affect the silicon. So, that is the point and then in TMH or KOH the silicon dioxide etching rate is very low compared to silicon and thus silicon dioxide can work as a masking oxide.

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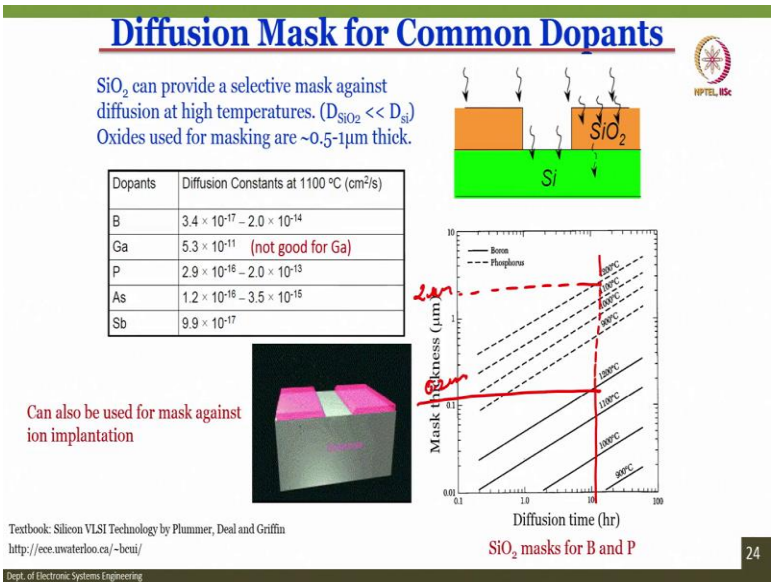

Another work is that silicon dioxide when you dope it dope with different contaminants like boron or phosphorus or gallium or arsenide what will happen is that the dopant cannot pass through silicon dioxide. So, what kind of dopant you want to introduce what kind of contaminants you want to introduce depending on that and depending on the time of the diffusion, the thickness of oxide would change.

For example, if you want to diffuse boron at 1200 degrees centigrade for about let us say 10 hours, then you have to see what is the thickness that you require, it is 10 hours 1200 degrees centigrade and somewhere it is here.

So, you should have somewhere 0.2 microns, 0.2 micrometer thickness silicon dioxide would work, but if I want to do the same thing for phosphorus, at 1200 degree centigrade for 10 hours, so this this becomes the phosphorus so you should have somewhere around 2 microns thick silicon dioxide.

So, that is how the masking oxide SiO_2 mask for boron and phosphorus this is a chart through which we will know what should be the thickness of the silicon dioxide. It can also be used to mask against ion implantation. The ion implantation is another technique to dope the contaminants into the silicon.

So, this is deliberately intentionally added to the silicon wafer. For n type silicon wafer we add p type impurities for p type silicon wafer we add n type impurity sometimes within the well we can have n type impurities. So, depending on what kind of transistors you are fabricating.

Now, like I said there are two types of oxidation technique, one is wet oxidation technique and another one is dry oxidation technique. So, let us see how wet oxidation technique works versus how the dry oxidation technique works.

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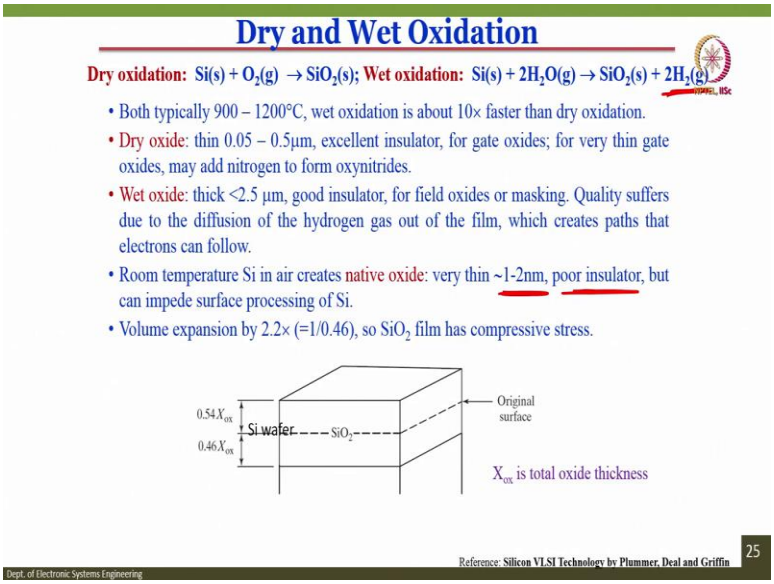

So, in this case you can see dry oxidation and wet oxidation the dry oxidation is silicon is which is solid when it reacts with oxygen which is not gas form it forms silicon dioxide and for the wet oxidation it is SiO_2 plus H_2O gives SiO_2 plus H_2O gives SiO_2 plus H_2 balancing equation $2H_2$ balance equation here $2H_2O$.

So, this is how the equation is balanced the what is the advantage the disadvantage both typically works in the same temperature range 900 to 1200 degree to centigrade but wet oxidation is faster than dry oxidation, wet oxidation quality is poor compared to dry oxidation, dry oxidation generally used for gate oxides a thin layer a very thin layer gate oxides and you can make, you if you want you can add the nitrogen to form oxy nitrites while the wet oxide is generally thicker, faster to grow.

But it suffers due to diffusion of the hydrogen gas you can see here hydrogen gas will come out which causes the parts for the electron that can follow or the because what will happen because of the diffusion that happens the hydrogen when it comes out through the diffusion technique from the silicon dioxide it forms this hollow regions or some paths through which the electron can follow and that is difficulty.

So, that means that wet oxidation cannot be used for gate layer oxides, room temperature silicon in air creates native oxide which is about 1 to 2 nanometer is very poor insulator but can impede surface processing of silicon and that is why when you have a new wafer, you have to do a HF dip form RCA-1 RCA-2 and HF dip. This is how the total oxide thickness is determined and then there are several techniques to grow the silicon dioxide I think this is enough for this particular lecture.

You have understood silicon, you understood silicon dioxide, you understood dry oxidation, wet oxidation and oxide can be used for masking oxide, field oxide as a native oxide, gate oxide and let us understand the techniques to grow these silicon dioxide on to silicon wafer in the next class, which is the thermal oxidation methods. I will go in detail in the next class.

So, till then, if you have any question you can ask through the NPTEL portal, and we will take it from there, we will learn thermal oxidation first and then we will also learn the thermal evaporation, E-beam evaporation by which you can deposit different materials, metal, insulator, semiconductors, sputtering is what of it because we call as a physical vapor deposition techniques, then once you understand that, we will go for photolithography, which is the heart of fabrication technology.

Once you understand how these techniques are used, then we will start attending important problems in the area of neural science and in the area of a brain to address some important problems and the corresponding device for the same. So, I will see in the next class till then take care. Just learn these things. Some of the topics that I say, some of the words that I use, just Google it and see what are the differences. And I will see you in the next class till then. Cheers.