Mathematical Aspects of Biomedical Electronic System Design

Hi, in last class what we have seen? We have seen that what is the cleanroom? Safety protocols while entering the cleanroom. We will also share a video with you of how to access the cleanroom and we have also kind of seen that what not to do in particularly when you use different chemicals and classes of cleanroom according to ISO standards.

We also understand that class 10,000 plus 1000, class 100, class 10. How the clean rooms are identified, is not it? Now, in this class what we need to understand is what is the substrate and how we can grow silicon dioxide if the silicon is our substrate? Again with an understanding of our system, a biomedical system and if I am reiterating then these chips will be integrated into this biomedical system.

And finally, we will understand the mathematical aspects of how this electronic system design would work for that.

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So, silicon, silicon dioxide. Now when you want to have a silicon dioxide this is a process; that you start with metallurgical silicon or you start with sand, the silicon dioxide, you purify it to 99.999 percent pure actually 99.9 times 9 percent pure. Once you go for a technique called CZ technique or Czochralski technique or FZ technique called float zone technique you can fabricate different silicon wafers.

But through CZ and FZ you were only able to get the polycyclic line silicon Ingot, which you can see here. Either CZ technique or FZ technique and once you have that, you get the silicon

ingot. Once you have silicon ingot you have to go for dicing, sawing, polishing and it can be chemical mechanical polishing or it can be an end followed by lapping and followed by chemical etching and then finally you have to you will get the silicon wafer.

Either it can be single side polish wafer or it can be double side polish wafer. What do I mean by single side polish wafer and what do I mean by double sided polish wafer? If you can see the wafer that I am holding in my hand, now you will understand the difference.

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Can you see the wafer that I am holding in my hand? Yeah, so as you can very clearly see this is a polished side so you can see the reflection. If I just do this you can see the reflection is not

it? But if I if you see the backside of the silicon wafer this rough is not it see it is rough front side polished, backside rough, front side polished, backside rough.

This is single side polished wafer. If I had double said polished wafer means front and back both will be polished. So, this is what I mean by single side polished wafer.

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If I go to the next slide silicon as we all know, silicon, silicon boules and wafers you had to if you see this picture, you will understand that the silicon boules are made in a class 10 class 100 kind of cleanroom environment, it is called silicon foundries and then the wafers are cut from the boule which is right over here.

And the reason of fabricating this particular boule inside that cleanroom is to make sure that there is no contamination. So, a silicon ingot or boule is what we say.

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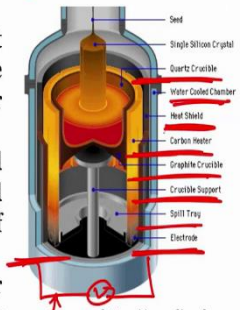
CZ Technique

- CZ technique or Czochralski technique is the most important method for production of bulk single crystals
- At the beginning of the process, the feed material is put into a cylindrically shaped quartz or graphite crucible with a fused silica lining and melted by resistance or radio-frequency heaters.
- After the feed material is completely molten a seed crystal with a diameter of typically a few mm is dipped from top into the free melt surface and a small portion of the dipped seed is melted.
- Then, the seed is slowly withdrawn from the melt (under rotation) and the melt crystallizes at the interface by forming a new crystal portion.
- During the growth, the diameter is controlled by carefully adjusting the heating power, the pulling rate and the rotation rate of the crystal.



Source: https://meroli.web.cern.ch/Lecture_silicon floatzone_czochralski.html

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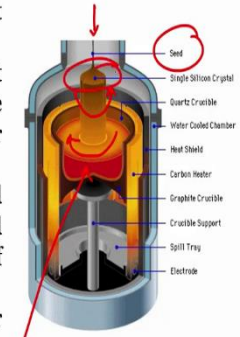

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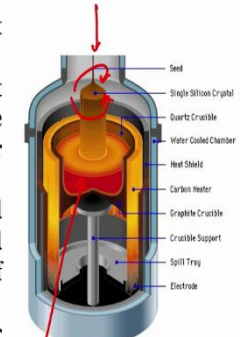

Source: https://meroli.web.cern.ch/Lecture_silicon floatzone_czochralski.html

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CZ technique as you can see here, it is also called Czochralski technique, depending on the pronunciation you will understand through different videos CZ Czochralski is pronounced in a different way. However, the important thing is it is a most important method of our production of bulk crystal silicons. Also it is cheaper than FZ technique.

At the beginning of this process the film material is put into the cylindrical shaped quads you can see this particular schematic, here, and what do you see that the and the external material all the way the extra material is made up of what? So, the final the blue colour thing that is a water-cooled chamber. Then you further go in you will see that there is a heat shield and if you further go in then you will see there is a carbon heater.

So then in further there is a graphite crucible and then there is a quartz crucible, graphite crucible, quartz crucible. Then the bottom is crucible support, then there is a spill tray and then there is a electrode. Electrode for the heater. Electrode is here and we apply voltage between these two electrodes and you can heat the heater.

Heater is very very simple you all know it is a thing with the resistance, resistance is given by $\rho \frac{L}{A}$ depending on the length and area you can change the resistance of the heater. Resistivity for a given metal remains constant. So, what we do here is that you start with the seed. So, now, let me just rub it down.

So, the and you can see here there is a seed crystal, seed crystal at the top in this way and when you and this is a molten molten silicon molten silicon molten which is melt molten molten silicon. So, when I did this rod or seed crystal inside is molten silicon and rotate it. So, you can say give one direction rotation or and this crucible which is holding the molten crystal will rotate in the opposite direction.

Seed will seal will rotate in one crucible will rotate in opposite direction. So, if we see this rotating clockwise direction the anti-clockwise direction crucible will rotate in a clockwise direction or vice versa. Now, depending on the orientation of the seed crystal and depending on the pulling rate and the rotation rate, the thickness of this boule would be different.

So, that is something that we need to understand. So, this is what this Czochralski technique is all about. If you read further it says that at the beginning of process the seed a material is put into this in integral shape quads which is right over here is the once you place the material then

you have to heat the material. This crucible is graphite crucible with a fused silica lining and is melted by resistance or additive frequency heaters.

After you find the material is completely molten a seed crystal is introduced seed crystal from here is introduced and from the top into the free melt surface and a small portion of the seed metal is seed crystal is the dipped into the melted zone or molten silicon then the seed is slowly withdrawn, slowly withdrawn from the melt under rotation, I told you.

Either you had to rotate in this direction are you can rotate in the opposite direction clockwise or anti clockwise and during the growth the diameter is controlled by carefully adjusting the heating power, pulling rate and rotation of the crystal rotation of the crystal. Three things is very important or three things are very important one is the heating power, second is pulling rate and third is a rotation of crucible.

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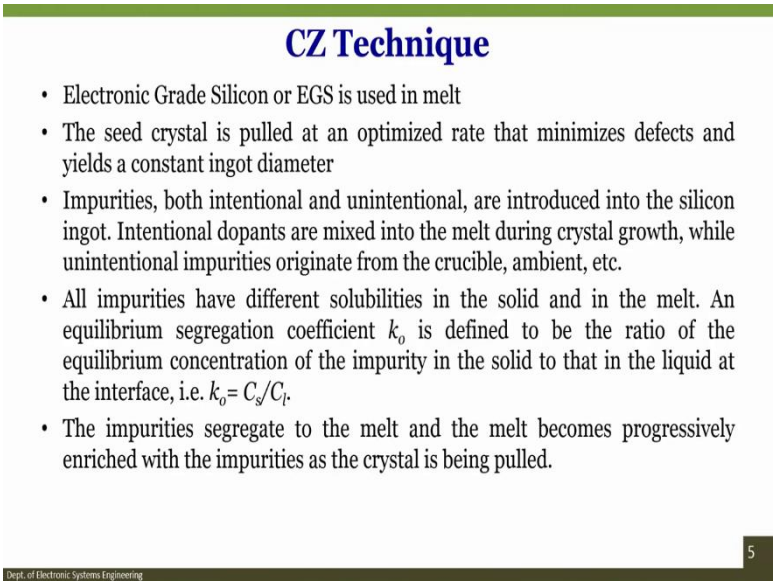

So, through the setting what we get? We get electron grade silicon and why we are understanding this technique, because finally we will use silicon wafer to fabricate different devices. So, the seed crystal is pulled at an optimized rate that minimize these defects because faster you pull more defects you have. If it is very slow again you have problems.

So, you had to optimize the rate at which the seed crystal is pulled off pulled out of the molten zone and you can get a constant ingot diameter if your rate is optimized, pulling rate is optimized. Impurities both intentional and unintentional, if it is not impure you all know silicon

becomes amorphous yeah sorry silicon is an intrinsic silicon. If you know N type or P type it becomes extrinsic silicon.

So, intentionally you can dope or unintentional there is doping which are introduced dopants or impurities are introduced into silicon ingot. Intentional dopants are mixed into melted during the crystal growth while the unintentional impurity or unit from several things including ambient environment, crucible etcetera.

Now, this all have all impurities have different solubilities and an equilibrium segregation constant k_o if you want to define an equal equilibrium segregation coefficient k_o, it is given by $k_0 = \frac{C_s}{C_l}$ while you can say that C_s is the equilibrium concentration of the impurity in solid while C_l is the equilibrium concentration of impurity in liquid at the interface.

So, $k_0 = \frac{C_s}{C_l}$ and k_o is known as equilibrium segregation coefficient. So, important thing remember $k_0 = \frac{C_s}{C_l}$. The impurity segregate into the melt and melt becomes progressively enriched with impurities the crystal is being pulled.

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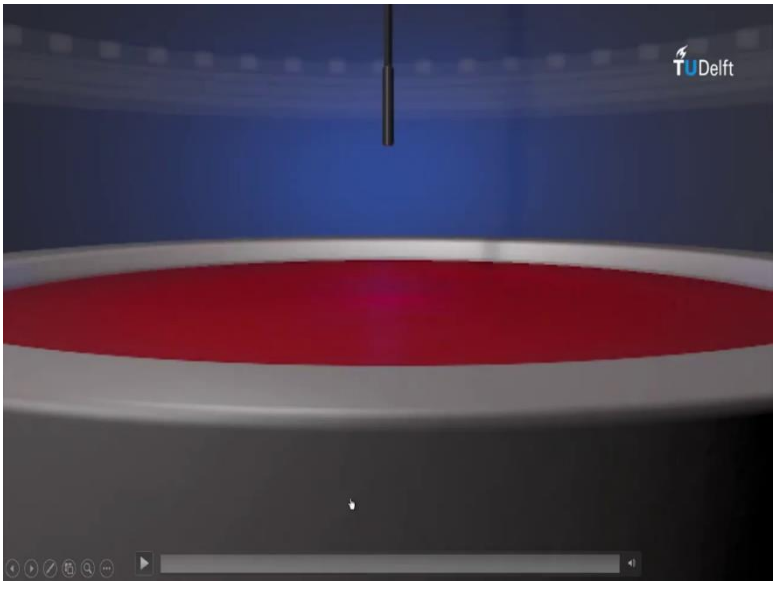

This is the video. Let me play the video this is show is from TUDelft is very informative video for academics. So, we will see here how the crystal is grown.

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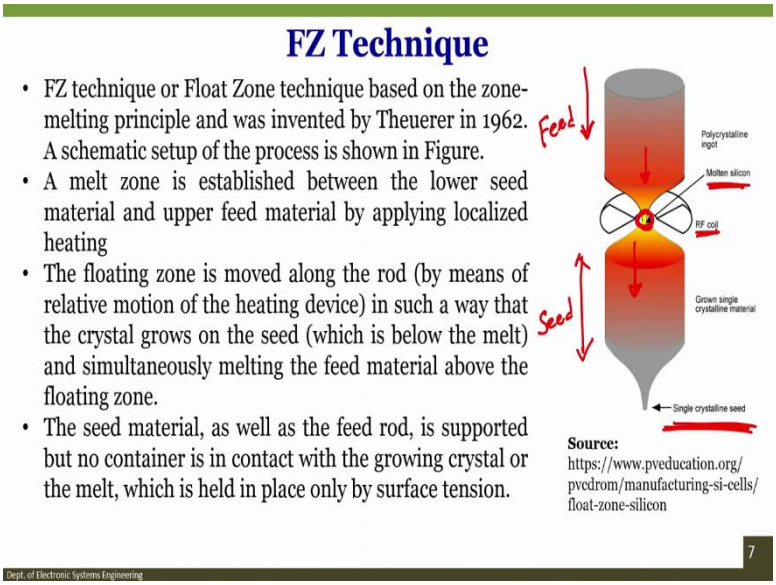

So, now you have seen how the technique works it now it becomes very easy for you to understand that how this easy technique is used for growing the ingot and finally, from that ingot we fabricate several wafers. Now, let us go to the another technique which is called float zone. The name itself suggests that there is a floating zone. So, float zone is based on the zone melting principle and was invented by Theuerer in 1962 schematic.

The setup is shown right over here. Here you can see that there are two things one is the top one is a polycyclic polycrystalline ingot and the bottom one is a grown single crystal material that grows here in the bottom and you have a single crystalline seed at the bottom. Whatever the molten zone is created is from the seed crystal to the growth crystal.

So, it is right over here. Here it is heated using RF coil and is a molten silicon. So, if you read it, it shows the same thing that as the melt zone is established between lower seed material and upper feed material the upper one is called feed material the lower one is called seed material, alright. By applying localized heating, where is localized heating?

Right in the interface, the floating zone is moved along the road in such a way that the crystal grows on the seed. So, when the seed crystal is moved and the floating zone is moved such a way that this seed crystal that you can see here it starts growing in this direction and simultaneously melting the feed about the floating zone.

So, when it starts growing in this direction as we have seen this feed crystal starts melting further because you get the seed crystal from the feed crystal. The second material as well as

the feed rod is supported but no container is in contact with the growing crystals or the melt which is held in place only by surface tension. This whole thing is held only by surface tension.

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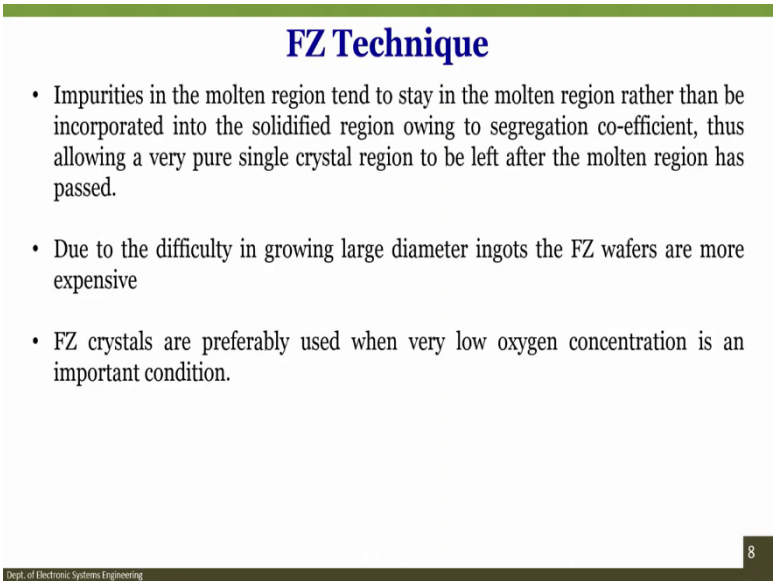

And the good thing is that because of this, impurities in the molten zone tend to stay in the molten zone rather than be incorporated into solidified region; that means that you the quality of the wafer that you get using FZ technique is way better compared to the CZ technique. In fact, a very pure single crystal region to be left after molten region has passed due to the difficulty in growing large diameter.

See the difficulty of the technical limitation of detecting is that you cannot grow a larger diameter of silicon wafer and that is why FZ becomes more expensive. But however, FZ crystals are preferably used preferably used when there is a low oxygen concentration requirement.

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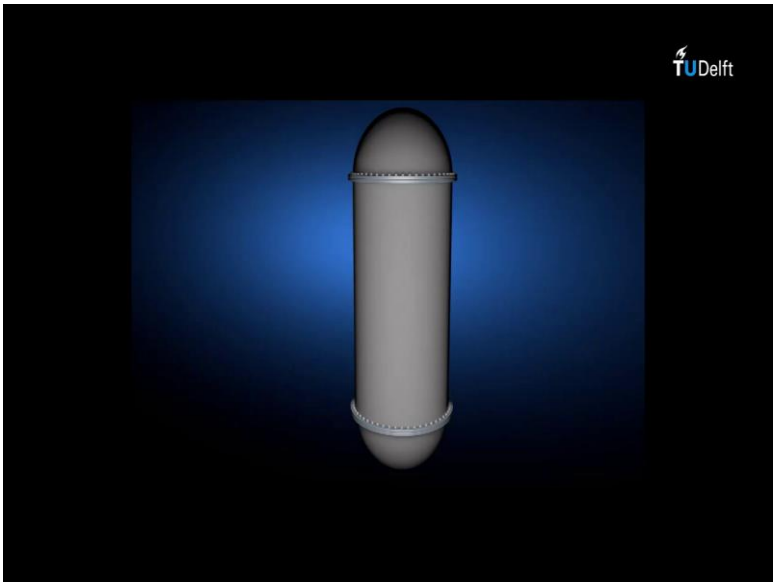

Let us see again an important informative video from on the FZ technique. Let me play it. So, you have seen. Now what do you have seen you have seen a CZ technique you have seen FZ technique. Let us see that in a schematic, if you start with crucible, we start putting the polysilicon and we melt it and what is the process to all the way to bring the wafer that means right from the start to the end what are the process involved? Let us see this one by one.

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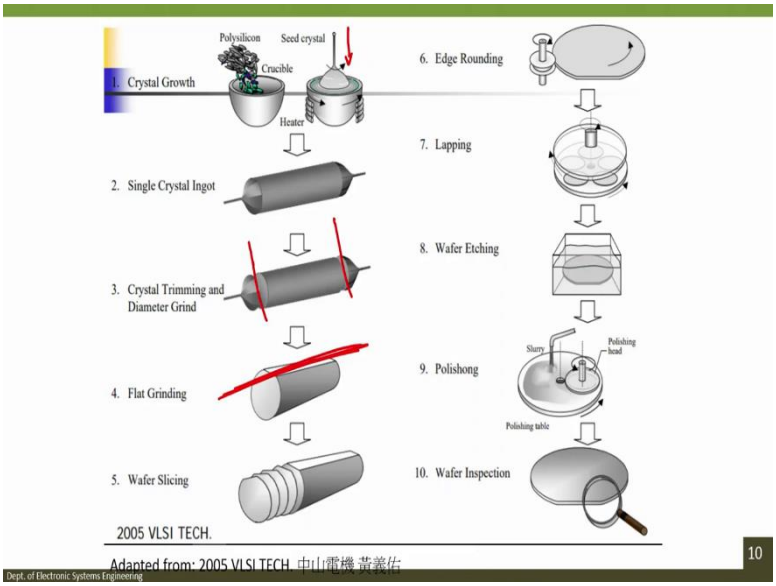

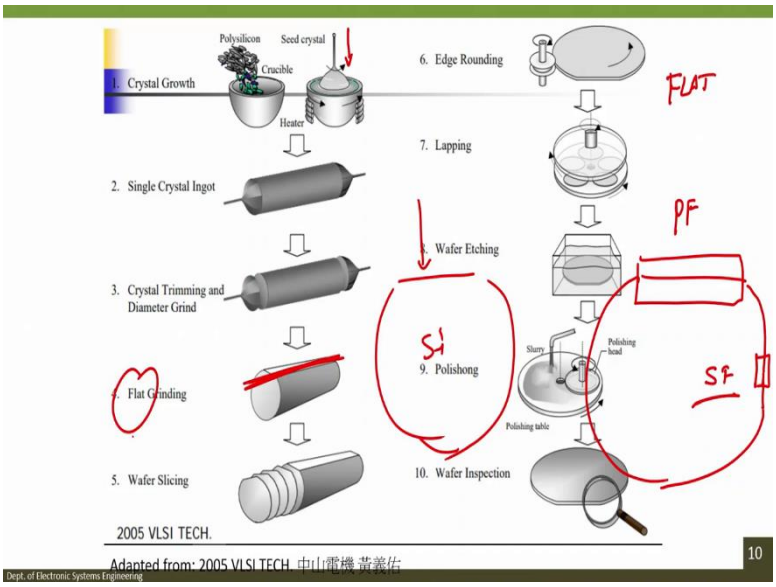

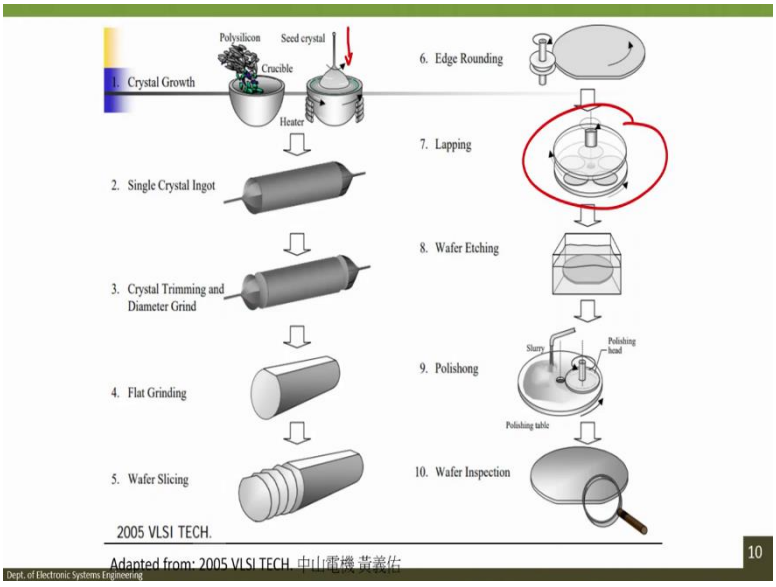

If you see the schematic what do you see is that polysilicon is added to the crucible and as and then it is heated either using RF RF or using the resistivity then you can introduce the seed crystal here the seed crystal is introduced into the molten zone. When you do that and you pull it at as a constant rate or at a different time than what you get is a single crystal ingot once you have this do you have to trim the sides, this side and this side, you are trimming it.

Then you have to create a flat zone, flat zone or flat grinding. There is a reason of flat grinding every wafer that you see would have this flat grinding and a flat grinding the on the wafer will always be seen visibly like a circle these are flat grinding. For silicon wafer there is a flat grinding. When you take any silicon wafer you will see a flat grinding on one side and sometimes you have a small flat on the underside.

The bigger flat is called primary flat, the smaller flat is called secondary flat, f l a t, flat. Because it is a flat you when you flat grinding gives us a flat. So, this flat grinding helps us to get the primary flat in all the silicon wafers, primary flat in all silicon wafers depending on the primary flat the angle of secondary flat with respect to primary flat we can say it is 100 or 111 or 110.

We can also understand whether it is P type or N type thus the flat grinding is very important step. After you do that you can slice the wafer you can slice the wafer I will just show you in the next slide using diamond wires and then there is the edge rounding followed by lapping. This is a lapping process. And then there is a wafer edge followed by polishing. After you polish either both the sides you can double set polish wafer if you polish same side.

Now, only one side then you have a single side polish wafer followed by for inspection. So, these are the steps if you just repeat then this crystal growth is given as what you are melting polysilicon in crucible. Next is create a ingot. Next is trim the sides of the ingot, then you do a flat grinding followed by wafer slicing, followed by edge rounding, lapping, etching, polishing and wafer inspection.

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Now once you do that you see here, there are two schematics you can see here. One on the left side, it shows the diamond coated wire. And there are two reels, whether is a take-up reel, there is a wire guides, and there is a wire moving in a direction these are silicon ingot. So, with diamond wires, you see here, the diamond wires you can slice the ingot into many wafers, is not it? And then once you have this sliced wafers you do the lapping and polishing.

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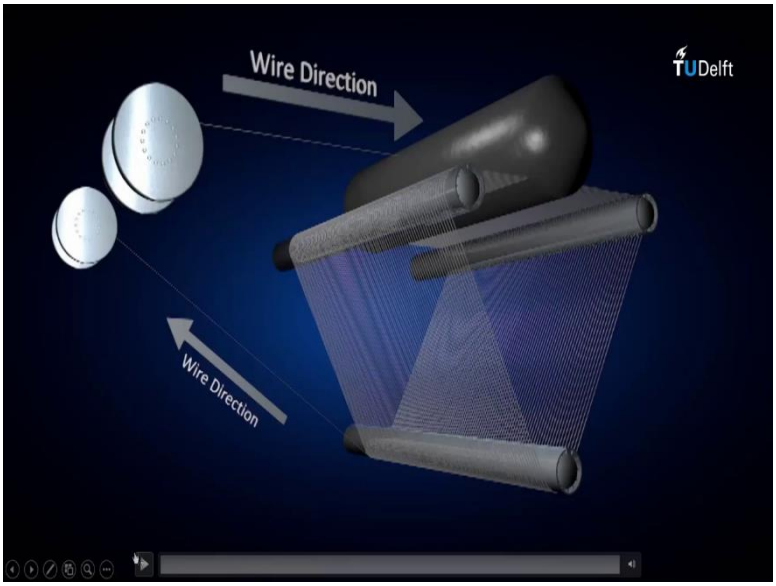

So this is a again a video, you just see how it works. And what is the reason of using a thin wire. Because in the in this, right now, with the core technology that we have even a few microns has a lot of thousands of transistors. So, if we waste a lot of silicon during the fabrication, that is in fact a loss in that total amount of material that our company has to bear.

And that is a very high loss. And that is why to remove this loss or to reduce the amount of silicon that you have to throw it during this fabrication; you use this process of slicing this silicon wafer using diamond wire. So, I will just play the video, and then you can see the next slide. So, now you have seen this slide.

And now what do you see is that after this, the important thing is why we study all this thing like silicon fabrication, silicon dicing, slicing, lapping, polishing, all this thing is because 95 percent of the transistors, devices are still made using silicon wafer. And that is very important to understand how silicon is fabricated.

In the present course, professor Chandramani we will talk about the mathematical modelling, where he will talk about the biomedical system and there you will see that this biological system has a integrated chip which is made out of silicon and that is why the reason of learning silicon at this point of time.

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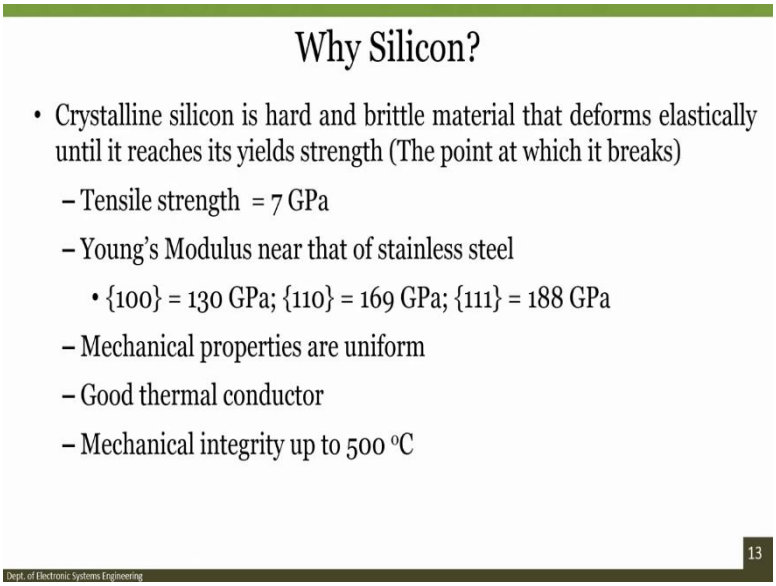

So, crystalline silicon is the hard and brittle material that deforms elastically until it reaches its yield strength and tensile strength is about 7 giga pascal, young's modulus you can see is near that of stainless steel, mechanical properties are uniform, good thermal conductor and mechanical integrity up to 500 degree centigrade. So, these are some of the important things of silicon material.

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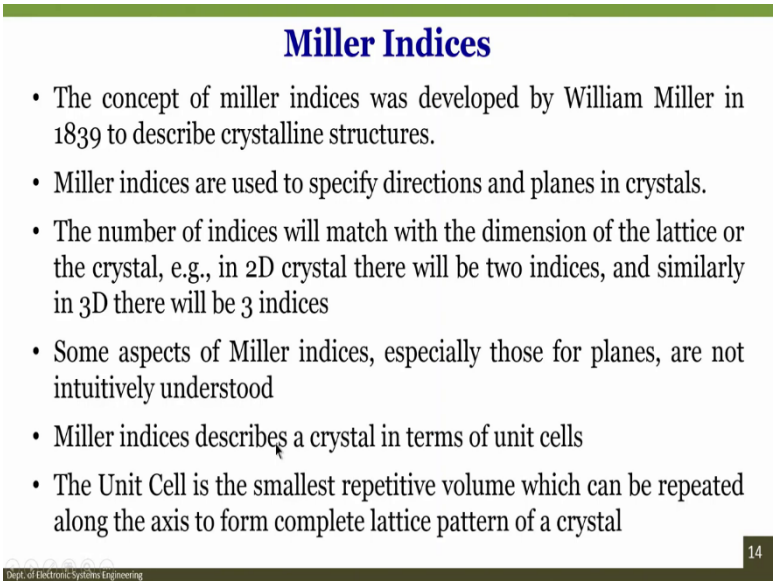

Now, very important understanding is miller indices, which was developed by William Miller in 1839 and are used to specify direction in plane in the crystal. So, as you can see, just read out this particular slide.

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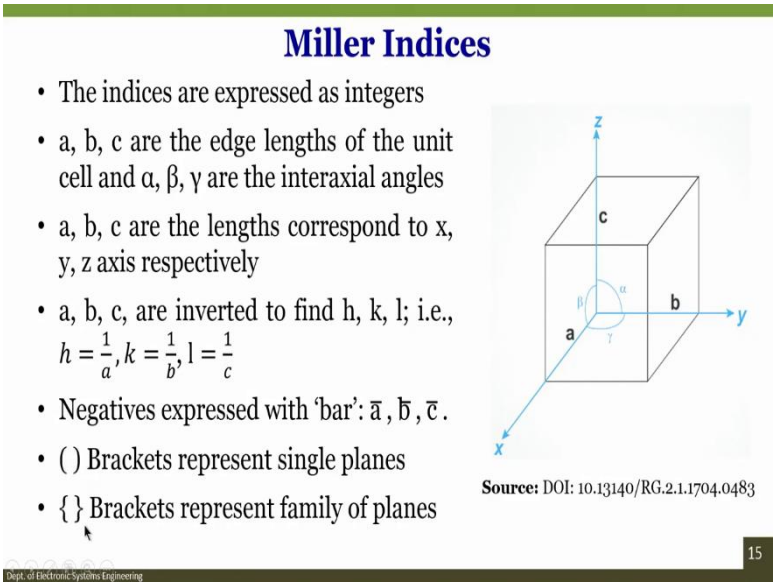

Let me go to a very important slide which is in one or two lines anyway, one or two slides you will see here a, b, c, are the edge lengths. α, β, γ, the inter axial angles you can see α, β, γ; a, b, c, are edge lengths and then you have a, b, c, are inverted to find h, k, l plane I will just show it to you.

And negative expressed with bar are, $\bar{a}, \bar{b}, \bar{c}$. This kind of bracket represents a single planes while the { } brackets are representing the family of planes.

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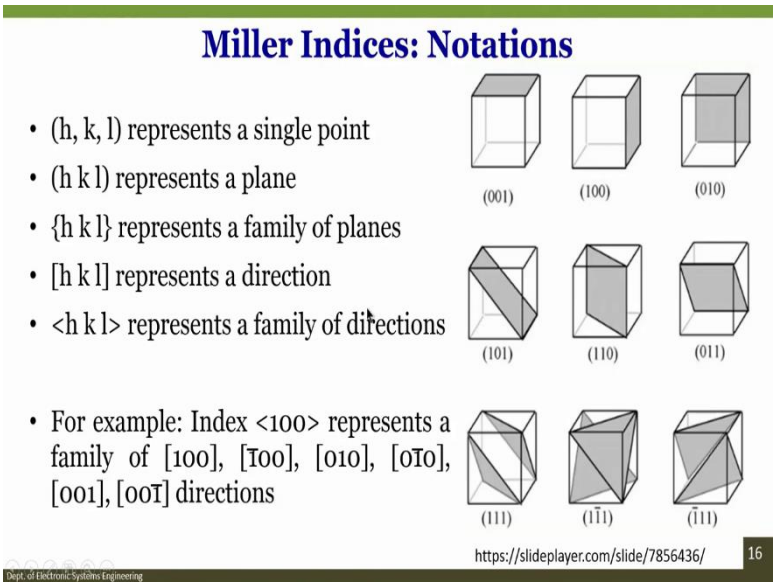

So, here you can see h, k, l plane or h, k, l represent the plane. Here h, k, l represent a single point if you have called it a family of planes if you have [] bracket then that represents this

direction while in this case, if you have h, k, l between two arrows it represent a family of directions. So, it such like plane, family of planes, direction, family of direction.

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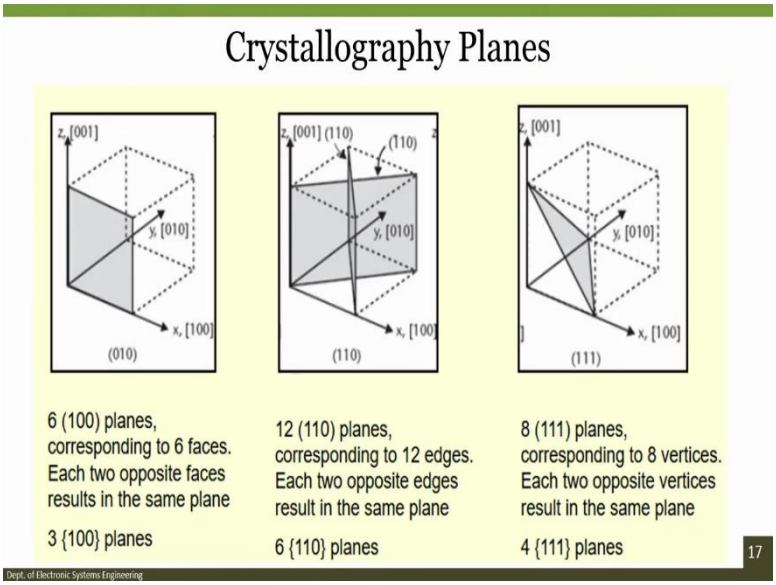

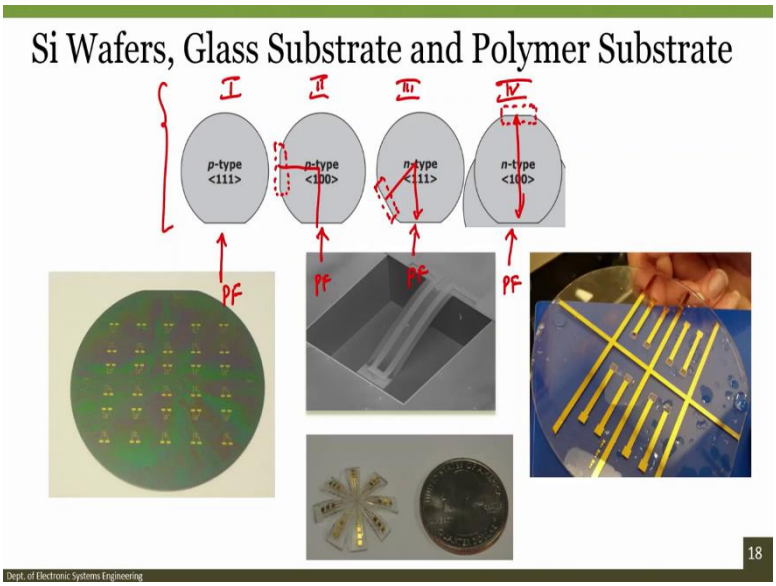

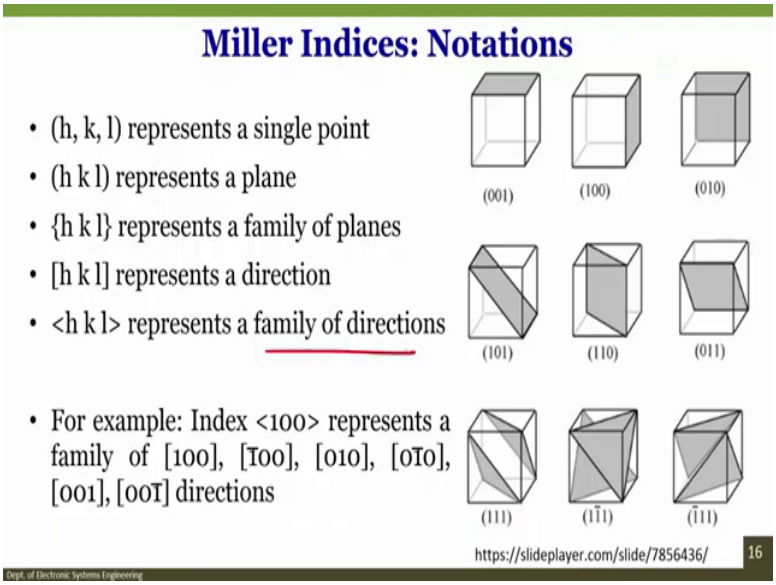

But even important point is the crystallographic planes. And here from the planes itself you can understand the crystal orientation and the whether this P type or N type the miller indices are very important to understand all these things. Like for example 111, 100, 111, 100. Why it is 111? How it is 100? How the crystals are oriented and what are the planes? This miller indices helps to understand these all points.

However for this course you do not have to worry about it. Let us focus more on what is important which is identifying the wafer based on the flat that is present on this silicon wafer. Now here you can see that there are flats one primary flat in every silicon wafer. You can see let us name it as 1, 2, 3 and 4 and here you can see there is a primary flat.

We will say primary flat as a PF. Here also there is a primary flat. In this case also you find primary flat and finally in the fourth one also you find primary flat, is not it? Now you see that where is the secondary flat? Is in this case you can you see secondary flat? You cannot see. In this case, yes, I can see a secondary flat right over here, is not it?

And this one, yes, secondary flat is here. In this one, yes, it is right over here. Correct. Now, this is 90 degree with respect to primary flat. This is 35 degree, 45 degree with respect to primary flat. This is 180 degree with respect to primary flat, is not it? So, depending on where is the angle of the secondary flat with respect to primary flat you can say it is a P type material or is a N type silicon wafer and whether the orientation is 100 or 111.

We have seen what is the meaning of this particular thing is a family of directions it is a family of directions.

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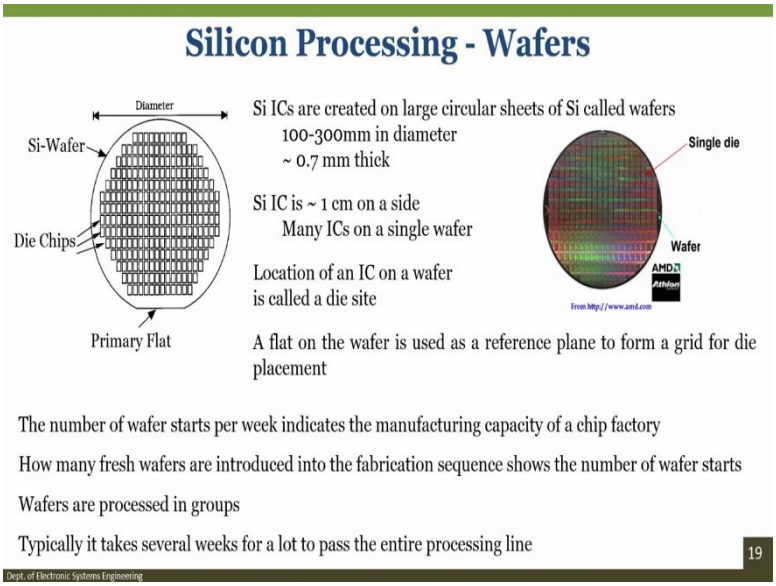

So, single processing wafers you can see here once it is finally processed this is called single dye and each single dye has billions of transistors which are used for several applications. And in a foundry it takes several weeks to pass a lot and the location of an IC on a wafer is called an die site. A flat on the wafer is used to the reference plane to form a grade for dye placement. And the number of wafers starts per week indicates the manufacturing capability of the chip factory.

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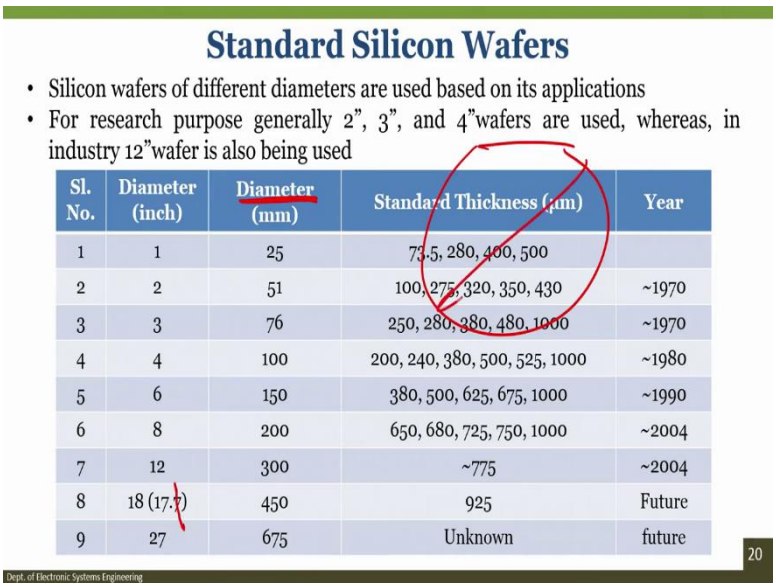

Standard Silicon Wafers

- Silicon wafers of different diameters are used based on its applications
- For research purpose generally 2", 3", and 4"wafers are used, whereas, in industry 12"wafer is also being used

Sl. No.	Diameter (inch)	Diameter (mm)	Standard Thickness (μm)	Year
1	1	25	73.5, 280, 400, 500	
2	2	51	100, 275, 320, 350, 430	~1970
3	3	76	250, 280, 380, 480, 1000	~1970
4	4	100	200, 240, 380, 500, 525, 1000	~1980
5	6	150	380, 500, 625, 675, 1000	~1990
6	8	200	650, 680, 725, 750, 1000	~2004
7	12	300	~775	~2004
8	18 (17.7)	450	925	Future
9	27	675	Unknown	future

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Depending on the size of the wafers again the wafer is generally only diameter you see a diameter. So, when I say 1, 2, 3, 4, 6, 8, 12, 18. I will say that is a diameter of the wafer that is there. That is 4-inch wafer, or it is a 6-inch wafer or 12-inch wafer or 18-inch wafer it depends on the diameter of the wafer.

With respect to the diameter of the wafer the thickness of the wafer also changes. So, for let us say 4-inch wafer which is 100 millimetre in diameter, the thickness generally we can obtain is right from 200 to 2000 microns. Generally, we use 500 micron thick 4-inch wafer in this department.

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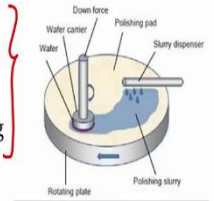
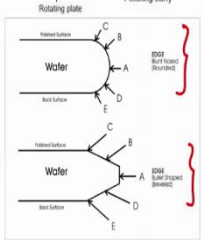
Silicon Wafers: DSP & SSP

- Silicon wafers are commercially available as: Double Side Polished (DSP) and Single Side Polished (SSP)
- Polishing or CMP (Chemical Mechanical Polishing):
  - This is a process of smoothing surface
  - Chemical etching with abrasive polishing
  - Generally Al, Ce, Si nanomaterials are used for polishing
- Edge Contouring:
  - Edge surface roughness and edge geometry
  - Rounded or blunt shape and Bullet or beveled shape
  - The figure aside
    - A: the crown or apex
    - B: the front side bevel or rounded region
    - C: transition area between polished side and the edge
    - D: the backside bevel or rounded region
    - E: transition area between the backside and the edge





http://www.prostek.com/ch_data/Semiconductor%20Wafer%20Edge%20Analysis.pdf

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Again, same process is just in a different format. What do you see? It is a it is a CMP or double side polished or single side polish. CMP stands for chemical mechanical polishing and what you get is a smooth surface either single side polish or double side polish. Single side polish for a cheaper compared to the double-sided polished wafers.

Then there is the edge contouring and therefore edge contouring the edge roughness and surface roughness, edge geometry is very important. Rounded or blunt shape and bullet or bevelled shaped as you can see here. What you see is edge blunt, rounded and here is a edge bullet shaped. So, this is the different way of edge contouring.

Again we will not you do not have to bother about the why it is a blunt needed, rounded or you require a blunt, bullet shaped or bevelled shaped edge. But what you need to understand is that in chemical mechanical polishing is used for smoothing of surface or smoothening of surface. Chemical etching with abrasive polishing and generally aluminium, Ce or silicon nano materials are used for polishing the wafer.

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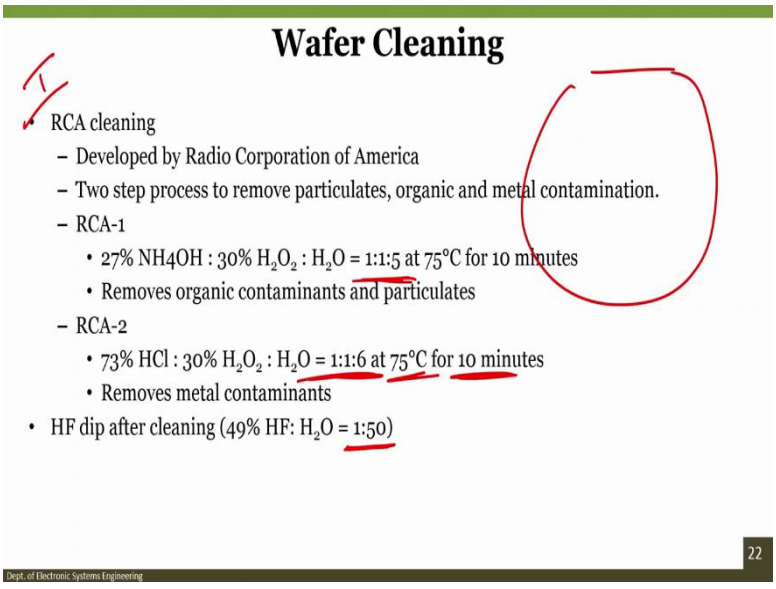

Now, when you get a silicon wafer when you want to start the process, the first step is the RCA cleaning. RCA stands for Radio Corporation of America there is RCA-1 and RCA-2. This is a two-step process to remove the particulates, organic and metal contamination and also to remove the organic contamination and particulates.

So, the RCA-1 you had to take a 27 percent of NH_4OH in the ratio of 30 percent H_20_2 in the ratio of H_20 there is 21 percent 27 percent NH_4OH which is 30 percent H_20_2 is to H_20, which

is 1 is to 1 is to 5 at 75 degrees centigrade for 10 minutes. You have to dip the wafer in this kind of chemical and finally, this will help in removing the organic contaminants and particulates.

You take it out or rinse it with DI water and you can dip it the other solution which is 70 percent HCl is to 30 percent H_20_2 is to H_20 in 1 is to 1 is to 16, 1 is to 1 is to 6 ratio I am sorry in earlier one also I may have wrongly mentioned as 1 is to 1 is to find a 15; it is 1 is to 1 is to 5. In this case is 1 is to 1 is to 6 and the temperature is 75 degrees centigrade for 10 minutes.

So, RCA-1 and RCA-2 are two steps finally you have HF dip cleaning which is 49 percent HF is to H_2O is equal to 1 is to 50. This is 1 is to 50. So, the when you perform this then the wafer becomes cleaner. Now does not mean wafer is not clean, it is already cleaned, but you had to clean to make sure that there are no organic contaminants and there are no metal contaminants on the wafer otherwise that will affect the overall characteristics of your device.

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This is another video let me play it again very informative video to see that how the silicon wafer is fabricated, how the process flows are there and you will see that in most of the things that there is very less involvement of the engineers. It is more like an automated system to minimize the contamination during the fabrication.

So, I will just play the video. So, you have seen now how the silicon is fabricated in a foundry. Let us quickly see the effect of silicon dioxide.

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When you have silicon dioxide the wafer will look different than what is a silicon wafer. So, if I hold the wafer which is in right now in my hand you will very clearly see that if it is a silicon dioxide or silicon you can see this wafer it is it is silicon and you can see this wafer silicon dioxide you can see the change in colour.

Compared to this one that there is a change in colour in this one, is not it? See there is a change in colour. So, this one is there is a silicon on which we have patterned material. This is silicon dioxide on which we have added the material. The material is metal there are 2 different patterns, but then you do not have to worry.

The point that I am making here is that the silicon wafer that you I am holding here, if you directly deposit a metal in some cases it will not work because it will get short circuit and or the effect of metal directly and semiconductor you know. If you studied physics you understand work function and other things.

However, if you use oxide then it is an insulator material and thus the silicon is only used as a base material. The entire thing that we grow on the silicon will be our device including the substrate of course, but that is an insulator material. This insulator is generally a silicon dioxide. Now silicon dioxide in this case is just an insulating material.

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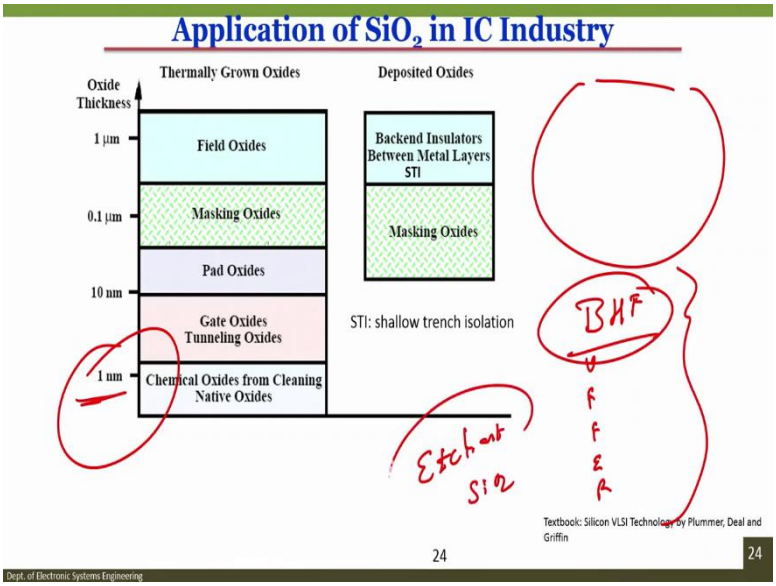

But when you create a MOSFET or you create any other device and as you can see in the schematic you will see that it can be used as a field oxide, it can be used as a masking oxide, it can be used as a pad oxide, gate oxides, chemical oxide for native oxides which about one nanometre. It can be used back-end insulators; it can be used as a masking oxide.

So, let me again tell you what exactly all these things are. One nanometre is when you keep the silicon wafer in room the in a in a environment which is a lab environment because of the presence of oxygen there is there is a native oxide that is created which is close to one nanometre and a way to remove this negative oxidize by dipping this wafer into BHF.

BHF stands for buffer hydrofluoric acid, buffer, B-U-F-F-F-R, hydrofluoric acid that we know. So, if you dip this silicon wafer which is a thin layer of oxide into BHF then the oxide will get etched because BHF is a etchant for silicon dioxide, is a etchant of silicon dioxide. So, there is your one nanometre oxide.

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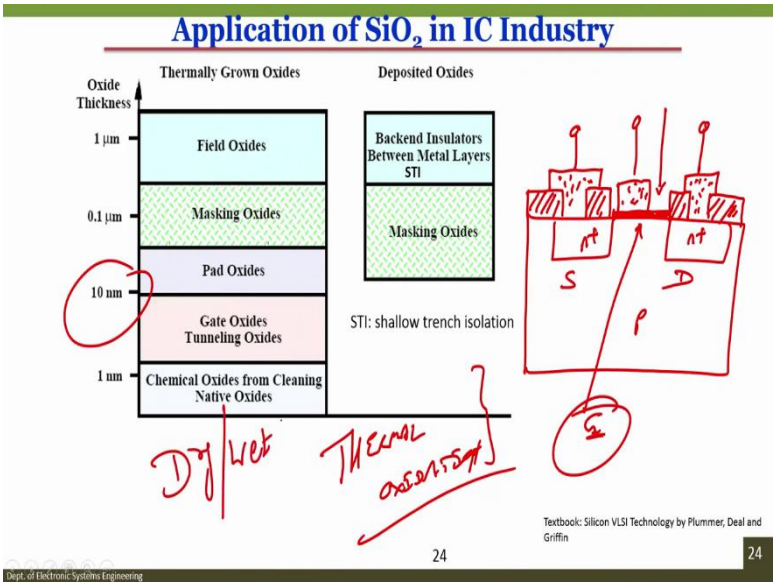

Then you talk about gate oxide. Gate oxide those who are from electronics background they would know that in case of MOSFET generally what we learn is there is a source, there is a drain and there is a gate and then in a gate there is very thin layer of oxide that you have, is not it? And then in this one you have a thicker oxide layer, this is your silicon dioxide, silicon dioxide, silicon dioxide, silicon dioxide and this one is also silicon dioxide.

On this you have your metal contact bed n+, n+, p. This is your gate, this is your source, this is your drain, this is contact, contact, contact; I am just showing a very basic view of the MOSFET. So, it is a n-MOS because the channel is through the n+ region and then here there is a thin layer of gate oxide. This gate oxide thin layer is about 10 nanometre, and we are just understanding depending on one of the technology.

There are different technologies to fabricate MOSFETs. This thin layer of gate oxide is grown using a technique called thermal oxidation. Thermal oxidation and thermal oxidation we can have dry thermal oxidation or we can have a wet thermal oxidation dry oxidation or wet oxidation. Now, let us go to the next step.

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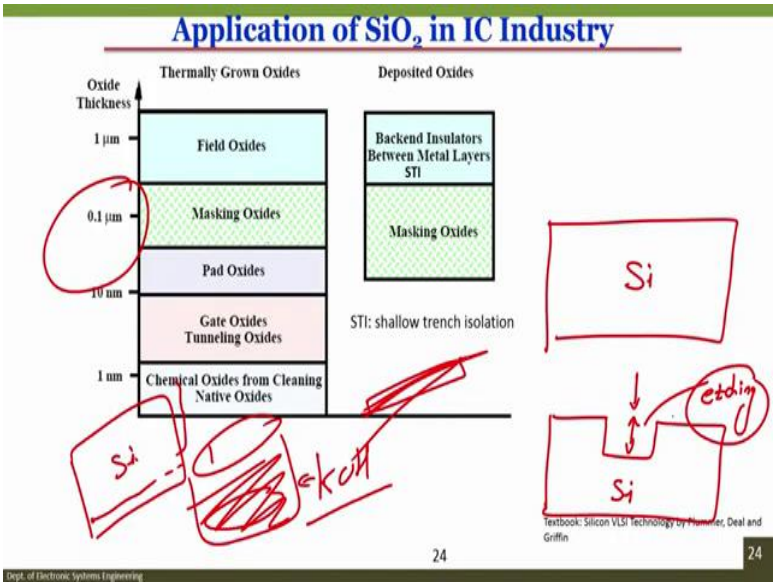

Next step is your 0.1-micron masking oxide. What does masking oxide mean? Let me let me give you an example. You have a silicon wafer, what I want to etch silicon wafer like this etch, etching E-T-C-H-I-N-G. I want to remove that silicon wafer. This one this one silicon from my silicon wafer. This removing of silicon material from the silicon wafer is called etching of silicon.

To do that I like if I dipped though I know that what is the chemicals that are, what are the chemicals that can etch silicon. Suppose I know that potassium hydroxide, KOH. It can if I dip the wafer silicon wafer into KOH it will dissolve. If I dip this wafer, let us say in a beaker like this, which is full of KOH material what will happen is?

This is a cross section of silica. Well see that the silicon starts dissolving this remaining area will dissolve only this material is left. If I dip this for a long, long, long time, this also goes away. So, everything is dissolved. So, I do not want that. I want only to the silicon to get etch only from this region. For remaining region silica silicon should not get etched.

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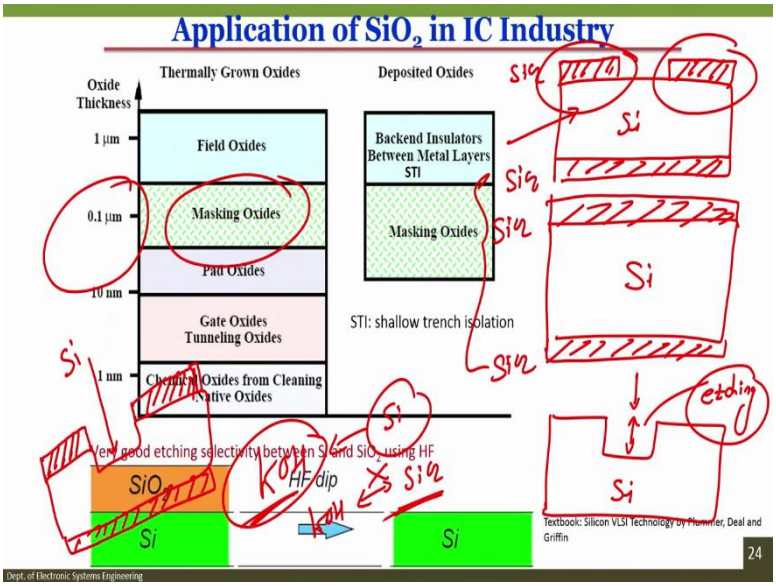

So, what should I do? To do that, what will I, I will use I will use silicon dioxide, I grow silicon dioxide I will tell you how the silicon dioxide is grown in one of the class. This is your silicon dioxide, this is silicon dioxide, this is silicon. Now you understand silicon dioxide will not get affected in BH in KOH.

Silicon dioxide in KOH which is potassium hydroxide, silicon gets etched it is an etchant for silicon is an etchant for silicon. But KOH will not affect silicon dioxide. That means if you dip the wafer with silicon dioxide like if you dip this wafer silicon will not get etched at all. So, what you do is you perform a photolithography and you remove oxide, you remove oxide from the top in this way to create a window to see you perform photolithography.

We will see photolithography in one of the class, silicon dioxide, silicon dioxide, silicon dioxide. So, I perform a photolithography to remove silicon dioxide from this particular area so that we can we can say that these are window that we have created through which we can see silicon. Now, if I dip this wafer in KOH for known amount of time, what will happen?

I will have my silicon dioxide as it is because silicon dioxide will not get affected in silicon etchant. We already know it is silicon dioxide and here you can see that silicon is silicon is etched. That means that silicon dioxide my silicon dioxide acts as a mask; acts as a mask that is why it is called masking oxide, that is why it is called mask, masking oxide.

Finally, if we looked at just we have seen in case of MOSFET it is one micron thick silicon dioxide that is used for field oxide.

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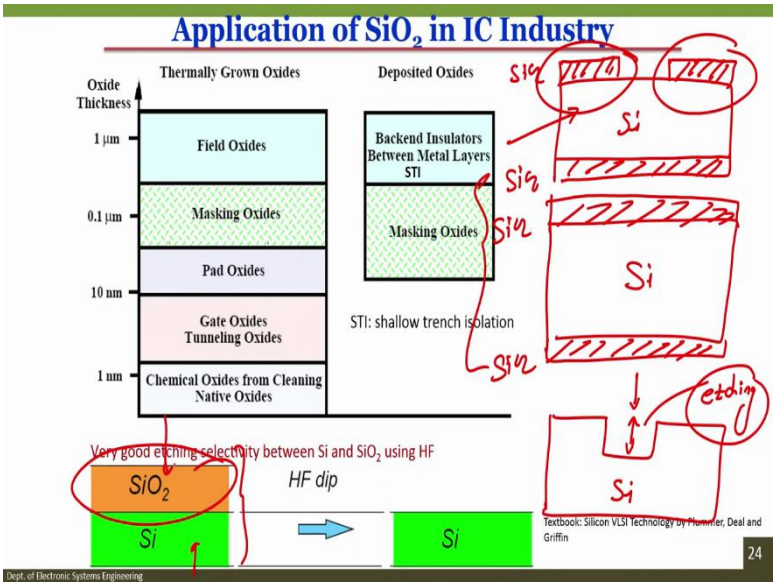

So, the same thing is you can see in this schematic that if I have silicon dioxide and if I dip in a HF then HF is a, HF forces silicon dioxide and that is why the silicon dioxide is etched. But if I dip this wafer into the silicon etchant like KOH or TMAH, then silicon will get etched from the backside, but from the front side do not get affected because silicon dioxide act as a mask.

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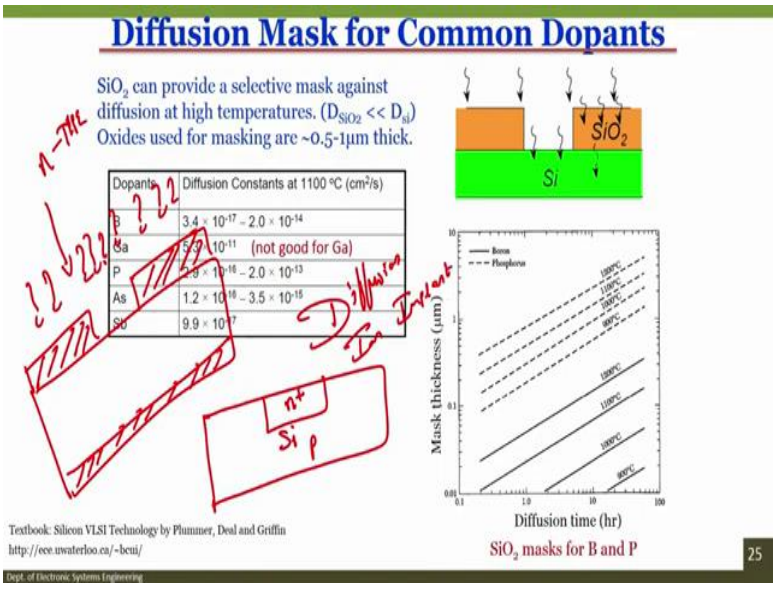

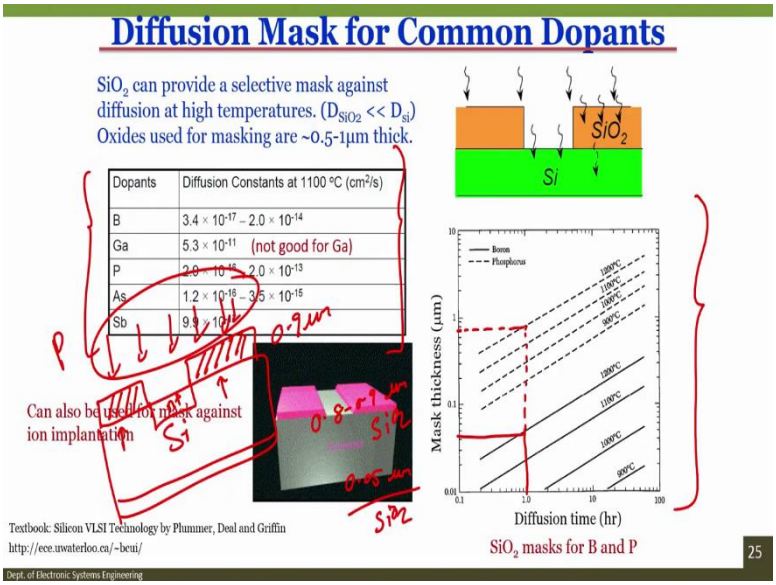

So, when it acts as a mask is not only mask against the silicon etchant, but it can also act as a mask of not allowing the dopant to pass through. That means in this case, what do you see if I have a silicon wafer And I want to dope silicon wafer only in this region. So, it p type silicon wafer, I want n+ dopant only in the centre of this silicon wafer. What can I do?

I will take a oxidized silicon wafer and then I will again remove the oxide from the centre and remining all the sides I will keep oxide as you can see here top and bottom and then if I dope this silicon dope this silicon by n type dopant, n type dopant. Then then there is two ways of doping silicon wafer one is called diffusion, one is called ion implantation, diffusion and ion implantation, ion implantation.

So, when you do diffusion ion implantation, these dopant that you are doping will cannot pass through silicon dioxide, cannot pass through silicon dioxide. Does again in this case silicon dioxide acts as a in as acts as a masking oxide. The silicon oxide acts as a select to mass against diffusion at high temperature because the D_{SiO_2} is extremely low and less than D_{Si}. As we know oxide is used for masking at about 0.5 micron to 1 micron thick.

And in this case, what you can see is that are different dopants under different constants at 1100 degree centigrade. The diffusion constant of silicon dioxide extremely less than different constant of silicon that is what I said about D_{SiO_2} less than less than D_{Si}. In this chart what you see is if I want to use silicon dioxide for as low as a mask for boron and phosphorus then how much should be my thickness.

So, from here if I use boron as a dopant into silicon wafer and if I am using a 1200 centigrade temperature then I had to draw like a line like this and then depending on how many hours. So, if I say that I am doping my boron for about 1 hour. So, if I dope my boron for about 1 hour at 1200 degrees centigrade, I require 0.05-micron thick silicon dioxide this is what it says. This chart shows like this.

Suppose you said no, I want to dope phosphorus into silicon for how much time? 1 minute, at what temperature? 1200 degree centigrade; then you can continue here and you can see that approximately what is the thickness? 0 point, 0.8-to-0.9-micron thick silicon dioxide can acts as a good mask for to not allow the phosphorous to enter silicon.

That means if I have silicon wafer here, and if I grow silicon dioxide like this, this silicon wafer and I want to diffuse phosphor into silicon wafer, then this silicon dioxide if the thickness is close to 0.5 micrometre, this low point which is your phosphor will not pass-through silicon dioxide. Thus, silicon dioxide acts as a mask against the dopant and protects the region which is below it.

That means in this region, you will not see dopant but in this region which is there is no silicon dioxide, you will see that there is a phosphorus doped into silicon wafer. Same thing is here, and there is a dry oxygen, wet oxidation. Let us see this dry oxidation, wet oxidation in the next class followed by lithographing followed by some of the examples how you can fabricate different chips that can be used for biomedical applications.

Till then you take care, have a nice day. Bye.