Design for Internet of Things
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Lecture - 20
LDO - 01

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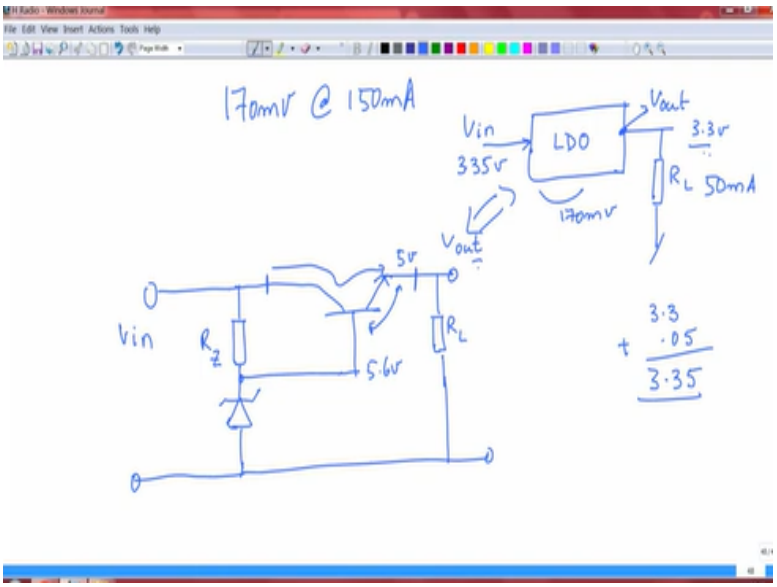

Okay folks, welcome back. You recall this picture we drew, about the input versus the output voltage. So, very close difference between the input and the output and at extremely low load currents the drop can be very, very low right? So, you want 3.38 output, you can just feed 3.35 volts at the input and then you can just drop a very small voltage across the LDO and beautifully it will still regulate the thing. This is something which is revolutionary as far as the voltage regulators are concerned.

When we started looking at linear regulators, what we know very well is in the world of Zener diodes and Zener regulators and so on. Just recall what we used to do in our earlier days a very simple circuit that you want to regulate. You have let us say Vin which is your input voltage and you want to Zener regulated. So, what you would do? You would put a series pass element, which is essentially connected to our well-known transistor which can be easily replaced.

Today nobody uses I mean; I would say put it the other way. Most often everything is MOSFET driven. You gave us MOSFET. I am sure you recall this picture, this is your R z current limiting resistor for the Zener and this is a Zener regulator. Here is your Vout, and to your Vout you can connect the load. The good thing about this circuit is that it will keep you well within regulation.

You have connected the Zener diode at the base, what you will get is a from the old transistor technology you will get a drop of 0.6 volts. If you have 5.6 here you will definitely get 5 volts and it will be stable. Any amount of current that is drawn will simply go through this series element. Basically, you are changing the conductance of this series pass transistor which allows you to draw various amounts of currents based on what the load requirements.

In our embedded world, sometimes R is a very high value and sometimes R is a very low value. The load currents that are drawn can be different. Particularly if you are sleeping current drawn is extremely small, it can be micro nano amperes. But if you are sensing and you are transmitting simultaneously, it can be 10 s of milli amperes. R L value equivalent can be varying. All that current supply comes nicely through this series pass element.

Folks; the beauty is this LDO is essentially something that has a series pass element inside it. But for the difference that you are not getting a drop; which is as huge as what you have here, but you have a very small drop between the input and the output. That is the only difference. Why did this paradigm come? Because this paradigm first of all technology has changed. So, we are not talking anymore of discrete components like Zener's and so on.

But everything packaged into a simple system plus a lot more circuitry, which will enable you to keep track of the output voltage any changes in the output load conditions. That has introduced the nice thing about how you can control this conductance of the series pass element. What is that circuit? How does that look different from this?

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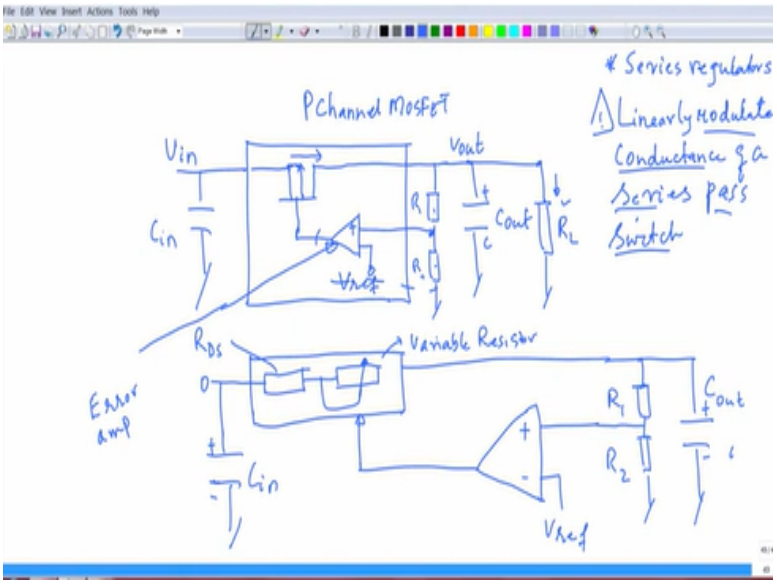

This is a standard P channel MOSFET which is your series pass element, no difference at all V in is here, no problem, V out is here. What is interesting is this circuit here with you see here, this whole circuitry here, it does the following. Same R L, which you saw here, same R L here is the same RL here okay>. Now, you see what happens. If there is any change in the load current, this load current change is sensed by these two sensing resistors R 1 and R 2.

This R 1 and R 2 sensing resistors will feed to a error amplifier. So, this is an error amplifier. This error amplifier will simply change the gate voltage, will modulate, will only open the gate more wider. When the gate voltage changes the current drawn will increase. Now whether to increase the gate voltage or decrease the voltage will depend on whether it is a P channel MOSFET or not.

So, do not worry about it, there is a change you have to change the conductance of the transistors I have written it here to the right side. The way to do that is to change the gate voltage. If the gate voltage changes, the current flows more current flows here this point under regulation always, the V out will always be under regulation. Why this game has changed is because today, in today's technology world, the resistance between the source and the drain is in the order of few ohms.

Hardly any drop across that resistor and how to visualize that? Second picture. Now, I have replaced the MOSFET with two resistors, the RDSon, the RDS - the resistance between drain

and source is one part. The other part is what you are changing with the gate voltage that is like a variable resistor. Both of them are in series, this essentially will keep varying this variable resistor will keep changing to some value to some small value over a small range.

So, that the output is always in regulation, V out is always in regulation, that is all that is there in a low dropout regulator. RDSon has gone to extremely low values. So, dissipation across the MOSFET has come down drastically and that is one part. Second part is because there is a very small R value, the difference between the source and the drain also has reduced has also shrunk because that is almost like a very low resistor value.

That therefore the ability for you to feed extremely small input voltages, which we showed here and getting out the difference between the input and the output being extremely low is because the RDSS and the variable resistor through which you control the gate will allow you to almost dissipate nothing across the LDO. Folks, that is all there is to an LDO, nothing else. In it is essence, it is just this one circuit, which you have to remember well.

And it is most logical also as you can see here. Very importantly, I have shown a P channel MOSFET. Can you, may ask now, can I make an N channel MOSFET series pass? Yeah, of course you can. If you make this N, this arrow will change, this arrow will be pointing in one other change you have to do is, here. This will now go to minus and this Vref will get plus thats all.

I made lot of assumptions, which I will now clarify with you. Let me put back the P channel MOSFET. How is this always remaining in regulation you may ask okay, the reason why it is remaining in regulation is because of the magic here because of this error amplifier. Look at what the error amplifier is doing? It has a reference; this reference is what is expected to be maintained at the output.

Any change with respect to the output this error amplifier will simply give you a certain voltage Out, which will modulate the gate and put it back to regulation. So, if load current changes; Vout goes tries to go out of regulation, that is sensed by these two resistors that appears at the input of the error amplifier Vref and error amplifier differences now, higher.

Because of the difference in high voltage difference between Vref and the sensed sample from Vout, the error amplifier gives a gain gives a voltage gain, which will be sufficient to drive the gate of the series pass transistor and therefore, current will increase and when the current increases Vout goes back to regulation. This is the point and that is all is there to this explanation. I showed you that the RDS is the resistance between the drain and the source of this MOSFET plus whenever the gate changes.

Gate voltage changes the small variable resistor which is connected in series these are all elements which are out there. These elements are during the construction of the MOSFET appear and that small variation in the resistance lowering the resistance value will increase the Vout to go back into regulation and this cycle continues. So, folks; that is the understanding of an LDO.

So, I found some material on the internet to be very useful for you to understand LDOs. And that I am going to show you. So, that you can read it yourself understand it very well and very nicely concisely he has put it. All the important parameters for design are out there. So, you must try and spend to understand them better. So, let us see what it says.

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First part is about defining what an LDO is? Not important at this stage because you know it so well. What is important is the power dissipation. What does he say about power dissipation? We already know this expression power dissipation is V in - V out into I load. The difference is what is dropped across the LDO. So, you recall what I showed you here, we said that the drop across the LDO here is just 170 millivolts.

That to when the current drawn is full current about 150 milliamps load current is being drawn. So, essentially how did you get this 170 because you know Vout minus Vin is the difference in the voltage. That difference into the voltage into the current is essentially giving you the power dissipation of the device. So, this paper, this website also is telling you the same thing, it is telling you that take Vin minus Vout into I load.

It will tell you the power dissipation across because the whole current is flowing through the LDO, it is not that LDO the output is generating power current by itself, it is has to flow through the LDO. The series pass element conductance is what we are changing and it is passing through from the input to the output the current is flowing. So, that current into the difference will tell you the power dissipation and essentially, that is what it says.

Now, higher power dissipation LDO requires larger packages. If you are dissipating lot of power across the LDO, the LDO has to even you should even apply a heatsink so that you can keep it cool. So, so much so LDO comes in different packages based on their power dissipation abilities. So, we will look at some of them as well. But before we go on, what I showed you as an example to understand I showed you about P channel MOSFET.

Now N channel is also possible and where do you apply N channel MOSFET is the question. So, we will come to that. Before that, if the LDO has to function, the LDO also requires some amount of current it not only is dropping the voltage. It requires a certain amount of current itself, that current is actually called the quiescent current, which is written here you see. I Q which is shown here is essentially the quiescent current of the LDO itself.

That should be very small. That means, input to output should be whatever load current that is required should come directly from the input and the device itself should not take any current which is a you know you know a proposition which is ideal but never going to happen. Any device that is intervening will have to require some amount of current itself in order to function. But you want to keep it very, very low and this design is saying about I Q of the LDO should be look out.

So, look out for the quiescent current of the LDO this should be very, very small if you are doing battery driven applications for your IoT device.

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Quiescent current of the LDO, the current consumed by the LDO. See this has different impacts, you may say that Sir, if I am not using the output of the LDO can I keep the LDO disabled? Answer is yes, you can keep it disabled. Even if you keep that LDO disabled, there

is a certain amount of small current flowing to the ground. It is flowing to the ground. That is one type of current leakage, some sort of leakage current ,will be flowing.

Different companies give different names to it. Some people call it shutdown current. Some people call it shutdown current. So, all leakage current is another name. So, you can you look up the data sheet you will know these things. So, be very clear that quiescent current is not the same as the shutdown current. Quiescent current is the current that is consumed by the LDO during its active functioning, itself is taking a very small amount of current.

In order to allow the I load which is required to come from the I in without itself consuming anything significant, extremely small. So, that is about it. Then there are applications which require because this is a linear regulator, you want that very clean DC output, we mentioned that already plus the noise of the LDO should be very, very low, it should be extremely low, in terms of noise support.

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We discussed about low noise, good PSRR. We never defined that yet. We will come to that all of them as we go along are some of the key criteria. He is saying the same thing that we discussed in our overview. Okay. This website talks about two types of LDOs. The LDOs on the left side is PMOS. You can see that this by this arrow, we have V in and V out and here is the same V in and V out.

And the gate is controlled pulled up and down based on the fluctuations in the i load. Therefore, the transistor can be you change the conductance of the series pass in order to keep the output at regulation. And all that is done using this error amplifier and the sensing resistors R 1 and R 2. Sometimes this R 1 and R 2 can also be inside. So, look out for manufacturers which may want to put them inside, in which case they will be mostly fixed output LDO.

You cannot have variable. So, that is one issue with that will come. Now as far as NMOS is concerned. The NMOS LDO requires an additional circuit which requires a charge pump. Because the requirements of VGS in order to ensure that you control the gate of the

conductance of the transistor, you need VGS which is higher than the output. And therefore, you need an external V bias circuit.

Either you put a V bias a circuit, or you put a charge pump, either one of the two will be required. And that is explained here. Now if you look at LDOs, N channel MOSFET need a gate drive which is higher than the output voltage. It is written here clearly that you will need a VGS higher than what is given at the output and therefore, how will you generate that .okay. So, you need to do that you need a charge pump.

Now, the good thing about NMOS LDO is RDS, the RDS is very low compared to PMOS. So, the drop across the input to the output can be even more low and it is very good for low voltage applications. Particularly IoT applications in the range of two volts and so on will allow you to use NMOS. If you choose an NMOS system and NMOS LDO your RDS can be even more lower.

This makes the possible use that these LDO with very low input voltages down to even one volt. Okay. So, you want one volt at the output you give one point to at the input you will get one voltage to the output. So, very low input voltages itself you can regulate. So, that is the good thing about the N channel because of its inherent characteristic. Whereas, PMOS is also good, but when you see a LDO which is in the range of 3.3 volts or 5 volts LDO and so on.

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You can be more or less sure that those LDO was must be the P channel type of LDOs. So, that is essentially what the this document is saying.

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So, you can see he writes in dark here, minimum input voltage requirement of about 2.5 volts is actually indicated here. Now, this picture is interesting okay. I come to this picture because that requires a separate discussion. Before we go on, I will show you one more note with respect to LDO, some more few things you need to know. This is again a recap; you have you can see this is a P channel MOSFET.

There is no additional circuitry for generating the using a charge pump for generating VGS higher than the output voltage. You do not need anything here you have input capacitor and

you have the output capacitor. And this is same thing he has shown in this picture to the right where he shows that the sensing resistors are kept outside. So, do look up for this aspect as well.

Now, this expression is known to you V - V out into the I load is essentially the drop power dissipation across the LDO. This picture on the right side tells you something about the different power dissipation values here. You can see the power dissipation is 0.25 watts that is 250 milli watts to about 1.25 watts. All these power dissipation values are shown here you can easily see that the 0.25 milliwatts is essentially for extremely low load currents.

The drop across the LDO is low and you can see that he mentioning it here. The right graph shows LDO voltage drop versus LDO load current for specific power dissipation values larger current or larger voltage drop across the LDO quickly leads to high power dissipation. Either you draw high current or you have larger voltage drop will increase the power dissipation across the LDO.

Now, if the power dissipation across the LDO is definitely going to be high. Then choose your package accordingly, the packages are SOT-23-5 to TO-252-3. You can see that different packages for the same input output conditions that you are looking for different packages will support you different power dissipation. It can withstand that power dissipation. Now, this picture that you see here is a P Channel series pass element.

You also have an error amplifier here; you have the two sensory systems here and this is the output here. You can see that this is the source, this is the drain and this is the gate. Now, you keep pulling this gate, in whenever there is the output voltage, whenever the output load current changes, the output voltage tries to go out of regulation. Every time that happens, the conductance of the series pass element has to be changed.

And how do you do that? You keep pulling the gate with respect to the source. And how do you see that plot? This is a very well known plot of what we have different VGS's are shown here. The minus sign is attributed to the fact that this is a P channel MOSFET. And you know

that you have to connect accordingly the polarity of the VGS with respect to the input which is Vin, this VGS has is controlled is entered.

You keep pulling it up and down and changing the transconductance. You can see that this picture here is telling you that the MOSFET is now moving towards the ohmic region as it is called and this ohmic region will not let you regulate the output voltage anymore. But it still gives you very good ability as long as you are able to maintain the required drop, the system is under very good regulation.

So, that discussion is mentioned in this paper as well. And the process simply gets reversed in the case of the N channel MOSFET, I would want you to explore how that happens and why a charge pump would be required there. What is next is we discussed enough about the LDO and it is functioning, but what we did not discuss is PSRR. Now, if your device is in output wherever, for example, you are connecting the output of the LDO to an ADC V ref.

Then you need extremely stable output voltages, you need very low ripple and there should, it should not be susceptible to any noise. So, essentially, you are going for a low noise regulator is a good choice for this supply. Now, what you see on the right side is the frequency of the input versus the PSRR on the y axis. Power supply rejection ratio is simply plotted on the y axis it is plotted in dB.

What you see is if you have low load current, the PSRR is maintained well. For the same load currents, if you keep the input frequency of the input signal more the supply ripple start increasing and the ripple gets in the range of the 10k and so on range. The variation, the drop in the PSRR is appears to go in this manner, you can see that it touches drops to minus 20 dB and then improves after that.

And so, essentially you have one picture, which is telling you about the load current. Now, the PSRR is directly influenced also by the load current, under high load again there is a drop in PSRR. So, please note the two variables that you have to keep in mind when you design your PSRR. One is that when you choose your LDO for a certain rejection ratio, you have to keep two parameters in mind.

One is what is the maximum load current? And the other is the frequency at which it operates. These two points have to be noted. You can see straightaway the difference between the load current changes in the drop in PSRR due to load current. Frequency is low here, but load current is high okay. And as you move to the other side, this difference continues to be maintained up to a certain point and after that there is a crossover and it gets a little more unpredictable.

So therefore, the point is as frequency increases the loop gain of this control loop of this LDO starts to reduce. The loop gain reduces due to bandwidth limitation, limit on the LDO and the PSRR curve starts to rise. So, this website is also telling, you giving you information about PSRR. Now, the question is what can you do if you know about all this? Can you do something to avoid it? The answer is a big yes.

Look what happens. Here is talking about some additional circuitry which you can add and this is called the high frequency bead, which can be applied before you feed in the signal to the V in. This high frequency bead actually is removing all the ripple that is coming as an input from into the LDO. And that ripple can be removed with this high frequency bead the design the choice of high frequency bead is also important.

It is not that if you have a problem of a 300 milliampere current draw, and you want to ensure good PSRR, it is not there is no solution. There is and this is essentially what the solution is. But what is the drawback of the solution? You need an additional circuitry to put a high frequency bead and then filter out the high frequency ripple and then feed it to the input of the LDO.

Now, again, you must note that every time we drew anything about the LDO, there was an input capacitor and there is an output capacitor. Please note they have huge bearing on the ripple of the LDO to control the ripple you can basically manipulate these capacitors.

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However, transient response becomes a big, takes a little beating if you increase the size of the capacitance. Its ability to respond to transients may be difficult particularly the output

capacitor C out has a problem. So, again it is a very careful choice of what should be the value of the output capacitor. So, the transient response is good, yet it can take care of sudden increases in the load currents.

Any increase in the load current should be coming from the capacitor right? So, that you do not disturb the control loop and put back the error amplifier and pulling the gate up and down at the input, you want to avoid all that as much as possible. So, put a large capacitor but large capacitor at the output as I mentioned has a problem with the transient load response, transient response. So, you have to balance between transient responses and so on.

Similarly, input, input if you want to avoid ripple, you can plan the input capacitor. And also, you if there is ripple that you want to avoid as an input to the LDO, you put this high frequency bead, which I mentioned here.

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This application note actually is talking about that bead itself. Now, I also mentioned to you about the fact that LDOs have to not consume anything at all. In fact, that is not possible but very little current should be consumed. And here is an example of what this paper with this application note is telling us. That LDO quiescent current is the current consumed by the IC internal feedback control and it should be as low as possible.

Now, he talks about one micro ampere of quiescent current. And this one micro ampere is it lower the better one micro ampere will allow you to put the increase the battery life of the system. So, this document comprehensively talks about the whole issue related to choice of LDOs. What we will also do is take some examples in understanding good interpretation of the data sheet of an LDO.

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So, that we connect everything and take a very small example as usual, solve that problem and see how all these parameters can be well understood from a data sheet perspective. Thank you very much.