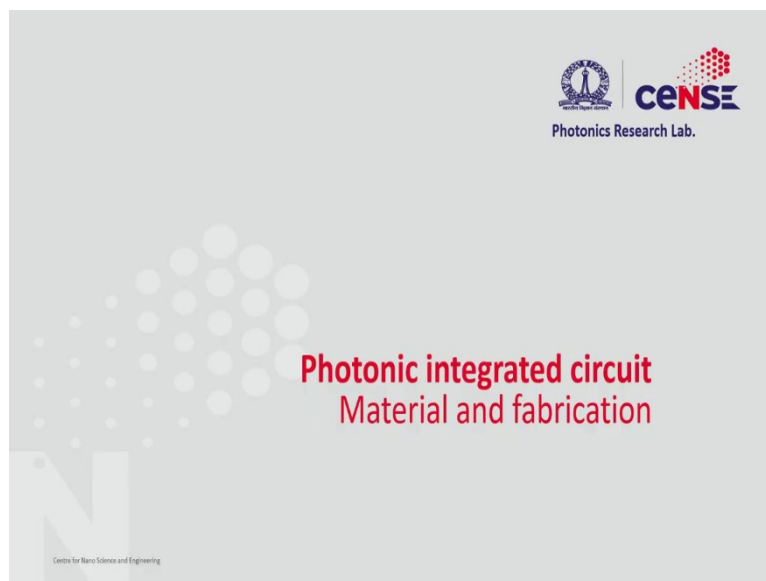



Photonic Integrated Circuit
Professor Shankar Kumar Selvaraja
Indian Institute of Science, Bengaluru
Lecture 46
Fabrication Process – 1

Hello, everyone. Let us look at how to fabricate a photonic integrated circuit. So, this involves understanding of the material that you want to use and also the fabrication technology one have access to. So, let us look at the technology aspects and then we can also discuss as we progress through the fabrication process about material and material complexities. So, let us look at different materials and also primarily the fabrication process.

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What is a process flow?




- Waveguide fabrication ✓
- Coupling grating ✓
- Thermo-optic tuner ✓
-

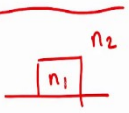
- Wafer cleaning
 - Organic clean
 - Inorganic clean
 - Metal clean
- Waveguide module
 - Waveguide lithography (mask-1)
 - 220 nm Si etch
 - Photo resist strip
 - Wafer clean
- Coupler module
 - Lithography (mask-2) ✓
 - Si etch
 - Photoresist removal
 - Wafer clean
- Oxide planarization
 - Oxide deposition
 - Chemical mechanical polishing
 - Wafer clean
- Thermo-optic tuner
 - Metal deposition
 - Metal lithography (mask-3)
 - Metal etch
 - Photo resist removal
 - Wafer clean

2

What is a process flow?




- Wafer cleaning
 - Organic clean
 - Inorganic clean
 - Metal clean
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- Thermo-optic tuner
 - Metal deposition
 - Metal lithography (mask-3)
 - Metal etch
 - Photo resist removal
 - Wafer clean

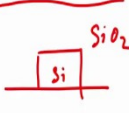


2

What is a process flow?



- Wafer cleaning
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 - Inorganic clean
 - Metal clean
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 - Oxide deposition
 - Chemical mechanical polishing
 - Wafer clean
- Thermo-optic tuner
 - Metal deposition
 - Metal lithography (mask-3)
 - Metal etch
 - Photo resist removal
 - Wafer clean



2

So, when we say fabrication process, we want to fabricate a particular type of device let us say, in this case we want to fabricate either a waveguide or you want to fabricate a coupling grating, or we want to fabricate a thermo-optic tuner let us say. So, these are all different devices that you can fabricate on the wafer. So, there are multiple steps that one should follow in order to achieve the desired structure on the wafer.

A simple process flow would look something like, like what is mentioned here, we should start with cleaning the wafer. So, we have, we have a silicon wafer let us say and the silicon wafer should be cleaned first. So, it might have organic contaminants, inorganic contaminants or also metal contaminants. So, you want to clean all of this, so it goes through a detailed cleaning and once the cleaning is done you should then start with the modules for fabricating the device now.

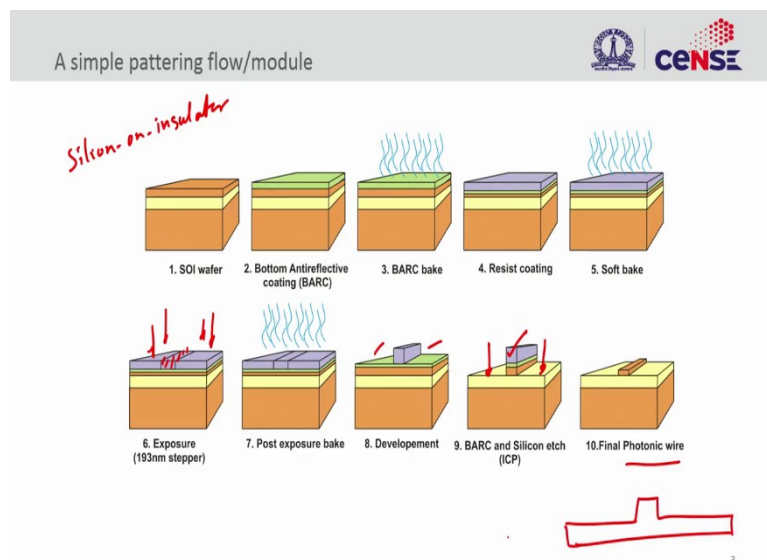
So, the first step is the lithography step, and once you, you have your lithography done using mask, then you have to etch or make a pattern in the silicon or whatever material that you are interested in, and then you remove the photoresist that you use to do lithography followed by again wafer cleaning and then this will define the waveguides.

And now the next step is to make some coupling device let us say, so in this case it is a grating coupler, and you again go through a lithography step, dry etching step, followed by resist removal and wafer clean. If you look at the, the type of steps, they are all identical, but the masks are different, the type of structures that you are going to write are going to be different here.

So, we will look at what this mask is all about as we discuss this patterning process, followed by deposition of the cladding. So, when you when you make a waveguide then it will have a refractive index of n_1 and then let us say you want to cover it with another material of refractive index n_2 , in this case this n_1 material is Silicon and the cover that you are going to put is Silicon dioxide.

So, you need to deposit oxide you need to do some polishing in order to make it flat and again it comes to wafer cleaning. And then for thermo optic tuner you have to do metal deposition, metal lithography, metal etching followed by resist removal and cleaning. So, these are all the fundamental process that one should go through. So, we will look at the key processes so that you can build based on that understanding any kind of process flow or any kind of fabrication process that you may want to do.

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So, this is how pictorially we could visualize how these processes will happen. So, this is only for one single edge step let us say where we define a photonic wire waveguide. So, you start with a Silicon-on-insulated wafer SOIs, Silicon-on-insulator wafer and then you do a bottom anti-reflective coating and then you have to bake the coating to remove the solvents followed by photoresist.

So, this is a photosensitive material that you coat on top of resist, followed by a soft bake step that is you are going to remove the solvents from the photoresist here, and then followed by exposure. So, this is where you are going to expose the region that you want to keep and then what you do not want to keep since we have a thin film here, we just want a wire.

So, you make sure you write a line here and after exposing it, that means you are illuminating with light source the region that you do not want, and then you will go through a post exposure bake, so this bake allow, allows you to chemically change the exposed part,

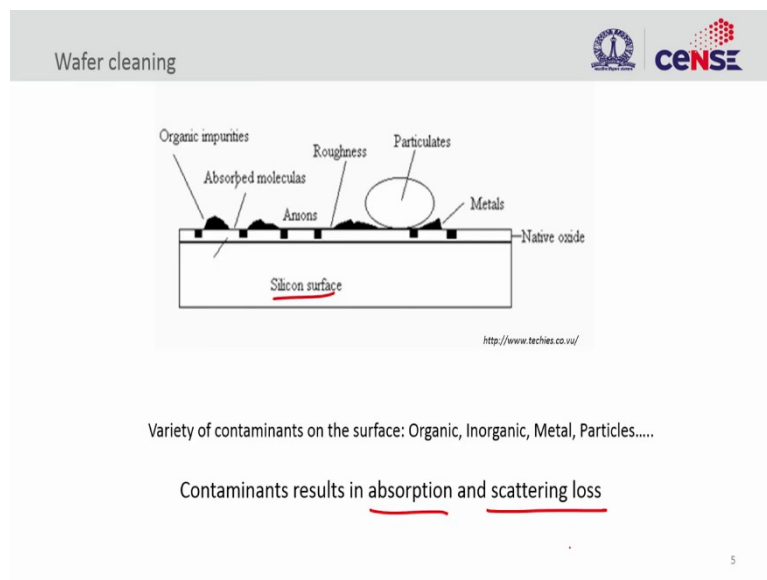
followed by development. So, in the development step is where you remove the material that you have exposed, so the remove, the exposed photoresist material is now removed.

And now we are going to etch away the material, this is done using inductive coupled plasma where you can etch through the material and after etching through the material you can remove the photoresist here. So, at the end you will get a nicely defined photonic wire waveguide. So, we repeat this step for other edge steps. So, if you want to have a shallow edge waveguide we go through similar kind of process.

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So, let us look at each and every step that we discussed, first thing is the wafer clean. So, the contamination is, is results in absorption and scattering loss. So, any contaminants that you have on the wafer will result in light absorption and light scattering. So, what kind of contaminants you could have? You could have organic contaminants, you could have inorganic, metal, and other particles.

So, the organic contaminants mainly carbon containing it could be or inorganic (con) contaminants this could be either silicon or any other material that, that is formed as a particle, it could be metal as well. So, they are all sitting on the surface. So, if you have a Silicon surface in this case it will have a native oxide and you have all these contaminants sitting on the surface. So, this contaminants are going to result in absorption and scattering loss which is something that you want to avoid. So that is the reason why we want to clean the surface.

(Refer Slide Time: 07:14)

Wafer cleaning




- **Wet clean** *Using wet chemical*
 - Solvent ✓
 - HF clean ✓
 - RCA clean ✓
 - Piranha clean ✓
 - Ozonised cleaning ✓
- **Dry cleaning**
 - Plasma assisted
 - Gas

6

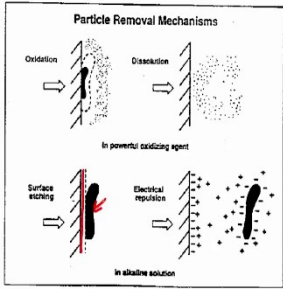
There are two ways to clean the surface, one is wet clean the other one is dry clean. So wet clean means using wet chemicals. So, this is hydrofluoric acid, this is RCA clean and then you have Piranha clean and oxidized cleaning, or you can also do solvent clean. So, these are all different wet chemical cleans that you can use, or you can use dry cleaning. So dry cleaning meaning you can use plasma, or you can use gas in order to clean it.

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Wet clean



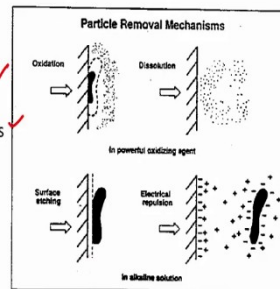
- Oxidize and remove organic contams
- Oxidize and remove inorganic contams
- Create clean interface (native oxide)



The diagram illustrates four particle removal mechanisms: 1. Oxidation: A surface with particles is treated with a powerful oxidizing agent, leading to the formation of a native oxide layer. 2. Dissolution: The oxidized surface and particles are dissolved into the solution. 3. Surface etching: A surface with particles is treated with a solution, leading to the removal of the surface layer and particles. 4. Electrical repulsion: A surface with particles is treated with a solution, leading to the removal of the surface layer and particles through electrical repulsion.

9

- Oxidize and remove organic contaminants ✓
- Oxidize and remove inorganic contaminants ✓
- Create clean interface (native oxide)



9

So, let us look at what is the cleaning principle one can use. So, one strategy is to oxidize and remove the organic contaminants. So organic contaminants are primarily carbon containing. So, carbon containing could be oxidized, so you can make the carbon contaminant sitting here oxidized and then you can remove it by dissolving it.

So, the other way is to do is also oxidize the surface and then remove inorganic. In this case you are going to oxidize the surface, so inorganic contaminants may not be (oxidi) may not be able to (oxidite) oxidate it. So, instead of looking at other options, Silicon could be oxidized. So that means you can oxidize the surface here and then by using appropriate solution you can take out the contaminants by using really interesting charge transport here, so using repulsive forces you can take out this particle out of it.

So, by using these two strategies both oxidizing, one is oxidizing the contaminant itself but the other one is oxidizing the surface and then you can remove it. So, this would result in a very clean surface and this clean surface will have the native oxide, in this case Silicon native oxide is Silicon dioxide.

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- Developed at Radio corporation of America(RCA) by Werner Kern in late 60's
- 3 step process
 - (RCA-1) Standard clean 1 (Organic clean, particle, some metal)
 - Ammonia, Hydrogen peroxide and DI water (1:1:5) at 70C
 - Diluted Hydrofluoric acid
 - (RCA-2) Standard clean 2 (Metal and trace metals)
 - (7%) Hydrochloric acid, (30%) hydrogen peroxide, and DI water (1:1:5 at 70C)
 - Diluted (2%) Hydrofluoric acid clean →
 - Rinse with DI water

removes SiO₂

Si

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So, we talked about RCA. So, there are two chemicals that I mentioned one is RCA and another one is Piranha clean. So, let us look at the RCA clean. So, this was invented by Radio Corporation of America where they want to clean the wafer, so that you can remove the organic and metal contaminants. So, there are two steps involved here, there is RCA-1 and RCA-2.


So, in RCA-1 there is ammonia and hydrogen peroxide is used. So, this helps you in oxidizing, so this is a heavily oxidizing agent ammonia and hydrogen peroxide, and then you have diluted hydrofluoric acid. So, this dilute hydrofluoric acid will dissolve oxide. So, silicon dioxide can be removed using this. So, you can remove both organic contaminants by directly oxidizing it or you can also oxidize the surface and then remove it by using dilute hydrofluoric acid.

The second step here is to remove metal and trace metal contaminants. So, metals are very detrimental to our optical propagation as we all know metals absorb light. So, the imaginary part of our susceptibility is, is non-zero. So that means they absorb light here so in order to remove that we use hydrochloric acid with hydrogen peroxide. So, there is oxidizing agent here as well by using this combination of 70 to 30, so this is 70% to 30%, we can remove this metal contaminants but both at 70°C, slightly at elevated temperature.

So, after going through this clean, we put the solution through hydrofluoric acid. So, this hydrofluoric acid removes Silicon dioxide. So, this is on a Silicon surface, so it removes Silicon dioxide and leaving out a clean Silicon substrate for us to start with. And finally, we do a DI water rinse that will remove whatever hydrofluoric acid left on the surface.

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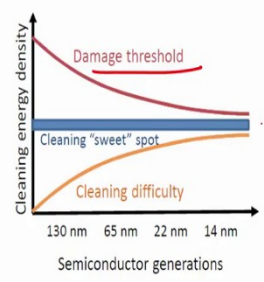
Pirana clean



- To clean organics and gross particulate contamination
 - Strips photoresists
 - Standard clean for SiGe & Ge wafers ✓
 - Used as pre-clean before RCA clean

- Recipe
 - H_2SO_4 (98%): H_2O_2 (30%) = 4:1 to 2:1
 - Temperature 120-80 °C
 - Try to use least aggressive recipe

- Mechanism
 - H_2SO_4 reduces organic to carbon
 - H_2O_2 oxidizes carbon to CO_2



Cleaning energy density

Semiconductor generations

130 nm 65 nm 22 nm 14 nm

The next type of clean we talked about is Piranha. So, Piranha clean is primarily used to clean organic contaminants. So, we can use it to remove photoresist which is again a organic polymer and we use it for both Silicon, Silicon germanium and also Germanium type samples. So, this is used before RCA clean in order to remove all the organic contaminants.

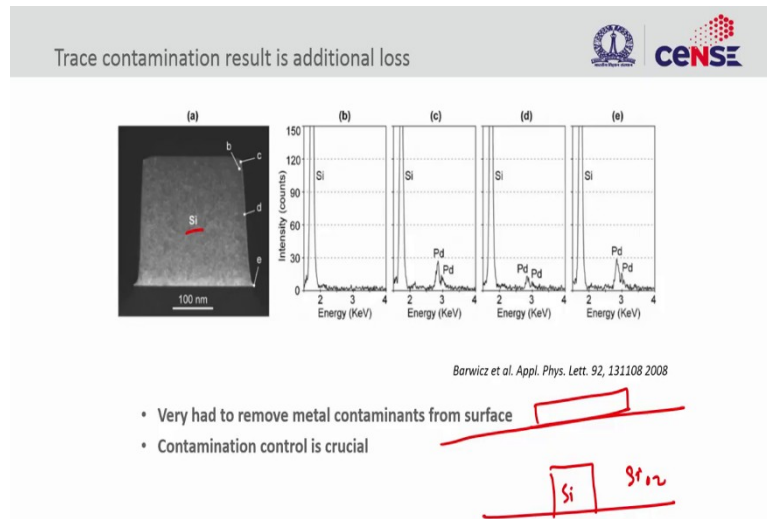
So, the composition of a piranha clean is a sulfuric acid with peroxide. So sulfuric acid 98% concentrated sulfuric acid with peroxide. So, in the ratio 4 : 1 or 2 : 1, but at some elevated temperature. So, by keeping it at elevated temperature they could react well this the reaction

it also is exothermic, it will remove all the organic contaminants. So as the mechanism states here the, the sulfuric acid will react with organic to create carbon.

So, it break down the chain and and make it all carbon on the surface and the oxidizing agent is going to create carbon dioxide out of it. So, whenever you do this clean you will see the bubbling happening and this bubbling is, is due to the creation of carbon dioxide from the surface due to this oxidation of carbon. So, as you, the cleaning is, is very important as you can see here when the structure dimension are becoming lower and lower the energy density that you have also need to be preserved here.

So, so the energy on the surface that is required in order to create damage is also going down. So, you want to make sure that you do not damage the surface. So, as you clean the the, the wafer you do not want the cleaning solution to damage this surface. So that is why very aggressive clean are good but then we should not damage the underlying substrate here, so that is the whole point.

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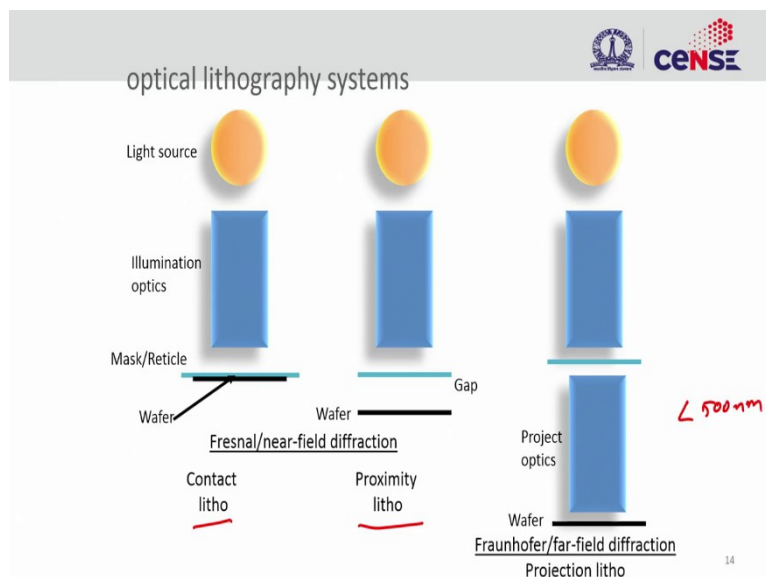


So even after cleaning the substrates with, with all kind of necessary cleaning chemicals if you have certain contaminants, you may not be able to remove it at all. So, you have to make sure that you do not expose the substrate to any metal contaminants. So, any trace contaminants in this case. So, what you see here is a is a Silicon wire wave guide and they have done XPS on various locations.

So XPS tells us what are all the material present on the surface. So, you can see here there is a metal contaminants present on the wafer, that this wafer was already exposed to this metal contaminant. So, because of this it is, it is very hard to remove this metal contaminant. So, it is very important to note down that when you are making photonic integrated circuits you should not expose your waveguides to meet any metal contaminant process.

If you are going to use metal, you should always use it after producing your waveguides concealing the waveguide and then you can bring any metal on top. So, you should not directly expose the surface of our waveguide devices to, to metals because it is very hard to remove metal contaminants from the surface you will always have some trace content of metal on the surface.

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So, once we are we have cleaned the surface the next step is to pattern this. So, I have a clean wafer now, so I want to transfer the pattern and we use optical lithography to transfer this pattern and there are three popular ways to do optical lithography. So, one is contact lithography, the other one is proximity. So, these two come under near field imaging and then the third type is projection lithography.

In projection lithography we use projection optics in order to write. So, the projection lithography is primarily used for large volume production, while contact and proximity lithography is used when you are doing research and large features let us say, so particularly for optical devices that are very small we need projection lithography. So, when the feature dimensions are less than 500 nanometers.

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Photoresist

- Material that absorbs exposed light (particular wavelength) and undergoes chemical change.
- Solubility of the photoresist changes with exposed light.

Exposed section is removed (+vePR)

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So, how do we transfer the pattern? The pattern transfer happens through an indirect process. So, you should already have a mask that contains the design that you want to write, that is what we call mask, photomask or stencil. So, this should be already made. So, this can be made from your CAD design. So, you do a circuit design in some automated tool like a circuit design tool, and you use that CAD design to make this mask. And this mask allows a certain region for light to pass through and certain region to stop.

So, when you expose this photo sensitive material that we coated on top of the substrate when you expose it so the solubility of this material would change. So, when you expose it, it becomes soluble. So that is called positive photoresist. So, you can also have the inverse, so when you expose you can also make the material insoluble.

So, in both these cases there is a chemical change that happens, and that chemical change also depends on the, the wavelength of exposure that you use. So, based on the, the right photoresist and the wavelength that you have, you can create this sort of pattern on the photoresist. So now we have whatever we want transferred from the mask on to the photoresist here.

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Photoresist: Novolak (i-line)

Substrate

Substrate

Substrate

Insoluble sensitizer (Inhibitor)

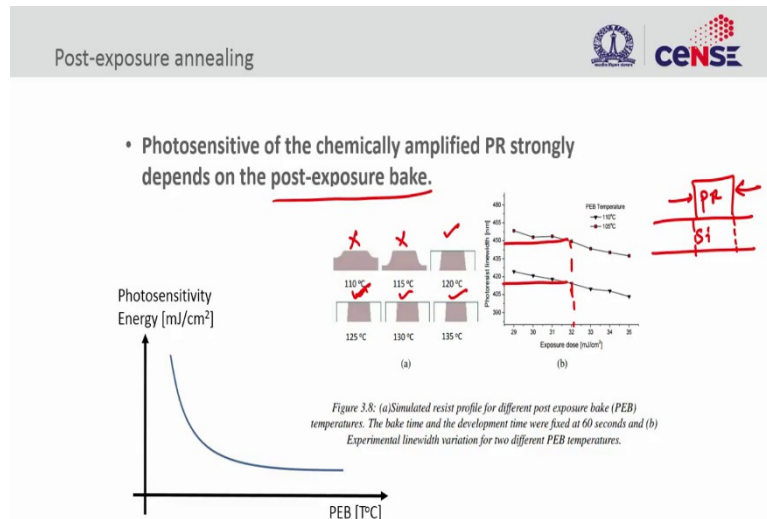
Soluble Photoproduct (Acid)

Allen, R. D., Conley, W. E. and Kuntz, R. R. Deep-UV Resist Technology. [ed.] P. Ray Choudry. Handbook of Microlithography, Micromachining and Microfabrication. s.l.: SPIE Press, 1997, Vol. 1.

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So, let us look at how this photoresist chemistry actually works. So, when you have the substrate, you expose it through with this light that you have, and what it does it is, it changes the insoluble sensitizer that you have in your polymer material that you have and then makes it soluble. So, this is acid soluble to be precise. So, by using this chemical change you can transfer the patterns.

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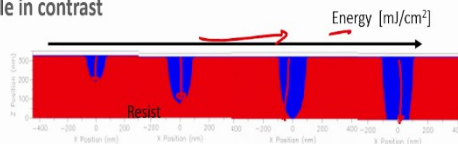
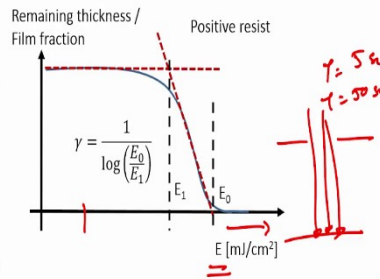
And once you have exposed in some of the resist you have to anneal it and what we call post exposure anneal. So, when your anneal temperature is not appropriate or not optimized then you would not be able to create the structure you want. So, so these three structures are something that you, you can qualify as a transferred pattern, but then these two are not yet exposed. So, one should keep track of the requirement of this post exposure bake based on the (temp) photo resist that you use.

So, in this case it is a chemically amplified photoresist that requires this post exposure bake. In some of the photoresist you do not need this post exposure bake, if that is the case you do not have to apply this baking or annealing of this substrate. So, another implication of this post exposure bake is the size itself for the required dose you can, you can have very large change in your critical dimension or the photoresist line width, in this case the waveguide line width, so this is Silicon let us say, so this is your photoresist.

So, you want to use this photoresist to define the waveguide. So, the photoresist with itself strongly depends on this post exposure bake temperature. So, as we have seen in our earlier lectures on the design of, of the wave guides, the width is very important and also when we talked about lasers and light emitting diodes the width of your junctions are also very important. So, we should be careful here to choose the right baking temperature so, that you achieve proper image transfer or pattern transfer.

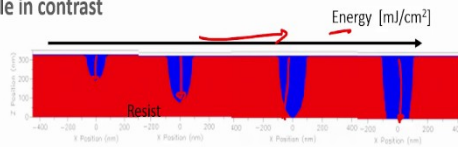
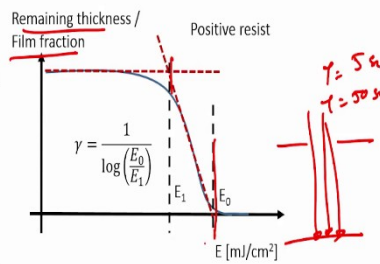
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- Contrast of a resist is an important property that determines the suitability and performance.
- Contrast curve : Remaining photoresist fraction of a **uniformly illuminated resist** Vs **Exposure dose**
- Resist chemistry plays a major role in contrast



18

- Contrast of a resist is an important property that determines the suitability and performance.
- Contrast curve : Remaining photoresist fraction of a **uniformly illuminated resist** Vs **Exposure dose**
- Resist chemistry plays a major role in contrast



18


It is not just the, the post exposure bake but also your dose itself like how much exposure that you give. So that is given by E here, so how much energy is exposed to this photoresist layer. So, what is this, this exposure dose? This is nothing but integrated energy over time. So, when you are opening this exposure so you wait for, you can wait for 5 seconds, or you can wait for 50 seconds.

So, when you wait for 50 seconds, the dose is going to be very high, because you are getting a lot of photon flux integrated and when you have 5 seconds you will have very less amount of photons going through. So, by changing the exposure time you can increase your dose. So, the dose meaning how much of photon flux reaches the surface, so that is the energy per unit area here, so some milli Joule per centimeter square is the unit that we use here.

By looking at this curve you can see here this is the photoresist and when you increase the exposure energy it starts developing because it is chemically getting changed. So that is what see here at the bottom so when you increase the energy, when you increase the energy, you can see you can expose the full thickness of your photoresist and the curve that that helps us in understanding how much energy we need is called this contrast curve.

So, when you have very large energies then all the photoresist is removed. So remaining photoresist is 0. When you have very low illumination you will not, so the slope is very important to understand that what is the minimum exposure dose required to completely remove the photoresist or expose the photoresist.

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Development


- Following post-exposure bake the exposed(+ve) part of the resist is removed using a base-developer.
- In manufacturing, development is done in a spin stage.
- For small samples, dip development is sufficient.
- Final pattern depends on developer, development time, method used, etc...

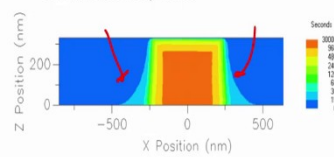
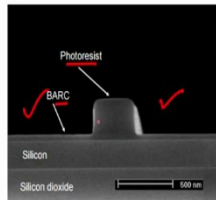



Figure 3.9: Simulated resist profile for different development time.

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And after exposing there is a chemical change that has happened but then the chemically changed photoresist is removed using a wet chemical process using an acid to develop this particular exposed, this is similar to our photo film development. So, you expose the film from the using the camera but then the image is there, but you cannot see that image. So, you have to develop that film, so that development is done using a chemical process.

The same thing applies here as well, so what you see here is, a photoresist that is sitting there this is the bottom anti-reflective coating layer, and all the resist is removed you see from the sides and that is removed by putting the (develop) developer on, on this wafer. So, the developer solution will etch away the, the material that is exposed and results in the, the unexposed part remaining there.

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Metal ion containing (MIC) ✓

- Made with NaOH/KOH
- Cheaper
- BUT, Na/K contaminates device
 - Especially bad for MOSFETs, diodes, etc.
 - Usually labeled as
- Used in MEMS, developing photomasks

Metal ion free (MIF) ✓

- Made with TMAH
- Expensive
- Na or K free
 - Can be safely used in CMOS and front-end process
- Used in electronic devices, photonics

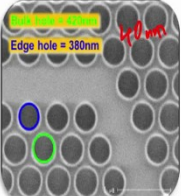
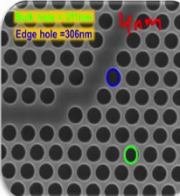

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So, you can do this development using two different type of chemicals, one is metal ion containing chemical and the other one is metal ion free chemical. So, potassium hydroxide, sodium hydroxides are metal ion containing base that you can use in order to remove your, your exposed photoresist, while tetramethyl ammonium hydroxide called TMAH, tetramethyl ammonium hydroxide can also be used to develop this.

The only difference is the metal ion free is, is reasonably expensive compared to metal ion containing. We always prefer to go for metal ion free, the reason for this as I mentioned earlier, we do not want any metal contamination or metal ion contamination on this surface. So, any metal ion on the surface will result in absorption loss.

So, we avoid this metal ion containing developer for our photonic devices and particularly also for electronic devices at the front end of it where you are making transistors, we avoid using this. And the metal ion containing can be used for other application like MEMS and mask production also you can use this.

(Refer Slide Time: 25:30)

0.18 μm	0.13 μm	45, 2X nm
<u>248nm lithography</u>	<u>193nm lithography</u>	<u>193nm immersion lithography</u>
<ul style="list-style-type: none"> › First generation Large Scale PICs › Functional device demos › Poor Uniformity › Limited in resolution for dense structures (PhCs) › Low overlay accuracy › Still used by research fabs and BEOL › Lower cost 	<ul style="list-style-type: none"> › Matched device › Good device uniformity › Higher resolution for dense structures (PhCs) › reasonable overlay accuracy › Reasonable cost 	<ul style="list-style-type: none"> › High resolution, sub wavelength › Good device uniformity › Complex circuits › Good overlay accuracy › Integration opportunities › High cost › Industrially relevant
		

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So, the patterns could be done using different type of illumination process, we start from the, the illuminating wavelength of 148 nanometer lithography or 193 nanometer lithography and you also have 193 immersion lithography. So, you can have 180 nanometer technology, 130 nanometer technology or 45 and below nanometer technology.

So, we use this technology to make photonic devices and these devices have their own resolution effects from this different patterning process. So, when you look at 180 nanometer technology you can see the photonic crystals that we, we make they do not come out identical. So you are, you have designed these holes in the photonic crystal to be identical in this particular geometry, but they are not identical because of what is called proximity effect.

But then when you decrease the (wave) wavelength going from 248 nanometer to 193 nanometer, in this case 130 nanometer technology the difference between the holes are now one order low. So here it is 4 nanometer difference and here you have 40 nanometers difference. So, you are getting a better technology as you go to a better CMOS or fabrication technology, and the uniformity is also good, and you can have very accurate overlay and costing as well.

But then if you go to immersion lithography, so this is how present-day microprocessors are made and the memories are made, this gives you even better. So, we can make hole sizes that are 50 nanometers, so you can make even finer features that can be really useful for integrated photonic devices. So, the. the better the resolution that you get from the patterning process, the better our optical characteristics and also various devices that you can make. So, with this till now we have seen how you can clean it and how we can pattern a wafer so far.

So, now we have come to a extent that we can transfer our design to a mask and from this mask onto the wafer. So, the next step is to transfer this structures onto the substrate itself. So, our idea is to transfer this onto the Silicon that is underneath, so we want to make some photonic circuits in Silicon let us say as an example is what we are discussing in this series. So how do we etch Silicon, how do we go about in understanding this process which we will see in the next lecture. Thank you very much for listening.