Introductory Neuroscience & Neuro-Instrumentation
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Lecture No. 25
Introduction to Silicon Wafer Processing Techniques

Hi. Welcome to this particular module. In this module, we will look at silicon and silicon dioxide. The reason for understanding silicon, its process from sand to wafer, how, what are the processes, like in one of the modules I told you there are 2 processes, Czochralski technique, and Float Zone technique. So, we will see both FZ, which is Float Zone and CZ which is the Czochralski technique.

And in the following modules, we will see, a process called Photolithography. If you know what kind of substrate is that, substrate, as we discussed earlier, the substrate is a material on which you are going or a base on which you are going to deposit different layers to form a sensor or to form a chip. So, in the case of most of the semiconductor devices, a silicon wafer is a substrate.

So, it is important to understand the silicon wafer to understand the Miller Indices. Miller Indices are useful to understand the orientation, is it 1 0 0, is it 1 1 0, it is 1 1 1. So, we will understand that particular process as well. So, and there are very-very small videos that will help you to understand the process, how it happens in the Fab Lab.

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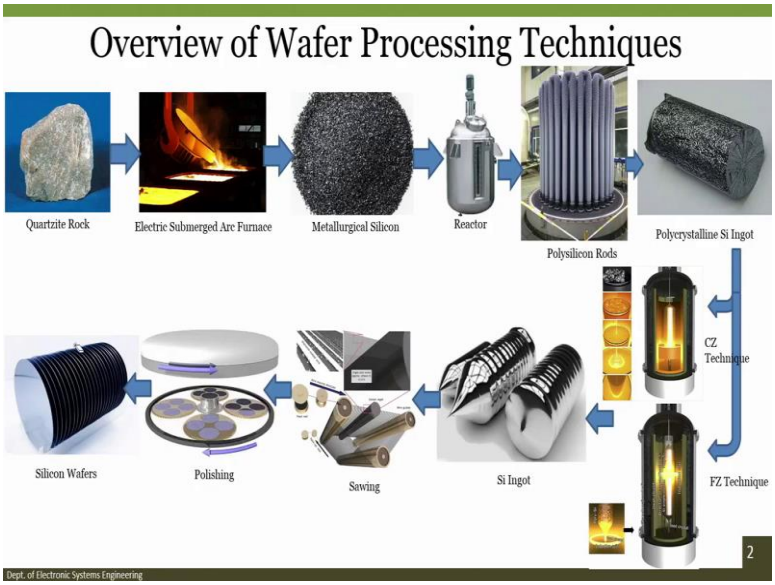

So, let us see the overview of the Wafer Processing technique. It starts from Quartzite Rock. And this rock is further placed in an Electric Submerged Arc Furnace, through that we get a Metallurgical Silicon, which is further reacted to form Polysilicon Rods. And from polysilicon, we form Polycrystalline Silicon Ingot, which is further melted either by CZ technique or by FZ technique. So, you can say CZ or CZ, and FZ or FZ. This further forms a silicon ingot, which is 99.99 99. 9 times 9, 99.9 times 9 pure silicon.

This silicon ingot is then further sliced with the help of a dicing saw, or it, the process is called Sawing. And here, the diamond wires are used to slice the ingot to form individual wafers. These wafers are further lapped and polished to form a silicon wafer that we can use for, or that we can use as a substrate. Again, depending on the size or diameter, the wafer can be of 2 inch, 4 inch, 6 inch, 12 inch, 18 inch and so forth.

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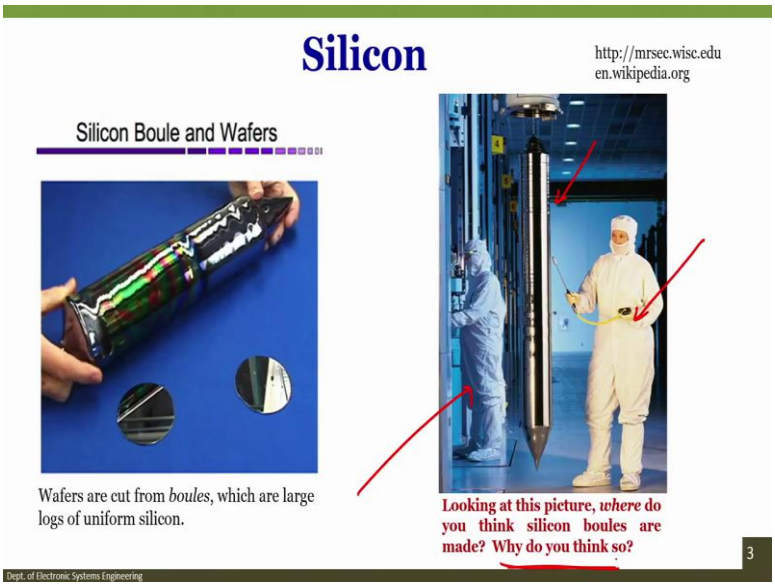

So, if you see silicon generally are wafers that are cut or silicon wafers are cut from the boules, which are large logs of uniform silicon, it is also called silicon ingot. And particularly, when you look at this picture, what exactly it shows? Where do you think the silicon boules or the ingots are made? And if you have correctly guessed, it is a Cleanroom or a fab lab. And we have seen the class of the cleanroom, Class 1, Class 10, Class 100. So, why require, why we require cleanroom? The answer is to remove any contamination.

So, one is that this, the engineer wearing the lab gown, shoe cover, gloves, wear cover, hair cap, glove, and this is a part of the PPEs working inside a cleanroom. And this is the silicon

ingot that you see. And the advantage of working in a cleanroom is to, why do we think so? Because the cleanroom will remove any contamination.

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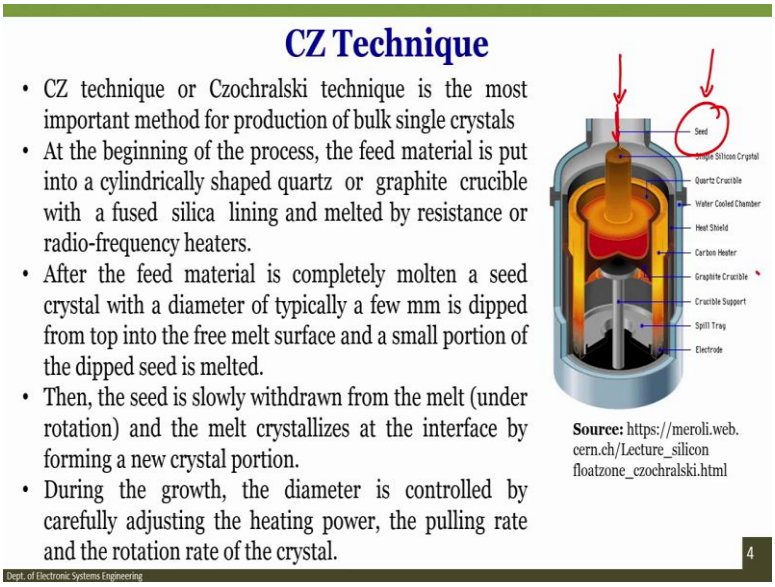

So, let us see the first technique which is called the Czochralski technique or CZ technique. So, CZ technique or Czochralski technique is the most famous important method for the production of bulk single crystals. And at the beginning of the process, the feed material is put or placed inside cylindrical-shaped quartz.

So, let us see this particular image, and you will, we will see one by one. You can see this one, just let us start from the bottom, there are Electrodes one and here. And these electrodes are heated at a high temperature. Then there is a Spill Tray, there is a Support for Crucible then we have a Graphite Crucible, this is a graphite crucible and this is like a cross-sectional image, so we can understand. You have a Carbon Heater. Then the outer surface of the furnace would not be at high temperature, so you have a Heat Shield.

You have Water Cooled Chamber to further cool this outer surface of the furnace. Then you have Quartz Crucible, you have a single crystal and you have seed crystal. So initially, this seed crystal is placed inside this particular molten silicon, molten polycrystalline silicon. And this seed crystal is rotated in let us say clockwise direction or let us say anti-clockwise direction, then this crucible is rotated in the clockwise direction, it is opposite. And the seed crystal is slowly pulled out of this molten silicon, so to form this ingot. This is the technique which is called the CZ technique.

Let us see further that at the beginning of the process of the feed material is kept in a cylindrical shaped quad or graphite crucible. Why quads or graphite? Because it can resist extremely high temperature with a fused silica lining and melted by resistance or radiofrequency heaters. Here, the image shows a carbon heater, so it is a resistance heater.

Now, the simple thing is when you want to heat a material, what you require is resistance. And how you define resistance? Resistance is defined as

$R = \rho L/A$, where ρ is your resistivity, L is the length and A is the area. So, if I apply a high voltage and the resistance is low, what will happen? Extremely high current will flow. If an extremely high current flows from the resistor then there is a generation of Joule's Heating, which is also called I^2R heating, resistance heating.

Where in the case of a radiofrequency heater, a radio frequency is applied to the material so that the heat is generated at the surface of the heaters. So, after the feed material is completely molten, which is this material, this is called seed material, it is called feed material, feed, because it is feeding to the seed material or feeding to the seed. So, this is the polycrystalline material which is melted inside the furnace.

And then a seed cell with a diameter typically of a few millimetres is dipped from the top, this is the seed crystal, it is dipped from the top into the molten free metal surface, and a small portion of that deep seed is melted. So, this is a rod and a small portion is melted. And then the seed is slowly pulled out or withdrawn, and the melt crystallizes at the interface by forming a new crystal portion. During the growth, the diameter is controlled by carefully adjusting the heating power, pulling rate, and rotation rate of the crystal.

So, let us take an example. If you see my hand here, if you see the hand, what I will show to you is that I am, let us say this is a seed crystal and this is a rod, so you understand that the seed crystal is placed inside this rod like this. And the whole thing is molten, this whole thing is crystalline polysilicon, which is in a molten state. Now, this seed crystal is placed inside this particular crucible and only the tip is melted. Now, what will happen? This will rotate in this direction; the seed will rotate in opposite direction. So, this is like this, the seed is opposite in this direction like this.

What will happen is depending on the pulling rate, depending on the power that is applied to the crucible, and the rotation of the crystal, how fast the rotation is, if the rotation is fast the diameter is small. If the rotation is low, the pulling rate is low, the diameter is more. So, this

is at a cold temperature compared to the molten material within this particular furnace. So, the slowly you pull out the seed crystal, you have a larger diameter. The rotation rate is lower, you have a larger diameter. Rotation is faster, faster is the pulling, diameter is low. Thus, we can change the diameter of the ingot by adjusting these 3 rates, pulling rate, rotational rate, and the power applied to the furnace, 3 things you have to understand.

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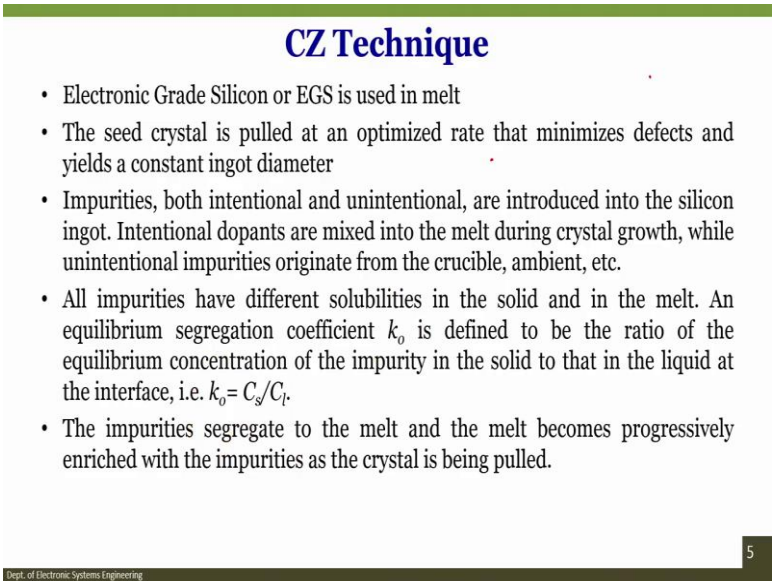

So, if you go for CZ technique, then you have Electrode Grade or Electronic Grade Silicon, it is also called EGS, which is used in the melt. The seed crystal is pulled at an optimized rate depending on what diameter we want that minimizes the defect. Now, this is also very important that if you are pulling it very high rate then the defects can be higher. And also, you should understand that the rate of pulling should be optimized, so that we can have a constant diameter. The diameter of what? The diameter of the ingot.

The ingot is nothing but a cylindrical rod of silicon, like this tip. So, impurities, both intentional and unintentional are introduced into silicon ingot. For example, if there is no impurity in the silicon wafer, I am just drawing cross-section, see silicon wafer generally looks like this, if I take a cross-section, it looks like this. So generally, when somebody asks you, “How to draw a cross-section of silicon?” Just draw a rectangle. This is silicon.

Now, this silicon without any dopant is Intrinsic. So, when you add the dopants intentionally, it becomes Extrinsic. So, either intentionally or unintentionally the dopants are introduced into silicon. Intentional dopants are mixed into the melt during crystal growth, while unintentional impurities originate from the crucible, ambient, etc. All impurities having

different solubilities in the solid and in the melt. An equilibrium segregation coefficient defined by ko is the ratio of the equilibrium concentration of the impurity in solid to that of liquid.

So, this is the equilibrium segregation ratio. And it is nothing but what is the concentration of the impurities in solid divided by what is the concentration of impurity in liquid. The impurities segregate to the melt and the melt becomes progressively enriched with the impurities as the crystal is being pulled. So, let us see a very small video of about 1 minute 30 seconds to see how this CZ technique works. Let me play the video.

Video: Let us start with the Czochralski method as developed by the Polish scientist, Jan Czochralski in 1980. It is a method to grow single-crystal silicon. In this method, highly purified silicon is melted in a crucible at typical temperatures of 1500 degrees Celsius. Intentionally, boron or phosphorus can be added to make p-doped or n-doped silicon respectively. The seed crystal that is mounted on a rotating shaft is dipped into the molten silicon. The orientation of the seed crystal is well defined, it is either a 1 0 0 orientation or in 1 1 1 orientation. The melt solidifies at the seed crystal and adopts the orientation of the crystal.

Crystal is rotating and pulled upwards, allowing the formation of a large single crystal cylindrical column from the melt. This big single crystalline silicon block is called an ingot. In this process, the temperature gradients, rate of boiling up, and speed of rotations are precisely controlled. This process is further developed through years of advances. And nowadays, crystal ingots of diameters of 200 millimeters and 300 millimeters, where lengths of 2 meters can be processed. To prevent the incorporation of impurities, this process takes place in an inert atmosphere like argon gas.

The crucible is made from quartz, which finally dissolves in the melt as well. Consequently, Czochralski Mono Crystalline Silicon has relatively high oxygen.

Professor: So, what you see in that one is that how the CZ technique works and how the ingot is produced. Now, let us see the next technique, which is our FZ technique or float zone technique.

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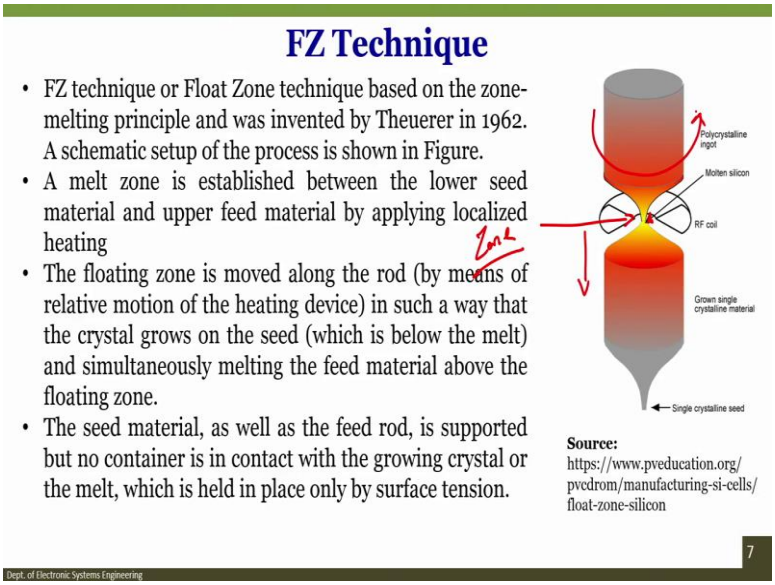

So, float zone technique, as the name suggests float zone, so F and zone Z, so it is called FZ, float zone technique based on the zone melting principle was invented by Theuerer in 1962. Of course, the way we pronounce the name would be different than how it should be pronounced, so do not worry about it. A schematic setup of the process is shown in the figure. This is how the schematic process is there.

And you can see here, is a single crystal seed. And there is a grown silicon crystal material, there is an RF Coil here. And there is a polysilicon ingot that is produced or there is a polycrystalline ingot, I am, which is in the molten state because of the hitting. And the single crystal is grown at the bottom. So, let us understand how this works. You can see here; a melt zone is established between lower seed material and upper feed material. So, in this case, this is the feed material and this is the seed material.

So initially, you do not have this thing, only the seed is there. So, it will look like this, and you only have a seed material. This is your seed, this is the feed material, and this is the molten zone. So initially, seed material is just a (sili) our rod, seed rod. And slowly, when you molt it, and this, and the seed is pulled down, there is a growth of the single crystalline silicon. So, let us further understand that a melted zone is established between the lower seed and upper seed by applying localized heating.

This is applying localized heating, which is shown here. Either it is using an RF coil or using the resistor type of heating. The floating zone is moved along the rod using the relative motion of the heating device in such a way that the crystal grows on the seed. So, this is

rotated such that the crystal starts growing on this seed material by simultaneously melting the feed material above the floating zone. So, this is the zone, which we call a floating zone or float zone.

The seed material, as well as the feed rod, is supported by, no container is supported, but no container is in contact with the growing crystal or the melt, which is held in place only by surface tension. These are supported by there is no container that is in contact.

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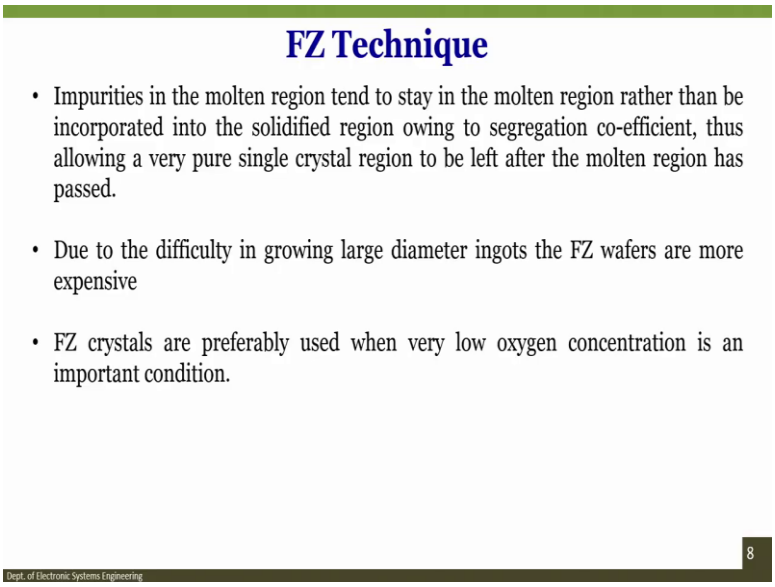

So, impurities in the, in this case, there is an impurity in the molten region, tend to stay in the molten region rather than incorporated into the solidified region, owing to segregation coefficient, thus allowing a pure single crystal region to left after molten region passed. You see, the impurities, in this case, stays only in this region, so when you grow the single crystal using the FZ technique, the crystal is more pure compared to the CZ technique.

Another is that because of the way the crystal is grown, it is difficult to grow larger diameter ingots using an FZ wafer. And that is why the, or FZ technique and that is why the FZ wafers or wafers grown using FZ techniques are more expensive. However, we get a very pure single crystal region. So, FZ crystals are preferably used when very low oxygen concentration is an important condition. Let us see, again I will show a small video on the FZ technique.

Video: The source material is a polycrystalline rod as processed in the earlier mentioned Siemens process. The end of the rod is heated up and melted using a radio frequency heating code. The melted part is put in contact with seed crystals. Here, it solidifies again and adopts

the orientation of the seed crystal. Again, both 1 0 0 and 1 1 1 orientations are being used. As the molten zone is moved along the polysilicon rod, the single crystal ingot is growing as well. Many impurities remain in and move along with the molten zone. During the process nowadays, intentionally, nitrogen is added which improves the control on micro defects and improves the mechanical strength of the wafers.

The advantage of the float zone technique is that the molten silicon is not in contact with other materials like quartz as in the Czochralski method. In the float zone process, the molten silicon is only in contact with the inert gas like argon. The silicon can be doped by adding doping gases like diborane and phosphine to the inert gas to get p-doped and n-doped silicon respectively. The diameter of floats on ingot is generally not larger than 150 millimeters, as the size is limited by the surface tensions during the growth.

Professor: So, what we understood that there are 2 techniques, the CZ technique, the FZ technique, the advantage of the FZ technique, we can dope impurities in the CZ technique. Here, we can have a better crystal in FZ technique, pure crystal, but the diameter is lower in FZ technique, wherein this case, which is CZ technique, you have a larger diameter, thus the cost can cut down because larger diameter wafers can be produced in FZ technique, the cost is higher because the diameter of the wafers is smaller. And particularly, when you want to use very low oxygen concentration is required, then FZ techniques are generally preferable.

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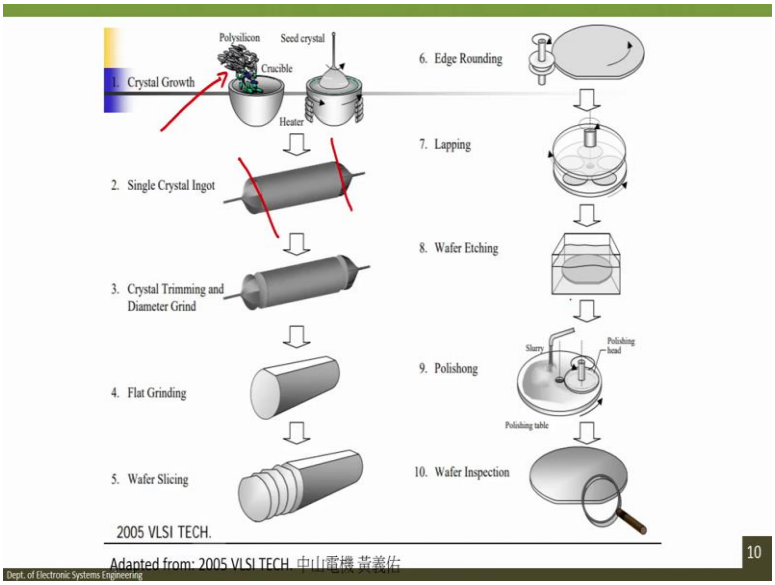

Now, let us see, a pictorial representation of the same, which is your CZ technique. And like we said, there is polysilicon which is added into the crucible, the crucible is, the polysilicon is

melted by hitting the crucible. Once you insert the seed crystal and you pull it at an optimum rate, at an optimum speed along with the rotation, then you get a single crystal ingot.

Now, this side of the ingot is sliced by Crystal Trimming and Diameter Grind. Then you have a Flat Grinding. We have discussed the importance of flat grinding for understanding the crystal orientation. Then we have Wafer Slicing. After wafer slicing, the next step would be Edge Rounding, then Lapping, Wafer Etching, Polishing, and Wafer Inspection.

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So, when the ingot is sliced, first these edges are removed, then you have something like this. And then this silicon ingot is sliced further with help of the Diamond Wire. And you can here, see, the wire guides are there, this will slice the silicon into wafers. So, this is a diamond-coated wire. And ingot and wires approximately, scale, drawn to the scale, so you can see here how these slices are happening. Once you have the wafer, you can use the lapping machine, which is shown here. If you go to this particular website, which is MicroChemicals.eu , you will understand the entire process in detail provided over there.

So, here let us see how the wire direction is there, and as you see one is from the top, another is from the bottom and this is how the ingot is sliced. I will play the video, and then we move to the next slide.

Video: The disadvantage of the sawing step is that we waste a significant fraction of the silicon as a curve loss. The curve loss is usually determined by the thickness of the wire or saw used for sawing, and is in the order of 100 microns of silicon. This is a large fraction of the ingot if you consider the typical crystalline silicon wafers used in solar cells nowadays are

in the order of 150 up to 200 microns. Sawing will logically damage the surface of the wafers, so this processing step is followed by a polishing step.

So, the question now comes is, “Why we had to use silicon? Why not germanium? Why not gallium nitride? Why not some other substrate? Why not sapphire?” So, the answer is that crystalline silicon is a hard and brittle material that deforms elastically until it reaches its yield strength. And that is why we also know the properties of semiconductor material, particularly silicon in detail. So, we can adjust those properties by adding impurities and creating different processes.

The technology developed to fabricate chips using silicon is well established. Of course, we want to improve the performance of the device and that is why new substrates are being explored, and at some point, or due to a smaller extent also, commercial devices using other substrates are available. However, 90 percent of the wafers or chips that are produced till now are based on silicon.

So, if you see the tensile strength of silicon is close to 7 Giga Pascal, Young's modulus, it is near to stainless steel, mechanical properties are uniform, good thermal conductor and finally, mechanical integrity up to 500 degrees centigrade.

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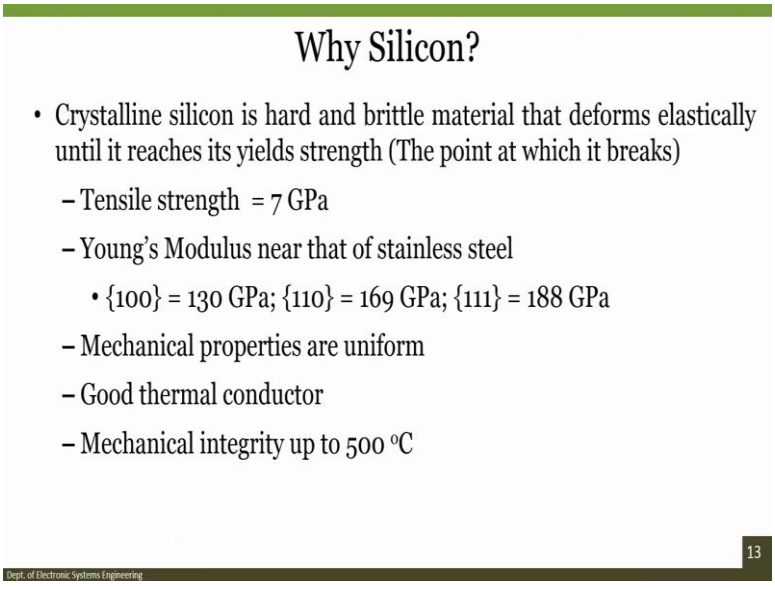

So, if you see the slide, the same thing that I told you is shown in the slide.

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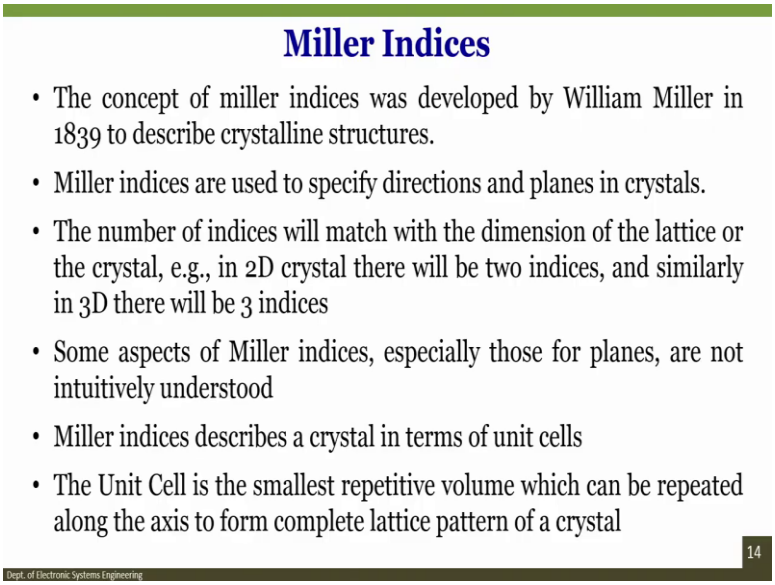

Now, what is Miller Indices? The concept of indices was developed by William Miller in 1839 to describe crystalline structures. So, they are used for specific directions and planes in their crystals. And generally, the number of indices will match the dimension of the lattice or crystal. For example, in 2D crystal, there will be 2 indices, similarly 3D crystal, 3 indices. Some of the aspects of Miller indices, especially, those for planes are not intuitively understood yet, however describes a crystal in terms of unit cells. And unit cells are the smallest representative volume, which can be repeated along the axis.

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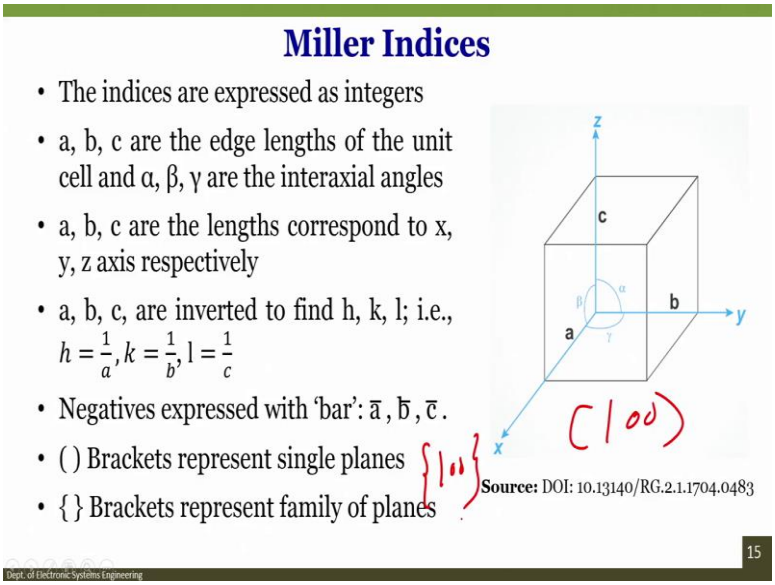

You will see these Miller indices in this example, where there are indices expressed as integers. If you understand a, b and c are edge lengths, a, b and c are the edge lengths, while

alpha, beta, and gamma are the interaxial angles. You can see, alpha is there, beta and gamma, this also in the interaxial angles. a, b and c are the lengths correspond to x y, and z, which is obvious. And here, a b and c are inverted to find h, k, l, which is

h =1/a,

k=1/b,

and l = 1/ c.

That negative expression bar that is $\bar{a}$, $\bar{b}$ and $\bar{c}$ are expressed, so, and generally when you write the Miller indices, then if I write to (1 0 0) like this or let me just write down 1 0 0, that means it shows the planes. But if I write the {1 0 0} like this in the curly brackets that represent the family of planes, so that is the difference between the way you draw the brackets.

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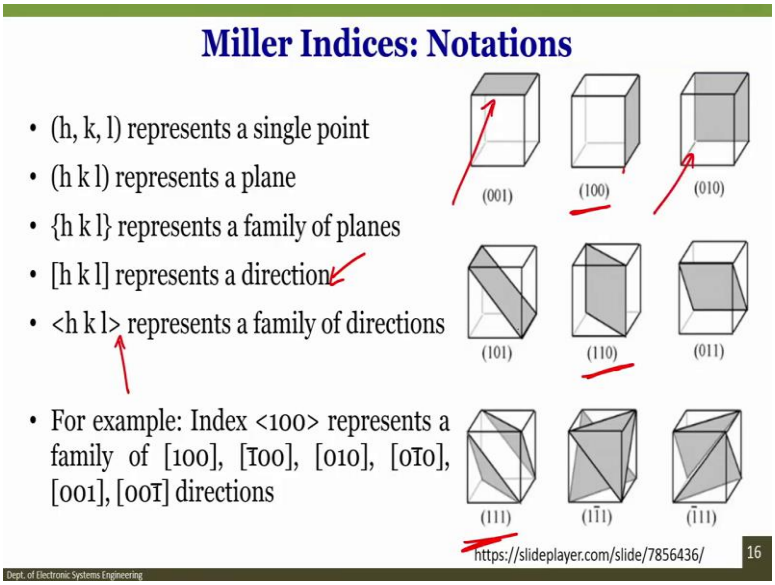

So, here you can easily understand that (h, k, l) if you write down like this represents a single point, while if you write (h k l) without any comma in between with this bracket, then it represents a plane, if you write with curly brackets then it represents a family of planes, if you write with this kind of notation, it represents a direction, and then finally, if you write in this manner, then it represents a family of directions.

So generally, as I said, we have 1 0 0 planes, we have 1 1 0 planes and we have 1 1 1 plane. But if you represent let us say, in another form then you can also say that if I consider this particular plane, it will be 0 0 1, but if I consider this one it will be 1 0 0, in this way, it will

be 0 1 0, so on and so forth, it is very easy to understand. So, example is index 1 0 0 represents a family of 1 0 0 1 bar 0 0 0 1 0 0 1 bar 0 0 0 1 and 0 0 1 bar directions.

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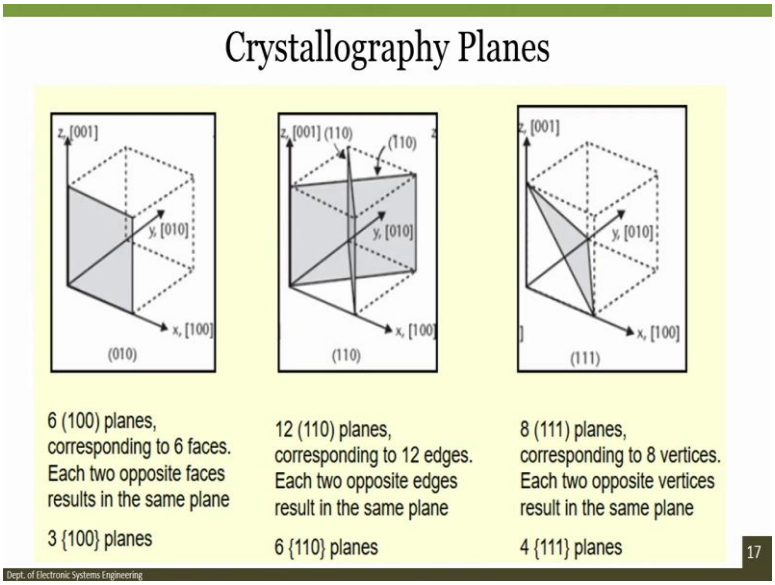

Further, we understand about crystallographic planes, and you can see that there are 6, 1 0 0 planes correspond to 6 faces, there can be 12, 1 0 0 planes corresponding 12 edges, then there can be 8 1 1 planes corresponding to 8 vertices. Each 2 opposite vertices results in the same plane. It is important to understand crystallographic planes, but for us, we will not stretch more on how these planes are useful.

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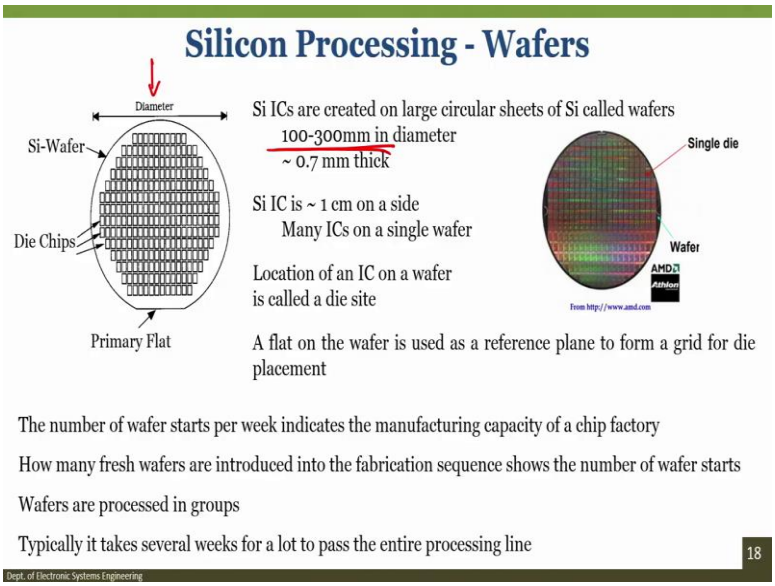

Whether then we will see that was kind of wafer we can use, so to fabricate different devices. So, in the case of silicon processing of wafers, you can see here that the diameter of the wafer is this diameter, generally as shown here. And within this silicon wafer, generally what we prefer is, if it is a 4 inch wafer, then if you draw a (rectang) square within this 4 inch wafer,

this is the area that you should use for device fabrication, this is the area that you use for device fabrication. So, it is kind of like this. And the devices that are made within this silicon wafer are called chips. As I told you earlier also that based on the orientation of the secondary flat concerning the primary flat, we can have 1 0 0, 1 1 0, 1 1 1 plane.

And generally, since this is some little bit old literature, it says that 100 to 300 millimeter in diameter, but now we also have wafers which are of larger diameter. Silicon IC is generally one centimetre on side, many ICs on a single wafer, you can design. And how a company manufacturing capacity can be defined? It depends on number of wafers that starts per week, how many number of wafers are used at the starting of a week is, indicates the manufacturing capacity.

However, how many fresh wafers are introduced into fabrication sequence shows the number of wafers that starts. One is how number, how many numbers of wafers are used at the starting, second is how many numbers of wafers are introduced in the fabrication sequence is the number of wafer starts. Finally, wafers are processed in groups, not single wafers are done. 25 wafers at a time, it is cleaned, then silicon dioxide is grown and further processes are done. And typically, it takes several weeks for a lot to finish up the entire process line. But because a lot of wafers are simultaneously processed and the diameter of the wafer is large, the cost of the device is low.

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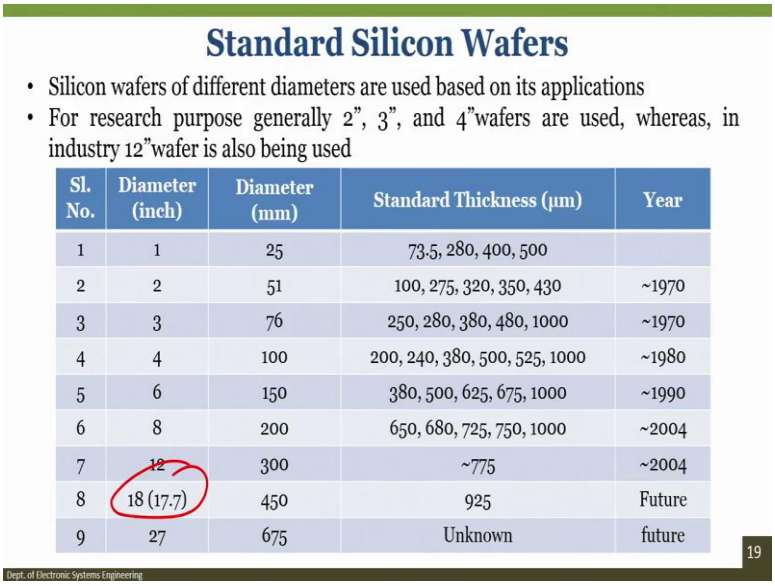

So, if you see a standard silicon wafer, we have right from 1 inch to 18 inch. And right now, we are close to this, we use 18 inch, so other than future, we can say it is kind of present, while 27 inch is still in not commercially used extensively.

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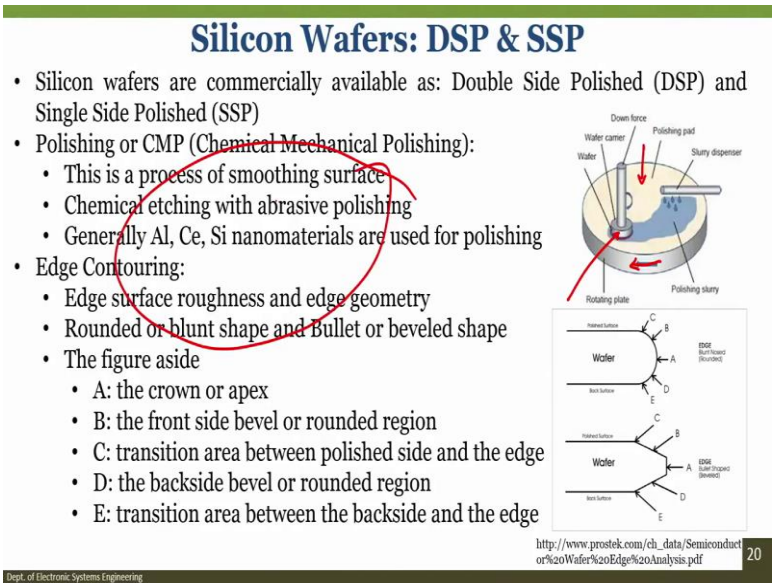

Now, another point is we require a polished wafer. What is polished wafer? The wafer is smooth in the surface. Now, what do you mean by smooth in the surface? Smooth surface is the surface roughness should be less than few nanometres or less than 2, 3 nanometres. So, silicon wafer, generally, if you see, I will show it to you, are either single side polished wafers or are double cell polished wafers, that means 1 side of the wafer is polished, the second side of the four is not polished, it is called Single Side Wafer, Single Side Polished Wafer. In another case, your both side of the wafer is polished, that is called Double Side Polished Wafer.

Single side polished wafer are generally cheaper compared to double side polished wafer, in fact not, it is cheaper. While the advantage of double-side polished wafer, we will see when we will discuss photolithography. So, polishing of the wafers can be done using a process called Chemical Mechanical Polishing, where there is a process of smoothing the surface, chemical abrasive polishing is done and generally aluminum see silicone nanomaterials are used for polishing, while we also had to understand about the edge countering, and if you see the slide, you can see that the edge surface roughness and edge geometry rounded or blunt shape and bullet shape or bevelled shape, like you can see here, this we have to correct.

And here you can see that the A represents the symbol, A here represents the Crown or Apex, B is the front side of the bevel, C is transition area between polished and edge, D is the backside of the rounded region, E is a transition area between backside and the edge. So, you can see here, a process, which is, the wafer is mounted on the (rotat) rotational axis on a holder, on which wafer is mounted. Then the slurry is dispensed using slurry dispenser. There is a wafer, what we called, there is a downforce of this particular wafer carrier. And these different carrier moves on this particular pad. And during this, the pad has roughness, which further polishes the wafer depending on the amount of polishing and rotation, the surface would be smoother.

So, the more the polishing, the more smooth the wafer would be. But also understand that more you do polishing; the size of the wafer would also reduce. I, when I mean by size is the thickness of the wafer. So, the wafer is mounted, as you can see on this wafer holder. And this is like I say rotational setup, which rotates in let us say clockwise direction, and you have this pad, which is shown in yellow colour and then there is a chemical. These chemicals are silicon nanomaterials, aluminium or Ce.

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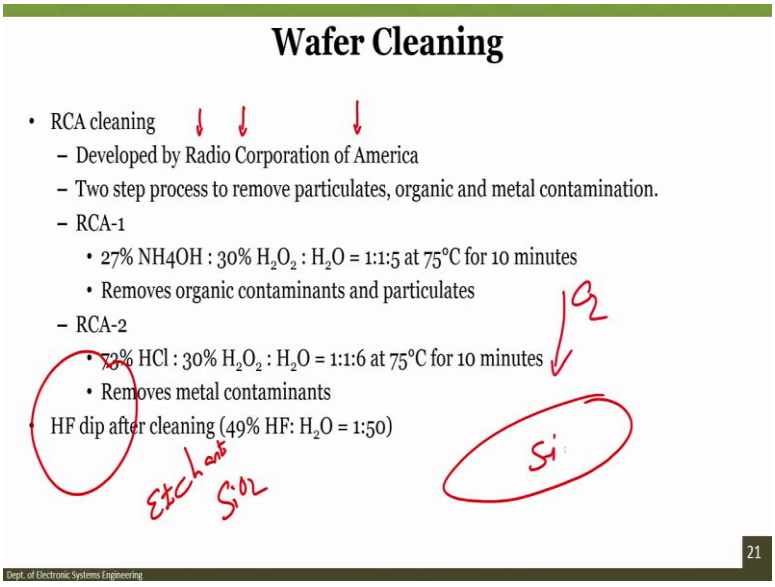

Now, once you have the wafer, what you will do? Before starting any process, it is mandatory to do or perform the wafer cleaning step. And generally, refer cleaning steps are divided into 2 steps. One is called RCA-1 and the second is called RCA-2. So, , this was developed by Radio Corporation of America, and that is why the name is RCA, R for Radio, C for Corporation, A for America, so RCA-1, and RCA-1 and RCA-2. So, in RCA-1, what we do is we use 24, 27 percent NH4OH mixed with 30 percent H2O2 mixed with water in this ratio 1

is to 1:5 at 75 degrees for 10 minutes. We dip the wafer, this will help to remove the contaminants and the particulates, while RCA-2 consists of 73 percent HCl is to 30percent H2O2 is to H2O in the ratio of 1 is to 1: 6, again at 75 degrees and dip it for 10 minutes.

So, we take this chemical, we dip the wafer inside the chemical, and it will help to remove the metal contaminants. So, to remove the organic contaminants and metal contaminants, RCA cleanings are used. And finally, after you do that you have to dip the refer in HF dip. And HF dip is 49 percent HF is to H2O, which is in ratio 1 is to 50. HF deep is used to remove any silicon dioxide present on the surface of the wafers. What happens is, silicon wafer is there and because there is oxygen in the environment, it forms a thin layer of silicon dioxide.

This silicon dioxide we do not want. And that is why to remove the silicon dioxide, if we dip the effort in HF, silicon dioxide gets etched because HF is the etchant for silicon dioxide. HF is the etchant for silicon dioxide. How silicon dioxide is grown? On a silicon wafer when oxygen reacts, then it forms silicon dioxide. We will see in the few slides from now, how the silicon dioxide processes is done. Before that, let us see the importance of silicon and how it is used to fabricate the chips. I will play the video.

Video: You may not realize it, but we are surrounded by arguably the greatest most revolutionary invention of the last 50 years. It is on TVs, stereos, watches, cars, phones, traffic lights, and pretty much every appliance in your kitchen. These days if a device uses electricity, it probably uses one. The tiny gizmo in question is, of course, the Silicon Chip. In this strange futuristic-looking plan, they produce silicon wafers, which are the basis for all modern microchips. Silicon has special properties because it is what is called a semiconductor.

That means that depending on how its treated silicon can either conduct or block the flow of electricity. It is this property that makes it ideal for supporting the millions of tiny transistors necessary for a modern computer chip. But because these transistors are so incredibly small, the silicon base on which they rest needs to be flawless. It took decades to perfect the process of producing silicon with a perfect monocrystalline structure. They begin with raw polysilicon or poly and are heated to over 2500 degrees Fahrenheit inside a special sealed furnace, which has been purged with argon gas to eliminate any air.

The resulting lake of molten silicon is then spun in a crucible and a silicon seed crystal, roughly the size and shape of a pencil is lowered into it while spinning in the opposite direction. As the molten polysilicon is allowed to cool, the seed crystal is slowly withdrawn at around 1 and a half millimetres a minute. The result is a single silicon crystal weighing around 440 pounds and with a diameter of around 200 millimetres. The Crystal is so strong, its entire weight can be supported by a single thread just 3 millimetres across. But it is brittle and it must now be cut down to size without shattering.

After testing with chemicals and X-rays to check its purity and molecular orientation, it is fed to a silicon salami slicer. This 10 ton wire saw uses a fast-moving web of ultra-thin wire to produce wafers of silicon that are just two-thirds of a millimeter thick and 99.999 percent pure. Once caught, there are microscopic marks left on the wafer surface. So, it is time for a buffing using a process called lapping. After a twirl in this high-powered polisher, they are still not smooth enough. So, they are given yet another buff using a chemical process. The result is wafers of silicon with a surface roughness of less than 1 millionth of a millimeter. Buffed to a sheen, they are finally ready for etching with this circuit design.

Coming up, how do they eliminate the biggest enemy of manufacturing in a microscopic environment, the common dust particle? Find out next on “How Do They Do It.” Packing millions of transistors onto these tiny silicon wafers is the job of chip manufacturers like Texas Instruments. Back in 1958, the inventor of the integrated circuit, Jack Kilby managed to squeeze a single transistor onto his design. These days, the latest generation uses almost a billion. And according to Moore's law that number doubles every 2 years. Of course, the more they try and pack into the design, the smaller each transistor needs to get.

There are over a quarter billion transistors in this design, someone has to shrink them down to this. Working at this microscopic scale exposes the chip makers to a major problem. When a transistor is only 110 thousandth of a millimetre across, the smallest particle of dust is enough to cause an electronic train wreck. So, before staff members like Dane Bailey set to work in the fab, it is on with the bunny suit. For our general product that we make here, a DSP typically takes on the order of about 1500 individual processing steps from start to finish. With an area of just under 194000 square feet, the fab is a class 1 cleanroom.

Thanks to 12000 tons of air conditioning equipment, the air is 1000 times cleaner than a hospital operating room. There is less than 100 particles per cubic foot of air is fused one particle landing on a critical area can kill a chip. To give you an idea of how clean this room

is, walking alone produces 5 million particles every minute. So, to avoid contamination from the inadvertently dusty staff, front opening unified pods or transport packets of wafers through the intricate process of component construction. The key problem is miniaturizing the complex designs and imprinting them onto the wafers. It is done through a process known as photolithography.

First, the wafer is coated with photosensitive chemicals that harden when exposed to UV light. In sealed dark rooms, light is shown through an image of the design, then through a miniaturizing lens and onto the coated wafer. When the chemical is washed off, the design remains just like a developed photographic image. But to pack all the components onto the wafer, they are built up layer by layers like floors and a miniature skyscraper. To complete the job, the cycle the wafers up to 40 times repeating the photo etching process for each new layer. Some layers are cooked, some blasted with ionized plasma, some bathed in metals.

Each different type of treatment changes the properties for that layer and slowly forms part of the jigsaw making up the chip's design. The finished sheets of silicon wafer carry up to 1000 individual microchips and billions and billions of circuit elements. All that remains is to slice and dice and the journey from sand to the circuit board is complete. What was once a worthless pile of sand can now change hands for more than nearly 700 dollars an ounce and calculate pi to 1000 decimal places in the blink of an eye. Metaphysical poet William Blake reckoned he could see the world in a grain of sand. But if he were to look again today, he would surely be more amazed to discover a billion tiny transistors.

Professor: So, what you have seen here is how silicon is used in IC industry. So, we will stop the module here, and we will continue in the next class Silicon Dioxide and the process regarding the same. And I will show it you, how the silicon wafer looks like. I will bring silicon wafers with me, one which is a single side polished wafer without any silicon dioxide and the second one with silicon dioxide grown on the silicon wafer, and then you, so then you understand that what is the importance of the silicon dioxide and how it looks when you grow silicon dioxide.

Depending on the thickness of silicon dioxide, the colour of the silicon wafer would change. Silicon dioxide, again understand, it is an insulating material or in other terms, it is also called as a glass. So, look at this video, like I said, this model is more like the informative module to (underst), to make you understand how the silicon is fabricated from polygons

lines, polygons line chunks, using 2 different techniques, and how, what is the importance of silicon in IC industry.

After we learn silicon dioxide in the next module, we will take lithography, so you understand it, how to devise or fabricate an end design sensor or chip that can be used for EEG application or we can use for ECOG application. Both are related to your neuroscience topic, EEG Electroencephalogram; ECOG, electrocorticography. And we will see both these chips in detail and how can we fabricate those. So, till then you take care, and I will see you in the next class.