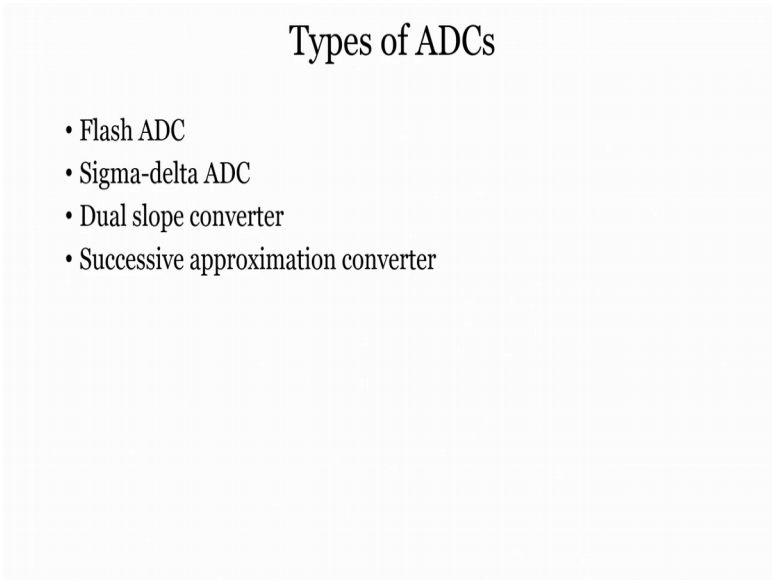
Electronic Systems for Cancer Diagnosis
Dr. Hardik J. Pandya
Department of Electronic Systems Engineering
Indian Institute Science, Bangalore

Lecture – 34
Electronic Systems for Cancer Diagnosis

Hi, welcome to this module and in this module we will look at analog to digital converters. So, what are types of ADCs and how does it function ok? So, there are 4 basic types of ADCs that we look at the first for is called flash ADC, then we will talk about sigma delta followed by a dual slope followed by successive approximation.

(Refer Slide Time: 00:47)



(Refer Slide Time: 00:53)

Flash ADC

- The flash method utilizes comparators that compare reference voltage with the analog input voltage. When the input voltage exceeds the reference voltage, a HIGH is generated. A comparator is not needed for all 0's condition. In general a 2^n-1 comparators are required for converting to an n-bit binary code. The number of bits in an ADC is its resolution

Advantage:

- Provides a fast conversion times because of a high throughput measured in sps (samples per second).

Disadvantage:

- Large number of comparators necessary for a reasonable –sized binary number

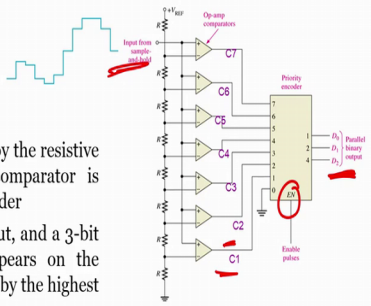
So, let us see flash ADCs: the flash ADC or the flash method use utilizes comparators that compare reference voltages with the analog input voltage, when the input voltage exceeds the reference voltage a HIGH is generated. Comparator is not needed for all o's condition. We will see in the next slide how the circuit looks like? In general a 2 raise to n minus 1 comparators are required for converting an n bit code.

The advantage here is that it provides a fast conversion time because of high throughput and this advantage is large number of competitors are necessary for a reasonable size binary number.

(Refer Slide Time: 01:27)

Flash ADC

- The flash method utilizes comparators that compare reference voltages with the analog input voltage. When the input voltage exceeds the reference voltage for a given comparator, a HIGH is generated



- The reference voltage for each comparator is set by the resistive voltage-divider circuit. The output of each comparator is connected to an input of the 8-input priority encoder
- The encoder is enabled by a pulse on the EN input, and a 3-bit code representing the value of the input appears on the encoder's outputs. The binary code is determined by the highest order input having a HIGH level
- Assume the step size of 1 V. The voltage divider sets up reference levels for each comparator so that there are 3 levels corresponding to 1V, 2V, 3V, 4V, 5V, 6V and 7V. The analog input is connected to other input of each comparator
- With analog input <1V, all the seven comparator outputs will be LOW. Suppose the analog input is between 2V and 3V, outputs C1 and C2 will be HIGH. The priority encoder will respond to HIGH on C2, and will produce a binary output of 010

For example if you see the circuit you can very easily see how many comparators are required for 8 bit converter like C1, C2, C3, C4, C5, C6, C7 7 comparators right. So, it is it this is how it actually works, so you have a reference voltage you have an input from sample and hold circuit and depending on the reference voltage and input voltage. If the reference voltage is higher than input voltage, then you have 0 at the output, if the input voltage is higher than reference voltage you have one output and that goes to the primary priority encoder and that is finally, converted to your parallel binary output right.

So, there are enabling pulse is to the encoder there are op amp comparators and there are input from sample and hold let us see here. So, the flash method utilizes comparator that compare reference voltages with analog input voltage like we discussed, when the input voltage exceeds the reference voltage for a given comparator a high is generated right. So, input voltage because it is connected to the non inverting terminal so high will be generated or one will be generated, the reference voltage for each comparator is set by the resistive voltage divider circuit you can see here the reference voltage.

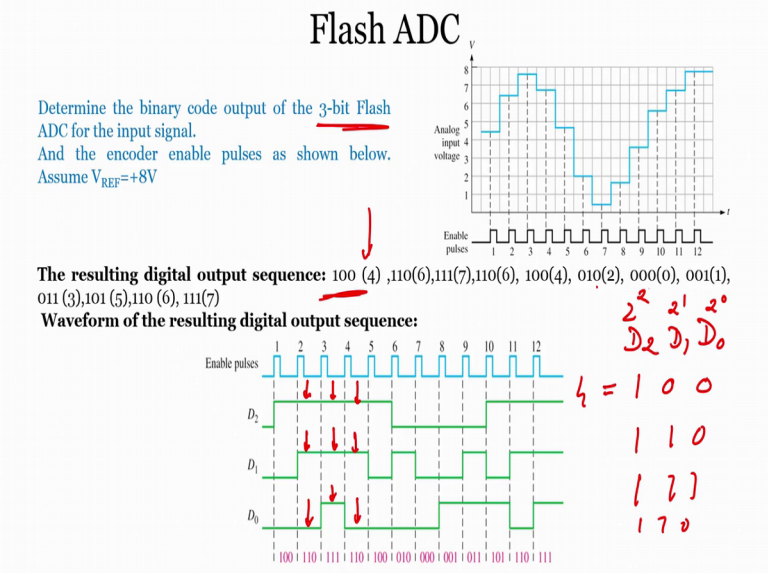
So, this is nothing, but a resistor R1 and R2 and if we apply voltage the voltage dividers circuit. So, same way you keep on dividing the voltage until the here and that is how the reference voltages are set. The output of the comparator is connected to an input of 8 bit primary encoder this is a primary encoder which is 8 bit or 8 input primary encoder. The encoder enabled by a pulse is enabled by a pulse and a 3 bit code representing the value of input appears on the encoders output here is the output that is appearing at the encoders pinned 1 2 and 4.

The binary code is determined by highest order input having a high level. Now assume that the style is step size of 1 volts, the voltage divider sets of a reference levels from each comparator. So, that there are three levels corresponding to 1, 2, 3, 4,5, 6 and 7, then analog input is connected to other input of each comparator now we understand this question.

So, with analog input less than 1 volt all 7 competitors will be low he what we are saying is if you have a step size of 1 volt and a voltage divider is set for all comparators. So, it is 1, 2, 3, 4 up until 7, then what will happen if the analog value that is the value from the signal is less than 1 volt what will happen all the comparators would be low right. So, output will be 0, suppose the analog input is between 2 and 3 then comparator C1 and C2

right will be high and the quadratic and corner will response to high of C2 and produce binary of 0 1 0.

(Refer Slide Time: 04:19)

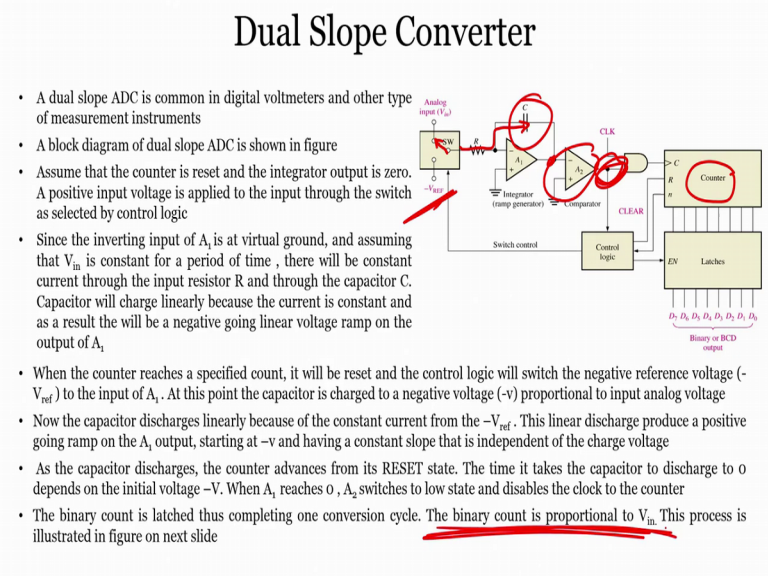


So, this is how the comparator works, this is out in general they are flash ADC will operate and if you want to determine the binary code output of 3 bit flash ADC and the encoder enable pulses are as shown below then assume we reference what is equals to 8 once. If you have this particular signal right you can see here as an analog signal and there is enable pulses. So, suppose you are asked that the resulting digital output sequence is 100, 110, 111, 110, 100, 010, 000, 001 and so on until here.

Waveform of the resulting these are output sequence droid so it's very easy, if you really see you had to draw pulses and for each pulse you have to show a particular signal for the first pulse what is it 100. So, if you have here 3 bit per if flash right so you have D 2 D 1 D 0. So 100 is given by D 2 D 1 and D 0 so 100 right, 2 raise to 0, 2 raise to 1, 2 raise to 2, so 100 will give us 4 right that is here.

Now we have second pulse so when you have first pulse only D 2 should be 1 D 2 should be 0, second pulse is; 110; that means D 2 and D 1should be on which is right over here and here and it D 0should be 0 third pulse 111. So, all three signals 111 should be high, 4 pulses 110. So, it will be 1 here 1 here and 0 here, it's very easy to draw very easy to draw the waveforms of the resulting digital output sequence.

(Refer Slide Time: 05:57)



Now, if this is the flash DAC, but if you if flash ADC, but if you want to understand the another kind of ADC which is a dual slope ADC let us see how it works. So, a dual slope ADC is a common in digital voltmeters and other type of measurement instruments, a block diagram of dual slope ADC is shown right over here. Where it consists of the analog input signal there is a switch, there is a integrator we are ram generator and there is a comparator with a control logic there is a switch which is connected to this block right through a control logic.

And then you have a clock, you have a counter, you have reaches and finally, you have the binary output. So, this is a block diagram of dual slope ADC suppose people ask or if in the exam you are asked what kind of dual slope ADC block diagram looks like you can draw this very quickly, assume that the counter is reset and the indicator output is 0 ok.

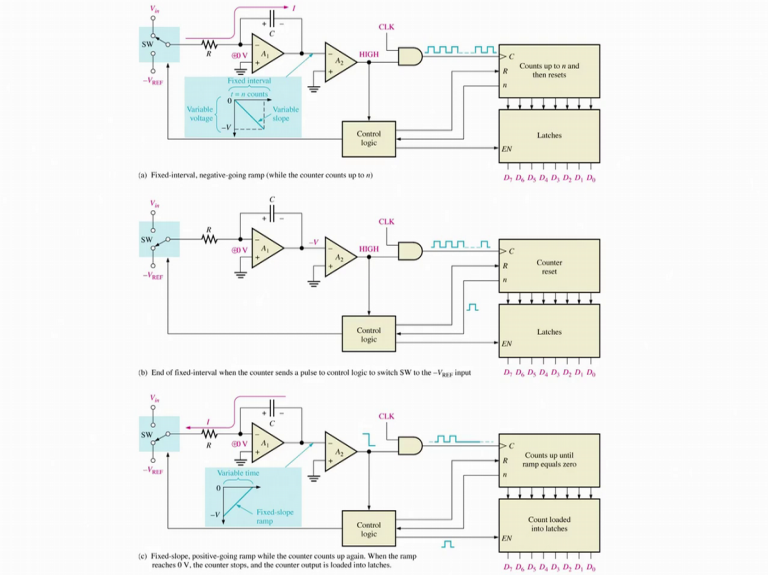
So, if the counter here is reset right counter is reset and you are here under is reset and your integrator output is 0 right. So, positive input voltage is applied to the input truth switch so here we are connecting switch to the positive input voltage and then seen the inverting input of A 1 is a virtual ground and assuming that V in is constant for a period of time, there will be a constant current through the input resistor and through capacitor correct.

So, it will be a constant current through input resistor and capacitor when you connect these 2 plus V in capacitor will start charging linearly because the current is constant and as a result there will be a negative going linear ramp on the output a one correct. Now when the counter which is at specified count it will reset and the control logic will switch back the negative reference voltage to input of A 1 in that case what will happen at this point capacitor is charged to negative voltage proportional to the input analog voltage.

So, now the capacitor discharge is linearly because of constant current from minus V reference. So, now, the capacitor has to discharge and have a constant slope that is independent of charging also one is capacitor charges then the counter resets and a capacitor starts discharging. As the capacitor discharges counter advances from sets the time it takes from capacitor to discharge from 0 depends on the initial voltage minus V when reaches A1 reaches 0 A2 reaches to low state right because A1 reaches to 0 A2 will reach to low state.

And disables the clock of the counter which is if there is low the clock will be disabled and if there is a case the binary count is less that is completely one conversion cycle the binary count is proportional to voltage V in.

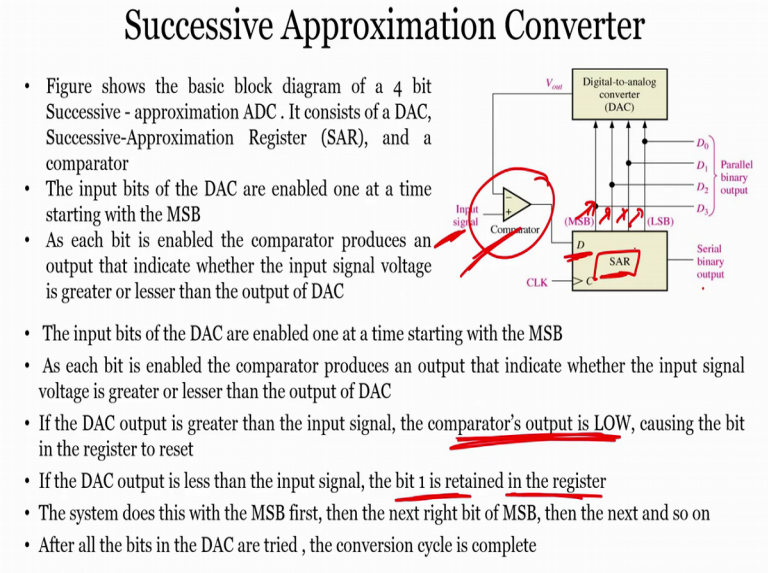
(Refer Slide Time: 08:43)



Now, this whole process is illustrated right over here right well initially the capacitor is charging when you are when your counted up to n and then is resets and then it is sent back it. When it is connected to plus V it is charging where is connected to ground then

at some point it because of the when there is a signal is sent it will start discharging capacitor will start discharging this will cause the change in the output signal.

(Refer Slide Time: 09:09)



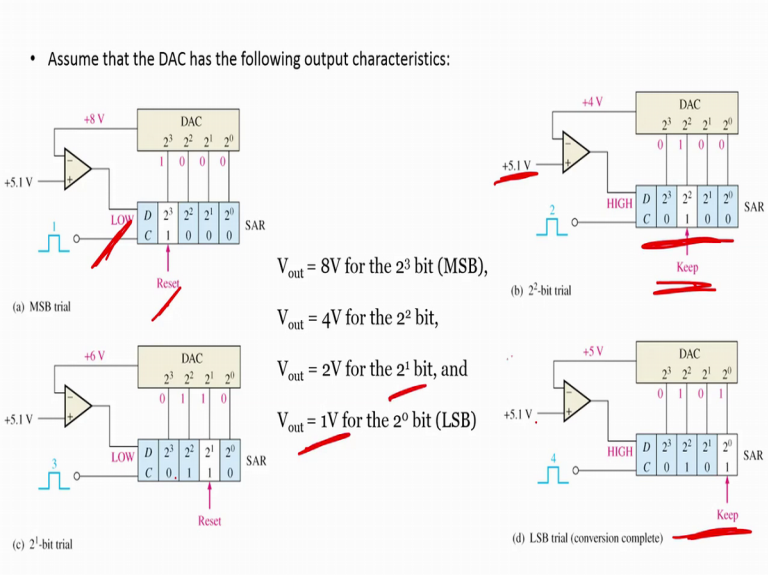
Now, if you have to understood the flash and dual slope ADC's let us see successive approximation ADC. Successive approximation ADC the block diagram is shown here when it has added digital to analog converter it has a SAR it has a digit clock and it has the serial binary output. It is connect the signal there is a digit connected is to the output of the comparator and we have a parallel binary output from D 0 to D3.

Now, the input bits of DAC are enabled only one at a time starting with the most significant bit and each bit is enabled the comparator produces an output that indicates whether the input signal voltage is greater then or less than the DACs. So, you understand this if the V out here and the initial input here. So, if it is more than the DAC or less than DAC we can easily see with the help of comparator, if the signal input is more than DAC then we can have a higher bit the signal input is less than DAC we can have a lower bit rate.

So, the input of the DAC are enabled one at a time with MSB at each bit is a matter compared to producing output that indicates whether input is greater or less than the output of DAC. The DAC output is greater input signal the comparator output is low causing the bit to bit to the register to reset right. So, we send here a digit called reset now if this DAC output is less than input signal then bit one is retained in the register.

Now, this is of course, register which is shown here and the system does not does this with the first MSB first and then next right off they start with MSB and then this one and then this one and finally, comes to the LSB after all the bits in the DACs are tried the conversion cycle is completed.

(Refer Slide Time: 11:03)

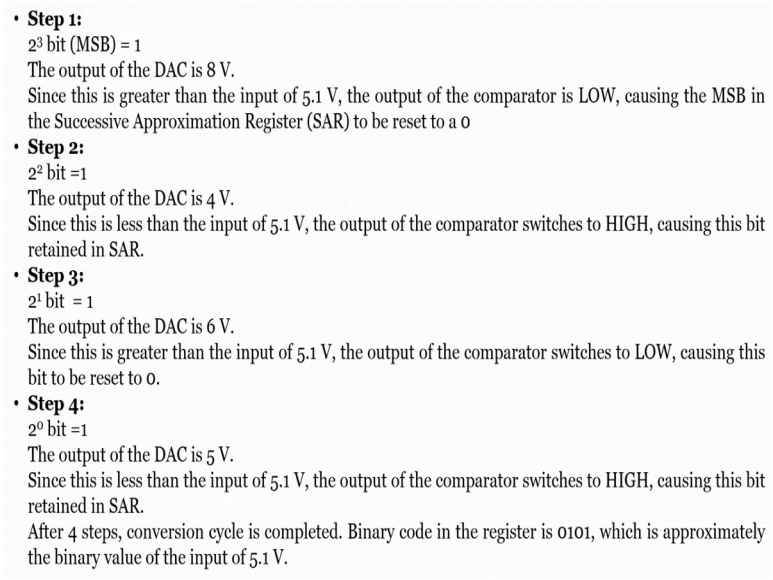


So, this is V out of 8 bit balls for 2 per to 3 you can see here as in the DAC following characteristics you can very clearly see plus 5 1 volt plus 5.1 was is given. Now you we have here 8 then 8 volt is greater than 0, so, low is same sent right.

So, now, it is sent here. So, when you could apply a clock you have 1 0 0 0, but if you have for 6 volts right then what will happen here is still is more than 5.1. So, again a low is applied and you have if you if you send this signal then it will be 0110 right. So, 110 will be the value. Same way if you go for 4 volts then in that case for was is less than 5.1 volts that is why it will be high bit and you can have here 0 and then 1 and 0 and 0 this will be in your register which is the when you are do keep.

Now, in this case if you see if there is a low value then you have to reset this value, there is a low value auto reset this value, but if there is a high value then you can keep this value. Same way here 5 volts is less than 5.1 volt you can keep the last significant bit which is (Refer Time: 12:19) which is 2 raise to 0 it's a 1 volt for 2 raise to 0 bit we can return here right 2 volts for 2 raise to 1 bit we can see here and similarly. So, it's very easy to understand the DA,C ADC characteristics and DAC characteristics.

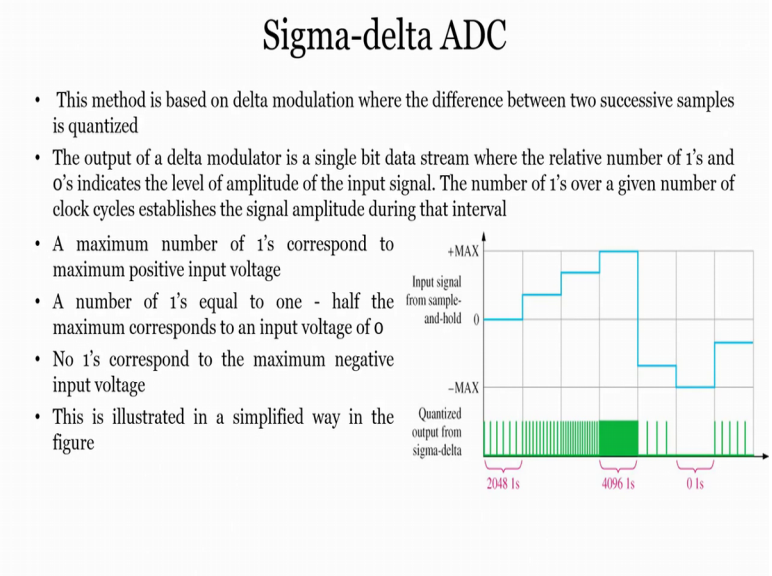
(Refer Slide Time: 12:35)



Now, this how the operation works. So, just to look at the slides in detail you can see very clearly let us take one example or let us take this example well step 1 2 raise to 3 MS bit which is your most significant bit and output of DACs is 8 volt. Since there is greater than 5 volts the output of the converter low causing the MSB of SAR which is successive approximation register to reset to a 0. Now step 2 is 2 raise to 2 which is bit 1.

So, output of DAC s is 4 volts which is less than 5 point 1 volt in that the comparator on switch is too high causing this bit to return in SAR. Similarly step 3 if it is 2 is to is to 1 which is 1 volt then output of DAC s 6 volts; since this is rather than 5 volt output of comparators which is too low. So, it's very easy right if it is more or less that is what we are comparing nothing so, difficult in this particular ADC.

(Refer Slide Time: 13:29)

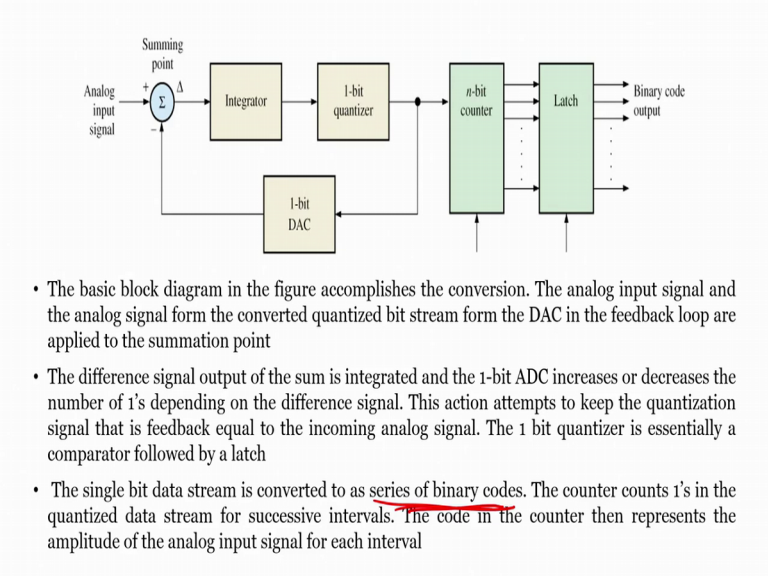


Now the final 1 would be sigma delta ADC. So, what is the sigma delta ADC means? This method is based on delta modulation where difference between 2 successive sample is quantized the output of delta modular very single bit stream where the relative numbers of 1s and 0s indicate the level of amplitude right.

So, how many 0's are there, how many 1's are there and the number of 1's over a given number of clock cycles establish the signal amplitude during the time interval. Now here the maximum number of 1's corresponds to maximum positive input voltage and number of 1's equal to one half the maximum corresponds to input voltage 0 right.

So, one half will correspond to 0 only 1 will correspond to high, number of 1 correspond to maximum negative input voltage this is illustrated in simplified way in this particular figure as you can see here 2048 1 4 0 and 6 1's these are all 0s when 0s it is minus negative if it is 1 it is plus, if it is in between then it is consider as 0.

(Refer Slide Time: 14:33)



So, if you see this particular ADC right which is our sigma delta ADC and this is a block diagram when you have the integrator, a quantizer and bit counter latch. And output of the 1 bit quantizer is feed back to the 1 bit DAC which is sent to the summing point where the summing point will look at the signal sent by 1 bit ADC DAC and analog input signal and the error is fed to the integrator.

So, that is what is written over here and a different signal output of the sum is integrated and 1 bit increases or decreases number of 1 depends on a difference signal this action attempts to keep the quantization signal that is feedback equal to incoming analog signals.

The single bit data stream is converted to as a series of binary codes, the counter counts once in the quantized data stream and code in the counter that we wizened amplitude for final signal for each interval. So, the point is the most easiest way of understanding DAC or ADC is when you use it until you use it you guys will not know how to operate this ADCs DACs ok.

So, what I think what we have learned in this particular module is how what kind of ADCs is are there and we are just if you have really see we are kind of run through that ADCs the reason is that we have to use this ADCs, the detail of how the abc s are operated is good to understand.

But how you can use it is more important alright. So, I leave it on you how you have you read it further how you understand it further if you are confused do ask me anytime you can ask me. But if you know how and where to use ADC's and DAC's for a signal consistence system that is where the real application lies in.

Because when you design electronic consistence system you need to know what kind of circuits you had to use right at what point your ADC will come at what point your DAC will come, at what point your filters will come, at what point your amplifiers will come at what your integrator and comparators will come. At what point your sine way and this kind of frequencies and generators signals will come at what point you have to interface your sensors to your (Refer Time: 16:51) distances system.

And at how you can convert this data to our display. So, this everything in some sort when you bring it together you can design a complete system. And through this particular modules what I have tried is to help you out or to share with you how to apply or use or presumably fire in real life scenarios in the practical applications and in that when you see the block diagram when you further go and see the circuit diagram.

Then you will see that where exactly this kind of circuits are used ok. So, you just go through it once again, if you have any doubts feel free to ask me right and then you take care, bye.