Fundamentals of Semiconductor Devices
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Lecture - 57
Basics of microelectronic fabrication

Welcome back. So, we had left last lecture and we ended on flash memory drives I told you the transistors with a floating gates are used in your flash memory drives. So, transistors have wide applications and we have discussed about power switching, power amplification in RF and memory devices like flash right.

Of course DRAM and SRAM they are also devices with semiconductors transistors, we are not talking about that right now, but you can just Google up and read they are very easy to understand. What remains little bit is a transistor since in high speed digital logic and after that we will go through some of the discussions on how to actually fabricate this devices practically.

It is not a fabrication on course so we will not go into details, I will just give you a quick idea of how devices are fabricated in real world right, what are the techniques and equipment used. And maybe in the last 2 or 3 lectures that are remaining we can solve some practical practice numericals from maybe previous years question papers and so on ok. So, let us come to white board and finish up what is spending of transistor applications.

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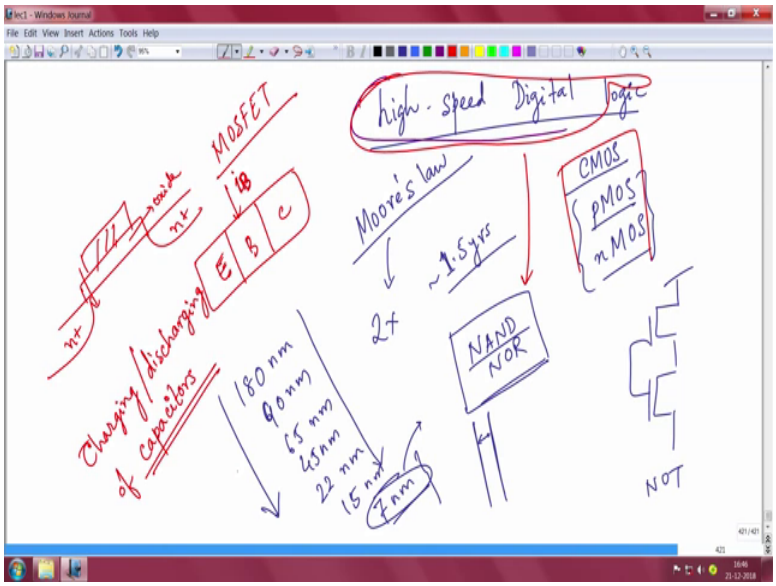

So the last application note that I had said we should discuss is about high speed digital logic and frankly speaking high speed digital logic is something for which all the MOSFETs you know that we have talked about in this course are used.

So, essentially we are talking about CMOS; CMOS stands for Complementary MOSFET. So, you have a pMOS and you have an nMOS which means you have a p channel MOSFET an n channel MOSFET and you can use them to make inverter sort of things right. You use a pMOS and a nMOS to make this inverter or NOT gate and you can make all these digital gates that you talk about like NAND, NOR, ZOR and so on.

This digital circuits or digital gates that you are learning or you have learnt these digital gates are made possible primarily because of this pMOS and nMOS it is a very comfortable and best flat form it is called CMOS platform. And CMOS enables you to make this digital logic circuits which are high speed that have enabled the processors all these computers and mobile phones right.

And with gradual shrinking of the device dimension which comes with Moore's law, you are able to make the devices faster and incorporate more functionalities in the cheap chip, that is because you have more and more devices per unit area that is what Moore's law says that the number sort of doubles every one and half years. It has been going on, actually it is going on and you know people predict and, but we will see when it ends right.

So, we are shrinking the transistor dimensions from you know microns to 180 nanometres to 90 nanometre 65 nanometre and so on right, 45 nanometre. Now you know we have also 22 nanometre, now people will talking about 15 nanometre which is commercialized, 7 nanometre note you know where Samsung and TSMC are completing there, 7 nanometre note is also now almost going to be real. Of course, this 7 nanometre. Now in this game this is also business game what essentially what this dimensions mean initially they meant like, maybe the size or the gate length or something of the transistor.

But now essentially it means the distance between two DRAM lines or you know the distance between two adjacent lines if the resolution anyway we can say 7 nanometre. But please remember that 7 nanometre for Intel and 7 nanometre for Samsung will not be the same, these companies have different terminologies nowadays. So, for example, 7 nanometre of TSMC might be actually 10 nanometre of Intel and so on.

This shrinking of this transistor dimensions allows you to get devices that are faster and you can incorporate more functionalities because you have more number of devices per unit area this is all primarily done for high speed digital logic ok; this is primarily all done for high speed digital logic. So, all the digital circuits NAND, NOR every all these gates are made of CMOS logic.

So, all the things that you have learnt in MOSFET and you know MOS capacitor they have essentially being contributing to these high speed digital logic ok. High speed digital logic can also be made of you know BJT sort of a thing by CMOS and all, but there is always this laws that is associated with BJT because in a BJT if you remember you have emitter and then you have base and then collector you have a base input current going in.

So, this base current essentially is a input current and there is a always a I square or loss you will actually keep losing power because of this base button and MOSFET you have this insulating gate know this is n plus, this is n plus and then there is an oxide here. On top of that you have the gate metal. So, this oxide has a very little current leakage. So, your input loss side you know that the current leakage current loss off state loss will be very low, that is why and also the ease of fabrication and scalability is better here.

You can have a large density of devices in CMOS and that is why high speed digital logic has been preferred for CMOS you know CMOS is preferred for that and you want

to make the device faster. So, essentially the high-speed digital logic consists of you know charging and discharging of capacitors ok. It is all about charging and discharging of capacitors all this NOT gates, NAND gates you see, but physically in reality they are actually capacitors that you charge and discharge.

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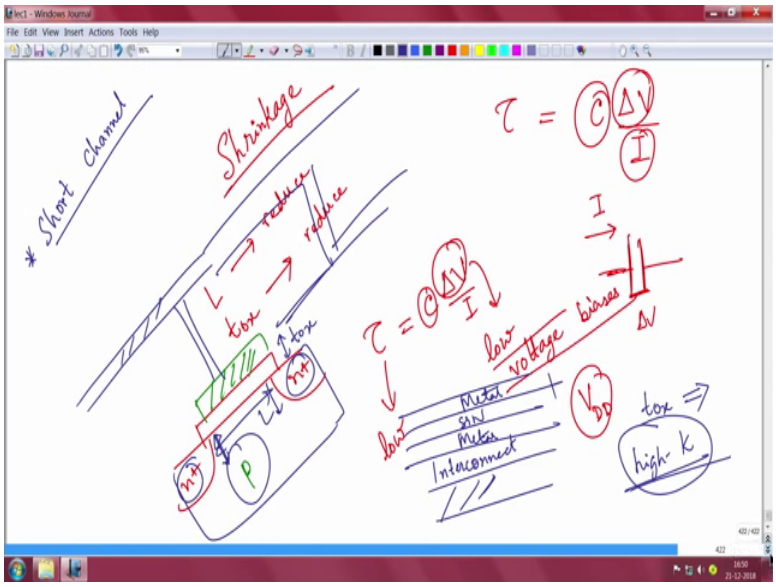

And the charging time and discharging time of capacitors in this case actually is the capacitance value times the change in the voltage that you are doing divided by the current that is implementing the. So, you have a capacitor for example a node, this capacitor could be a transistor or something that you are actually discharging what is the current that is used to charge and discharge that is this. What is the delta v? The potential you are actually moving around that is this and C is the capacitance of these things.

So, to make devices faster you need to make sure that your this time that is taken to switch or to charge and discharge should be as low as possible to get device that is faster and for that you need a low capacitance and you also need low voltages, you need low voltage drives or you can say low voltage biases right. So, that is why faster with the first generation, latest generation devices your V DD is also is shrinking, V DD is your the bias and this bias is shrinking so that you know the voltage that you have to move around across this devices also reduces you can get faster devices.

So, drain bias thus play a role in the device how far they are working in a way and with continuous shrinking of this devices you probably have known these and I have probably

have told this in other. You are shrinking the device dimensions both laterally and vertically which means the gate length is reducing, but along with the gate length you also have to reduce the dielectric oxide thickness because you need to maintain an aspect ratio. Your thickness of the dielectric or the gate dielectric also has to reduce, I told you about the constant field scaling constant voltage scaling.

All the device dimensions are shrunk in such a way including doping they need not be all done to reduce the maintain the constant field or constant voltage, but all the different dimension of a MOSFET you know this is n plus, n plus and then you have a oxide here and then you have a metal here sort of thing right then this is the doping.

So, you know this doping level this depth of this junction this doping of this junction the junction depth, this length the transistor length, this thickness the gate oxide thickness all this these are reduced appropriately. So, as to ensure the device works close to what we want, the device works as desirable as we want.

So, this shrinking has been going on the gate oxide for example, has been reduced and with reduction in gate like leakage your leakage reduce increases. So, that is why people have gone for high k dielectric that I have already told you in one class, using a high k dielectric you can have a thicker; you can have a thicker dielectric, but the capacitance action is the same right.

So, then short channel effects come in this all this scale devices that also we have discussed in details, short channel device affects come when a device has become very short maybe 100 nanometre and less than 100 and a few 100 nanometre short channel effects can also kill your device so you have to take into account there.

There are things like strain channel germanium silicon alloyed, strain channel where you can enhance the mobility of holes for example, you are talking about new types of metal contexts poly silicon contexts, the interconnect delays have to be reduced because there will be multiple layers of this transistors that you have to connect from many lines.

These are called interconnected lines you know from one transistor to another transistor you will have lines, this interconnected lines also will lead to parasitic resistances and capacitances, you have to reduce the interconnect delays. So, when you have multiple layers you know one layer would be your transistors for example then you have

interconnected dielectric. So, will that will be a dielectric layer that will separate then there will be another metal line here, then there will be again a another dielectric some silicon nitride another metal layer here.

So, we keep doing this for multiple layers of integration and this inter layer dielectric or interconnected dielectric can you know also will increase a lot of delays and slow down the circuit. So, for high speed digital logic you need dielectrics with low dielectric constant in this inter you know inter layer dielectric so that the charging discharging delay is smaller. Whereas for gate oxide you need a high dielectric constant to make sure that you can have thicker oxide and still have lower leakage and you know equivalent oxide thicknesses high. So, there are many of these things and eventually everything is culminated in Moore's law.

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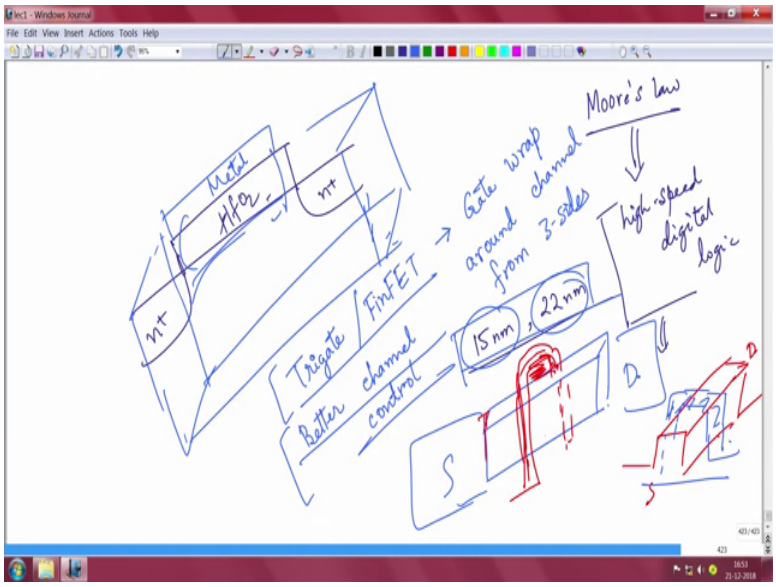

And all this Moore's law applies to the shrinking of the transistors and all this shrinking of this transistors and everything that we do is primarily to do with high speed digital logic only ok; high speed digital logic. So, high speed digital logic all the digital circuits we have learnt that all it goes here and now in more recent times you know CMOS is a planar device. In a planar device with such a small dimension as 15 nanometre for example, or 22 nanometres and such dimensions your CMOS planar device will have terrible short channel effect. Your gate is always at the top right so you have an n plus for example, n plus here and then you have a dielectric here, its silicon dioxide for example,

or whatever hafnium oxide it is a high k dielectric that you use it cannot use silicon dioxide only.

So, you will use like a hafnium dioxide and then you have like a metal here right. What I was about to tell you is that you know it is a planar device so you can think of it like a planar device sort of a thing right, it is a planar device; it is a planar device, but in planar device the metal will only be able to influence the gate from the top. So, the channel depletion and other things are difficult to control because of short channel effects.

So, what people have come out come up with some as called trigate devices, trigate architectures or these are also called FinFET because they have like a fin their device looks like a fin this trigate actually architectures are such that the gate will not be only on the top, the gate will wrap around; the gate will wrap around the channel; the gate will wrap around the channel from three sides not only one side from three sides ok.

So, what it means is that, you might have like a; you might like have a fin like this actually I am not very good at drawing, but you might have a fin like this and then this will be the this will be like a source and this will be like a drain and this fin this is like a connecting is silicon only. Your gate will like wrap around this whole thing right from the other side also. The gate will wrap around; all around top bottom everything with a dielectrical force will be there, but it will wrap around everything. It is like you can think of you know this is the side view, but in the front view you can think of like this kind of a structure right. So, source is here drain is there for example.

And the gate will come up you know on top of this like this right it will also go on the other side of course. So, it is like a FinFET or a trigate architecture that helps a better confinement of the carriers a better channel control is coming. Because you know you have your; you have your gate that wraps around the channel you know gives you a better control and you know control short channel effect, better control of threshold voltage you know current modulation and so on.

So, commercial devices and processes and all actually employee trigate FinFET architectures, the digital planar CMOS logic is used, but not in 15 and 22 nanometre nodes. If you have large devices like you know 180 nanometre maybe few microns.

You still use CMOS there, but all these devices like 15 nanometre, 22 nanometre you people actually use FinFET and trigate architectures for your commercial devices ok. So, this is a basically about high speed digital logic. So, that is pretty much about high speed digital logic. We have finished whatever we wanted to do it. Now what remains now is I will spend the rest of the time in this course that we have maybe a few lectures more partly in going through quickly about the practical aspects of fabrication that we will discuss right now.

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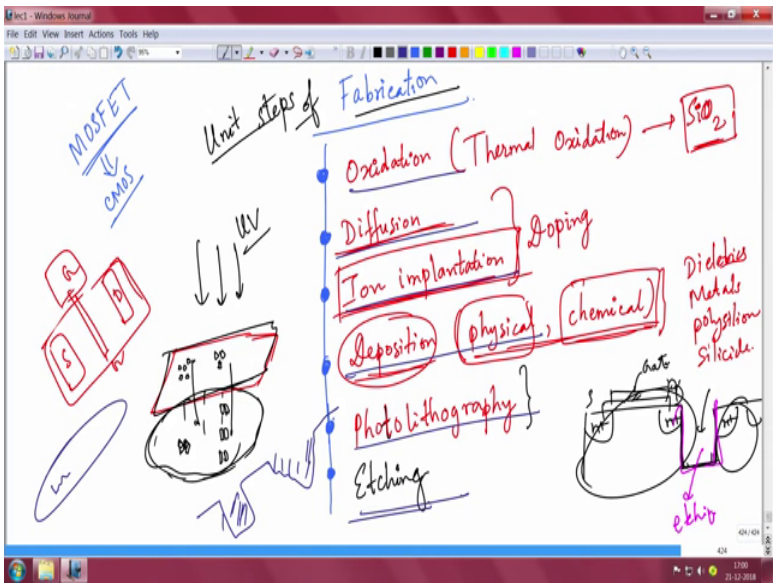

So, we will go through the aspects of fabrication, the practical aspects of fabrication that we should be aware of because it is not important than only we understand the devices and the physics of semiconductors. But you should be just basically be familiar with the real aspects of device fabrication so that whenever we device a design a new device or we talk of a device you know engineering we should also know the limitations of the fabrication processes because in reality you have to fabricate a device right.

So, they have any of course, devices, but I will talk about a classic MOSFET for example, the you know how do you fabricate a MOSFET. And then of course, if you know how to fabricate a MOSFET then CMOS fabrication can be understood we do not have to go in very details because this course is not a fabrication intensive course.

So, there are many key steps ok, there are many unit processes of fabrication what I am telling you here are unit steps or unit processes of fabrication of semiconductor devices

and this unit processes of device fabrication are you know they are used in conjunction with one another or they are used in a particular sequence, particular fashion to enable device fabrication such as a MOSFET.

So, for example and this is not an sequence I am talking about I am just talking about the unit processes that you use. So, for example, one step one of the unit processes is oxidation, when I say oxidation I typically mean say thermal oxidation ok. So, this process is used to grow silicon dioxide gate dielectric for example, for example you need to grow silicon dioxide gate dielectrics right that you remember.

And there are other approaches to also growing or depositing silicon dioxide, but this gives you very high quality thermal oxidation and this is primarily used for making the gate oxide. For example I told you there are also other techniques to use silicon dioxide suppose you want to use silicon dioxide as an interlayer dielectric or some other you know layers sort of thing.

Then you have two techniques one is called diffusion and one is called ion implantation, these are techniques that are used these two techniques that are used for doping you know p-type and n-type doping in semiconductor and these are for silicon I am talking about not for compound semiconductor. This diffusion and ion implantation are typically used for doping in silicon, you know with all this doping of p plus, n plus pockets and a channel and the p type substrates and n type substrates and so on. These are used there then of course; you have deposition, deposition of different materials including metals dielectric insulators.

This can be physical deposition physical like you know you are using a brute force you know some kind of physical vapour deposition and so on. It can be also chemical deposition where essentially you have a chemical reaction that will deposit the material. You can use this to deposit dielectrics including silicon dioxide by the way, dielectrics you can also deposit metals, you can deposit poly silicon.

Remember poly silicon gate you can use and then you can put silicide and so on, many things can be deposited here. One of the important techniques of course, all of these will need very intense equipment and a very expensive equipment these are housed in something called clean room.

A clean room is where you have you know very controlled environment minimal dust particles and so on. This needs very ion implanter for example, ion implantation needs ion implanter which is a very expensive equipment maybe in the order of 20-30 crores it needs extensive effort in maintaining also you need experts.

So, these are expensive tools that are housed inside clean room to in a way to enable the device fabrication deposition for example, can be many types of deposition and all these types of deposition physical or chemical are very expensive tools that are you know that are only in the select areas for examples this is a clean room. Then there is this approach or technical photolithography and this is the most basic and most crucial, photolithography is essentially transferring the pattern. You have this source drain gate I am talking about a top view ok.

Source drain and the gate finger will come like that right this is gate for example, this is a device isolation. You need to transfer this pattern to the silicon substrate from the mask where you are writing you know, you have like a mask it is a chrome glass for example, on that you have this small features.

You cannot see with eye probably they are microscopic and nanoscopic features these are like transistors maybe there is a source there is a gate whatever you know and then you have this silicon wafer below the silicon wafer below sits below on the silicon wafer you have to transfer the MOS patterns. So, that you have all this source drain all the source drain devices here maybe source drain, source drain, source drain.

All this devices are there you have to transfer this patterns from once one and from the mask to the actual wafer by exposing them to UV light. They are actually, there are so many things this process is called photolithography. You can think of it like a old time camera you know, if you see that really you know you have an old time camera you take the click the picture this you know Yashica and all this Kodak cameras similar thing, but it is a much smaller scale nanometre scale or so. You can transfer the pattern from one in to another and the final is called etching, etching is basically removing, you are removing material from a wafer.

For example you might have a silicon wafer I am not drawing it nicely for example, you want to you know if I draw a cross section view maybe you have this n plus pocket n plus pocket. And then you have a gate oxide and then you have gate here this is source

this is drain, but you want to isolate it from another device. So, there is another n plus here, the reason you isolate is that you do not want one device to talk to another device affect the other device. So, you isolate.

So, this trans that you have created this you know this trans that you have created this isolation, this is etching you have etched a silicon a way between two. So, etching also in a way you know you can design some funky structures, you know silicon wafers like that you want to have different structures that are. You know you are etching the silicon away in some areas, you are etching the silicon away you can have different sort of structures v shape or you can define the depth or whatever you are removing the material from selected portion in a selected fashion and trend this is called etching.

So, oxidation, thermal oxidation, diffusion and implantation, deposition, photolithography, etching these are steps and each of them have many you know each of them has many subgroups cum categories like deposition has LPCVD, PCVD, MOCVD so many things right.

So, they have this all these things together this is a unique steps of fabrication and you use this steps to make devices and this is in a particularly in the context of silicon devices that I am talking about. So, we will quickly run through all of this very briefly. As to what it each is all about without spending so much time right you should just be aware.

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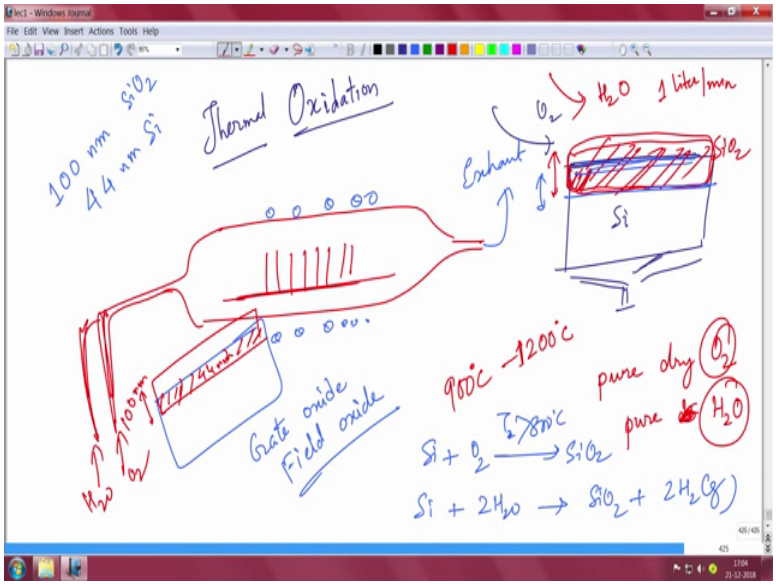

So, first one is oxidation right the first one is oxidation and I mean thermal oxidation, we will not go through the maths of anything. Thermal oxidation essentially is that you take the silicon to high temperature and you oxidize it to get you know silicon dioxide. So, any piece of silicon will always have like a small native layer of oxide here on the top. But you take it to high temperature, you take it to high temperature you heat it up and then you flow some oxygen or water vapour or some gas to oxidise it and then you will have a layer of silicon dioxide on the top.

This layer of silicon dioxide does not come magically, this silicon actually oxidizes some top part of the silicon will oxidize and it will give you like a silicon dioxide layer; it will give you some silicon dioxide layer. So, that silicon dioxide layer actually forms because the silicon some part is oxidized. So, it will eat away into some silicon ok, it will eat away into some silicon because it is oxidized from silicon it will eat way some silicon.

Typically you flow pure dry oxygen vapour, oxygen gas or you flow pure dry oh sorry pure not dry pure water vapour one is this is called dry oxidation this is called wet oxidation. And typically the temperature that you heat up the whole thing is depend, but it is typically from 900 degree to 1200 degree Celsius which is very high and the gas flow this oxygen or water vapour that you flow typically is in the rate of 1 litre per minute ok.

So, you have like a chamber like this, you will have an outlet here and then you have a gas like this, you have this different sort of thing you can put oxygen maybe you can put some other gas you can put water vapour or whatever and then there will be a platform here.

Where you will keep the silicon wafers like that vertically for example and then there will be heater this coils will be there you know heating coils will be there that are like in that tip coils or whatever you can say and then there is an exhaust here. So, you heat the whole thing and you flow these things, typically you use it to oxidise it to make gate oxide and also something called field oxide, field oxide is the oxide that is used to separate one device from another device.

So, these are typically used there and the classic reaction is essentially silicon sorry silicon reacts with oxygen at a temperature of more than 800 degree Celsius maybe 900 to this silicon dioxide that is the dry and in water vapour if silicon acts with water vapour

it will give you silicon dioxide plus a arrangement of hydrogen gas right. As I told you silicon dioxide inter phase will now move to the bottom because some parts of silicon is been eaten up so the silicon inter phase will move to the; into the silicon during oxidation.

To grow 100 nanometre of silicon dioxide you will have to consume 44 nanometre of silicon; that means, if you want to grow 100 nanometre of silicon dioxide on top of that then 44 nanometre of silicon will be consumed, will be oxidized if you do a mole fraction analysis and then you will get a total of 100 nanometre of silicon dioxide ok. That is the and this oxidation processes a lot of mathematics involved, like you want to find out the rate of oxidation this is fixed law you know how much you know surface you need in a concentration and all these things which we will skip you know carefully.

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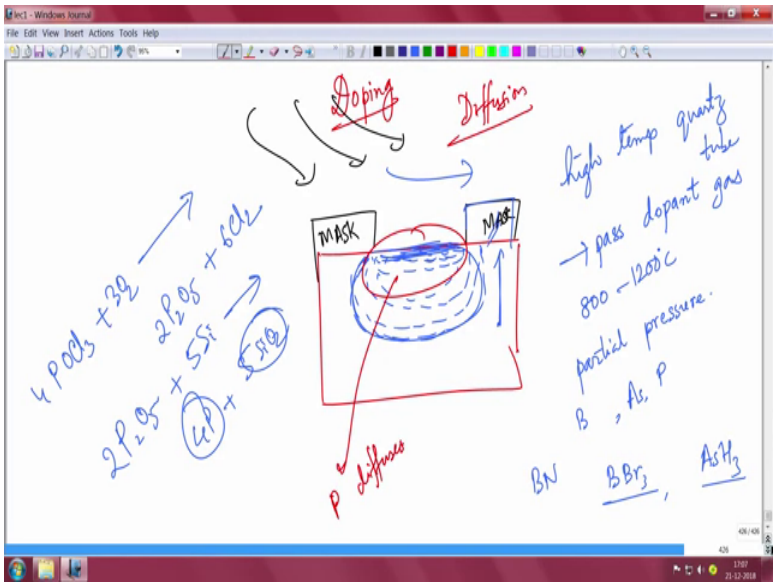

So, you for thicker oxide typically if you want to grow field oxides and all you use wet oxidation and if you want to grow the gate dielectric for thinner oxide you typically use a dry oxidation right. Now then next we come to doping right, next we come to doping and first in doping we will use diffusion.

So, diffusion you have learnt diffusion is of a you know gas particles at one place will move to another place and all the things you know, but here I am talking about diffusion to dope the substance. So, what you do is that you have something like this is your

silicon wafer example you have to make some hard mask like you know you have to make some silicon dioxide or some mask you have to make.

This is a hard mask that you have to use ok, it can be maybe silicon dioxide or something and then you exposed to doping, expose this to diffusion like you will flow some gas phosphene, arsine or whatever and then you will see that you know it will fall on the surface it will react know it will diffuse. It will diffuse inside the surface like this it will be lateral because diffusion is isotropic it will go in all thing.

So, this is the depth, there is a depth through which you are diffusing there is a concentration gradient here many things are there, but that gas will flow and it will diffuse wherever it is exposed to the gas. Wherever it is hard mass it will not diffuse I mean it will diffuse laterally there right. So, this is about diffusion and you are doping. So, this is like a pocket of doping you can say n plus p plus or whatever.

So, what you do is that you place the wafer in a high temperature you sorry you place the wafer in a high temperature quartz tube same thing as like a thermal oxidation. You place the wafer in a high temperature quartz tube and then you pass the dopant gas, you pass the dopant gas at high temperature. For example, the temperature can vary again between 800 to 1200 degree CC for silicon and then the number of dopant will depend on the partial pressure of the dopant impurity gas that you are following; the partial pressure of the dopant impurity gas that you are flowing typically you know you will use boron for p type and arsenic or phosphorus for n type doping.

So, you can have dopant sources; dopant sources can be solid state sources or liquid sources or gaseous sources like you can use boron nitride as a solid source dopant, you can use B Br 3 boron tri bromide as the liquid source or you can use arsin for example, as a gas source. There can be liquid gas solid source many source of doping, but you have to flow the dopant vapour and you know in a very high temperature so that it will diffuse in a way ok.

And it will for example, you might take an example of phosphorus maybe trichloride that if you put into oxygen environment and you pass you will eventually get pentoxide plus chlorine and then this pentoxide that you form it will form a glass on the silicon wafer and that it is subjected to reduction to reduce phosphorus. So, you have to subject it to the heated silicon in that case it will form phosphorus plus silicon dioxide; this is how.

So, this phosphorous will be formed in the surface for example, right. So, this phosphorous will be released in this surface here as talking about, this phosphorus is released there and it diffuses in the silicon that is what happens ok.

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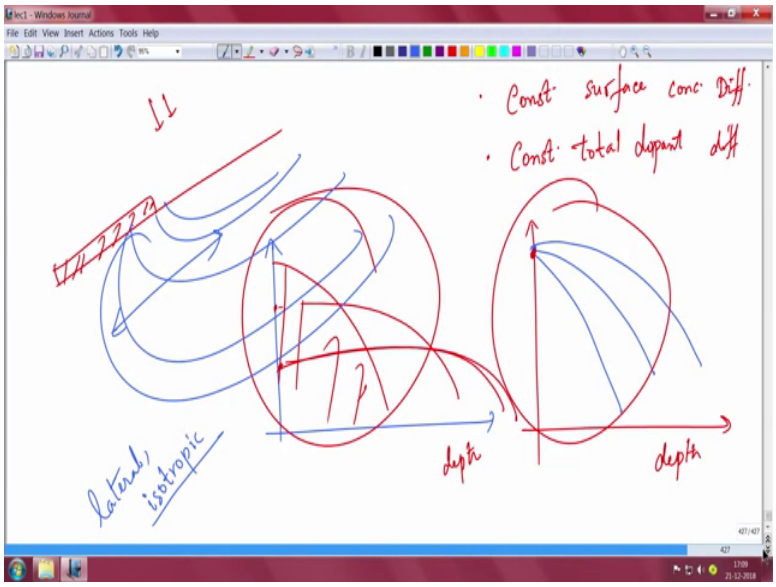

There can be two types of diffusion that you do very briefly speaking, one is called constant surface diffusion which means you maintain a constant surface concentration diffusion, which means you maintain a constant concentration of the dopant at the surface of the wafer and let it diffuse below the surface [FL]. So, the total volume might change of the dopant throughout the surface, throughout the wafer and one is called constant total dopant diffusion.

What it means is that the total volume of doping that you are using is constant at the surface you may not maintain a constant gradient. So, what I mean is that in constant surface concentration, if you this is the depth of the silicon wafer where you are diffusing then your on the surface you will have constant diffusion. So, at different diffusion coefficients corresponding to different temperatures you will have something like that at different temperatures.

At the surface you will remain constant, but over you know the depth it the volume of the doping might also change. In constant total volume you ensure that the total volume a constant dopant in the constant that the total dopant you are using is constant. So, for example, at temperature you have a profile as depth this is depth of course, at higher

temperature it will diffuse more like this, even high temperature it will be more like this. So, the area will remain constant and there is the surface the concentration is reduced it will go deeper, but in constant surface it will be like this. So, there are two types of diffusion both are used in a you know silicon processes the dope.

Typically two step processes are used, a preposition diffusion is used where you use a constant surface and then you use a driving diffusion little high temperature may be you basically do a constant total diffusion that is what you use. And in diffusion of course, even if you have a like a hard mask this is a hard mask for example, and your definition is coming you know this decision gas, the diffusion is actually be lateral you know it will actually go like this because it is a isotropic sort of things. So, there is also a significant lateral spread in the diffusion, you if there is a lateral spread of the diffused doping species and also it is sort of isotropic.

So, it is not you know it is basically spreads everywhere in the wafer, in the all the directions it can go it is not like a anisotropic you know diffusion. So, that is why people have now a days also resorted to you know ion implantation which is the next topic.

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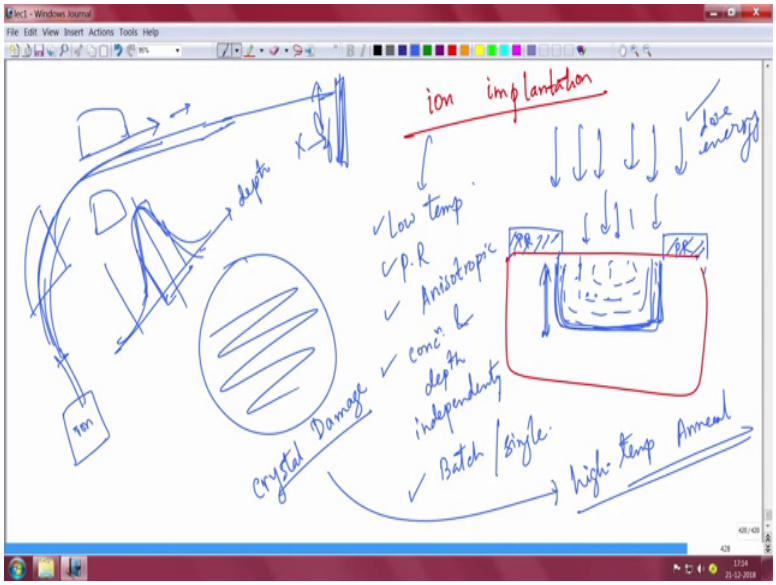

People use still use this diffusion please do not get me wrong because they can do much depth it will much depth higher depth they can go and then you have ion implementation, what ion implantation does is that you have a higher energy beam of ions. So, for

example, this is your silicon wafer here you do not have to use a hard mask, this is a room temperature process only you do not have to heat it up unlike diffusion.

So, it is a low temperature process; you can have photo resists I will come through that photo resists later photo resists are like organic compounds that will protect the surface at certain areas these are easy to put room temperature process and you use a higher energetic beam of say you know phosphorus whatever or arsenic or boron so that the doping is actually isentropic.

So, the doping will only take place here anisotropic ok. So, the doping will be actually only in this and depth to which you go of the doping can be decided by the doze you know the energy of the doping this atoms that you are giving, it is a very expensive tool called ion implanter. It is a very high energy beam of ions that are bombarded and then they go and form this kind of a pocket it is anisotropic there is no lateral diffusion here it is very controlled. But it can do only not it cannot do much higher depth also you have some crystal damage because it is very high energetic very high energetic process, it is a very high energetic process.

So, one is that you can do it at low temperature you do not need to go to high temperature process you can use a photo resist mask which means it is a very simple process that way its it gives you an isotropic doping profile. So, it is [FL] pocket like a vertical wall sort of you cannot, you do not have diffuson here, it can be you can control the depth of the junction and the concentration in independently the concentration and depth of the doping can be independently controlled. Unlike in diffusion where the concentration and depth are related, it can be done here.

You can do batch as well as single wafer you can do batch by batch or you can do single wafer process right. So, that is an advantage because in your diffusion you will need high temperature hard mask and isotropic doping wafer and so on and so forth right. It is a very expensive tool and implantation as I told you.

You have an ion source in some way, you have an ion source that you know that generates the ions, but then you have a magnet sort of thing so that only selected ions with specific mass ratio can actually get deflected. They go through a lot of accelerating plates so that they get accelerated at high voltage, you have many filters and beam focus and other things. And eventually you have the wafer the silicon wafer where you can

scan them x and y so as to you know dope if you have a wafer like this then you can essentially scan and make sure that doping is you know you can control the doping and different parts of the wafer.

But the disadvantage is that, it is a high energy beam of ions that come. So, there is some crystal damage, there is some crystal damage and all the beams of ions that have fallen on the here will essentially make sure that phosphorous or boron whatever you are doing they will all go and sit in the lattice side they might not get ionized. So, you have to do after the ion implantation is done, you have to do a high temperature anneal. You have to do an high temperature anneal to recover the crystal loss and to make sure that all this you know dopant atoms that you have added like phosphorous or boron they are activated, they are able to donate or accept electrons now.

You need to activate them ok; you need to activate them it is also very costly tool very high maintenance also is done. So, most of the academic institutes do not have an ion implanter right. And in ion implantation of course, initially when you implant it will not abruptly stop like that as a function of depth; as a function of depth the doping profile will look something like this.

So, you know there is a Gaussian distribution, there is a range to which you go there is a studle the deviation, but anyways with annealing you can actually approximate like a you know you can approximate this uniform profile here you can get the depth and doping profile it is very important ok.

So, that is an important aspect of ion implantation, you can do all this simulation tools that are used to predict how much doze of ions you need what is the energy of the ion the angle, the tilt the rotation of the wafer and so many things are there then show that ion implantation is done to get this. You know very high aspect ratio or this you know a highly anisotropic profiles can be obtained in a doping sort of things.

So, that brings us to an end to this lecture. We have finished up some of the parts of fabrication now; we are still a couple of lectures remaining to finish the course. And this today's class we will end with this discussion on ion implantation. So, we have taken care of, we have started this lecture with the remaining of CMOS high speed digital logic.

We have introduced many of the fabrication techniques what are the techniques that are needed like you know photolithography, ion implantation diffusion and you know deposition and so on.

So, these are the things that we will study. We have covered thermal oxidation, we have covered diffusion and ion implantation which are used for doping right and in the next class we will probably go through some the deposition techniques, how do you deposit metals dielectrics and different kind of poly silicon and so on and so forth, physical and chemical depositions. And then we will go through etching and photolithography so that we are familiar with the very basics of how device fabrication is actually done ok.

So, thank you for the time and I will see you in the next class.