Fundamentals of Semiconductor Devices
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Lecture – 31
MOS: Capacitance Voltage

Welcome back. So, if you recall in the last class, we had started MOS capacitor - metal oxide semiconductor. In the next couple of lectures I said you know, we will finish up understanding the classical MOS capacitor which is very important to understand MOSFET. So, if you recall in the last class, I told you how a schematic of a structure looks like and we also discussed the energy band diagram. I told you that depending on the gate bias that you apply on the metal, your bands will either band upward or downward and you might get different conditions.

So, we took the example or the case of a p type doped silicon on which we have an oxide and a metal told you that you know, if you apply a negative voltage on the gate on the metal, then you are going to get an excess of holes at the interface; it is called accumulation. And if you apply positive bias on the gate metal, then you are going to repel the holes away from the interface. So, you will deplete the semiconductor near the interface and then eventually, as you keep increasing the gate bias as more and more positive, the bands will keep bending and bending until the Fermi level will be closer to the conduction band than to the valence band. In other words, you will start getting electrons, although it is a p type semiconductor and finally, we will have strong inversion where you will have so high, you know, a bending in the band that your conduction band and Fermi level will come very close, you will have a very large number of electrons as high as electron concentration as it is holes in the bulk of the semiconductor; that was strong inversion. So, we will start from there now and we will discuss about the capacitance diagram. So, the idea of our understanding will be that first we shall discuss the physics the logic and you know the explanation of how things are happening and what are happening, and we will put the equations in the mathematics to the back.

So, once we understand the concept in from the physics point of view, after that we shall start the equations or the mathematics, we shall not write the mathematical equations initially ok.

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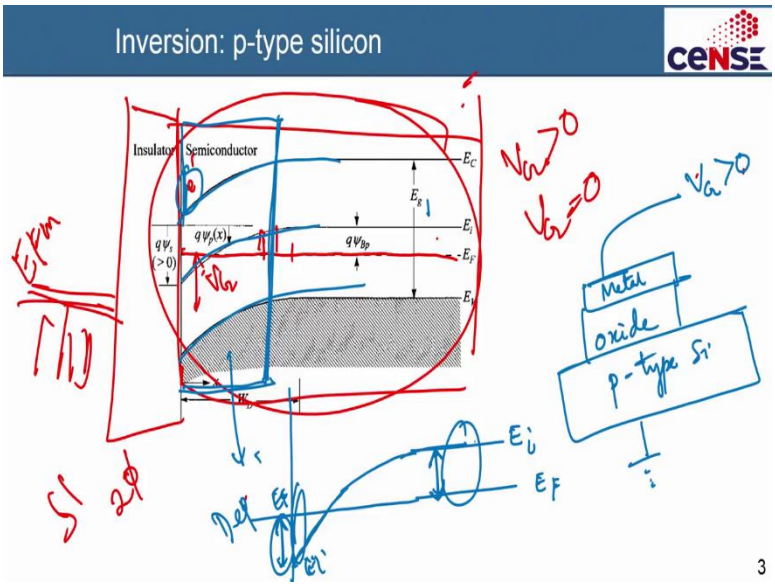

So, let us come to the slide again. So, if you saw in the last slide; this is the last slide. So, I told you this is the diagram for your energy band diagram for your MOS capacitor. You will have a metal right, you will have a metal, you will have an oxide and then, you will have a semiconductor, say you will have a p type silicon. So, in this case, if this p type silicon is grounded and you are applying a voltage here which I call V_G as a gate voltage I am telling it, then if your gate voltage is positive, then you are going to get a bend in the energy band diagram ok; you are going to get an energy band, you will get a bend in this diagram that you can see that this is a bend that is happening, this is a bend that is happening right and this bend will eventually be such that, essentially what it means is that, you are pulling the bands down. So, you are getting increasingly more electrons here and this part is also depleted where the field is a field exists no; this part where the bands are not bend as bend, this has a field and this is a depletion region because you are pushing the holes away from this area. So, it has fewer holes, but also it has an increasing number of electrons.

So, it is the electron concentration will be confined very close to the interface, but a depletion will extend pretty large ok. So, there is a depletion region here that is formed and because the conduction band is now coming closer to the Fermi level, so there will be more electrons here and I told you that strong inversion is defined as, the strong inversion is defined as when the bands have, if this is the your intrinsic level and this is your Fermi level, the Fermi level will stay flat, but this intrinsic level will bend right.

So, at the at the surface this is the surface, this will this should band so much that you know this E_i - E_F in the bulk should be as much equal to E_i - E_F on the surface, this is E_i on the surface right and this is E_F on the surface; E_F is flat. So, if this amount is equal to exactly this amount, which means the band has bent as much downward as it is here; that means, that there are as many electrons here as there are holes here. Then you call this is a strong inversion. It is the start of a strong inversion, before that it is weak inversion ok. So, before that, this is weak inversion.

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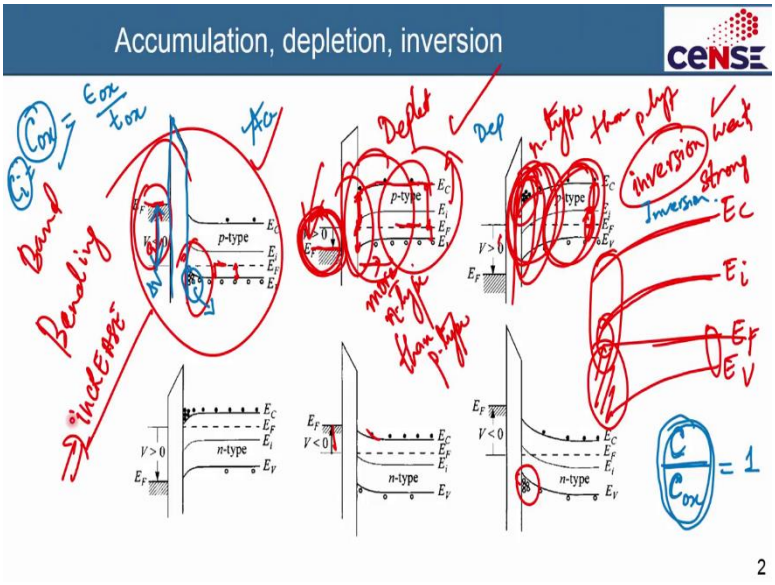

So, these are different conditions; if we also go back to the previous slide I showed you here, right, there are three conditions here. One is the accumulation, this is accumulation, this is depletion, and this is inversion, this is inversion right, this is inversion. So, those things we know now.

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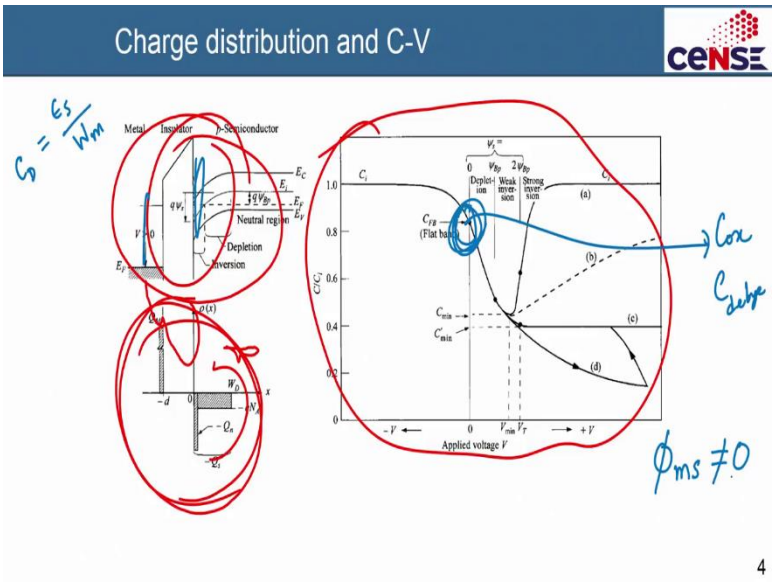

Now, the question is how do you understand the capacitance voltage diagram. So, this is the most important part here. We have to understand this charge diagram ok. We will have to understand the charge diagram. So, for example, if you look into this, let me bring the laser pointer here, ok. So, if you look into this figure here, what it shows you is the charge distribution diagram in an MOS capacitor. So, you have to understand this charge distribution diagram in conjunction with the band diagram here.

So, if you apply positive voltage here, then it is going to repel the holes away and that is why it will create a depletion region here. You see there is a depletion region here. This is the neutral region, there is no change in the field or anything here. This is the depletion region which is forming because you are repelling the holes away, but because the energy bands are bending downwards, you are going to get some electrons here. So, that will be called inversion that concentration of electrons here will also increase as we apply this positive bias more and more.

So, there is a depletion region here and there is an inversion region here, this inversion region is forming because the bands are bending, and the bands are bending because you are pulling the you are applying a higher potential here. So, this inversion charge that forms here will be negative because electrons will be accumulating here, or you can see electrons will be forming inducing here. So, you will have a large density of electrons here which is negatively charged, which is this, the negatively sheet charge of electrons that is forming

and you are depleting the p type semiconductor to up to some extent. It is called the depletion width and the depletion is forming because the positive gate bias here is pushing the holes away and creating a depletion here right.

So, the depletion in a p type semiconductor when you deplete it of mobile carriers, what is left behind here is negatively charged acceptor ionized impurities. So, that negatively charged acceptor ionized impurities is this. They have a certain depth up to which they have depletion. So, this is the depletion charge here, this is the inversion charge here, both of them are negative and the total negative charge will have to be balanced by a very infinitely thin positive sheet charge that is at the metal.

So, the positive gate voltage at the metal essentially ensures that there is a positive charge, you know, that you are putting at the metal which is exactly balancing the charges in the, in the inversion layer and in the depletion layer. We assume that there are no trap or interface charges at the oxide interface or in the oxide. So, now the question is as you sweep this voltage from negative to positive, the capacitance varies like this that many, it is always same till this point and after that it there are many branches. This will correspond to how fast you are sweeping or how what is the frequency of the small signal you are applying. So, let us not come to that right; now let us think again a little bit slowly.

The way you measure capacitance is that, you have a small signal that you apply here and this is grounded, the substrate is grounded, you apply a small signal here and for a small change in the voltage here, what is the change in the charge stored here, that is basically the capacitance and remember this is the oxide or the dielectric that you are putting. So, this dielectric, this is the dielectric that has a finite thickness and a capacitance of the dielectric will also be there, ξ by the dielectric thickness oxide, that is in series in the capacitance that is here. The question is, what is the capacitance that is here and what, you know how will they in series combination will manifest; essentially that is what this picture is about. Let us not worried about this picture very quickly ok; we will come to that.

So, when you have, when you have, when you have an when you apply a negative voltage on the gate, if you recall, if you apply a negative voltage on the gate, then you get an accumulation like this. When you apply a negative voltage on the gate, you have an accumulation like this because this negative voltage will attract the holes towards the interface. So, there will be more holes at this point, then anywhere else. So, there will be

an accumulation of holes; it is a very high density of holes that form at the interface, very thin layer of holes. And any small signal or any small charge that you put or push, you know, will always be added or subtracted from these accumulated holes. These are majority carriers, they can be very fast.

What I am trying to say is that, for any small voltage that you apply on the gate, the corresponding amount of small charge that you will add or subtract will be with respect to the, with the accumulation, holes that are accumulated here. So, if you apply a small signal on the gate, the extra charge will be pushed in and out of these accumulated holes because that is a high density of holes and that can respond quickly. Which means any voltage at the gate is able to modulate the charge at this point. So, the capacitance will be then purely given by this oxide capacitance because, this is a metal. There is it is also like a metal, you know, there is a excess carrier here, which I can pull in and out by applying a gate voltage.

So, the only capacitance that you will see is the capacitance corresponding to this dielectric, which is given by what, let me use the marker again. The capacitance corresponding to this oxide, you can call it C oxide, is actually the ξ of the oxide divided by the thickness of the oxide ok.

$$C_{ox} = \frac{\xi_{ox}}{t_{ox}}$$

So, that will basically, this gives you the capacitance of the dielectric layer. So, any thickness, if you have a thickness of t_{ox}, then the ξ/t will give you the capacitance per unit area; farad per centimeter square of this oxide and this is the highest capacitance that you can get in the whole system. So, if you apply a negative voltage, the total capacitance of the system will be equal to the oxide capacitance only. So, if I say, let me use the marker again, the pen again. So, if I say the total capacitance of the system is suppose C. If the total capacitance of this oxide is C, then I can plot a ratio of C/C_{ox}.

I can also call this C_{ox} as C_I, that is the insulator capacitance, or I can call it oxide capacitance, which is C_{ox} the same thing. Some books call it C_i some books call it C_{ox}, but it is basically the same thing, the insulator or oxide capacitance. So, if the total capacitance is C of the system and the oxide capacitance is C_{ox} which is this, then under this circumstance when you have a negative voltage you are applying on the gate; you are getting more holes here, any additional charge your voltage you are putting here is able to

modulate the charge here, which means only the oxide capacitance will be the capacitance that will show up in the whole system because you are able to modulate the charge here ok.

So, this quantity will therefore, become 1. The total capacitance of the system is actually the oxide capacitance of the dielectric right. So, this ratio becomes 1. So, let me again use the laser pointer here. So, that is what it means by this thing. So, when you can see that this is the region; this is the voltage that you are applying 0. So, this is the negative of that voltage; I was talking about negative voltage. So, when you have negative voltage you are going to get only the oxide capacitance that you will measure because you are able to push in and out holes; this is not a diagram for the accumulation by the way, the diagram for accumulation is this, the diagram for accumulation is this.

So, when you apply negative bias and you get accumulation, this is the accumulation region please remember this is the accumulation region and your C_i basically C_{ox} is oxide capacitance. So, the oxide capacitance, the ratio of the total capacitance C by the oxide capacitance is 1 which means the total capacitance of the system is actually the oxide capacitance and that is why the ratio is 1 ok; the ratio is 1. Now what will happen when you apply a positive voltage on the gate? When you apply a small positive voltage on the gate, you will start repelling holes from here.

So, you will create a depletion region here and the bands will start bending, the inversion has not formed yet, but as you apply more and more positive voltage here, you will also deplete this area more and more; which means the depletion width will keep increasing. The depletion width will keep increasing, but there is a capacitance that is associated with the depletion region ok. There is a capacitance that is associated with the depletion region. That capacitance with the depletion region, I can call it say C_D, that is the depletion region capacitance, that corresponds to the depletion region and that is given simple by ξ_S, the semiconductor dielectric, not the oxide dielectric divided by the depletion region W_m, that the W_m is the depletion width ok.

So, let me again use the laser pointer to point out the thing. So, essentially, your this is the dielectric constant of the semiconductor. This is the depletion width in the semiconductor; this actually corresponds to this width, the depletion width here, the entire depletion width here. So, the depletion width will have a charge know. This is this charge; this is the

depletion width; this is the charge. This depletion width will have its own capacitance if you recall p-n junction and Schottky junction classes that we had taken some time back. This depletion width will have its own capacitance which is given by this is the width W_m. It is called W_D; here I am calling it W_m, does not matter the symbolic. So, the ratio of this is the capacitance, that is the depletion capacitance corresponding to the depletion charge that is stored here.

Now, this capacitance will be in series with the oxide capacitor. Remember the inversion has not yet formed ok; this is the diagram in inversion, but initially the inversion will not form, until your bending it sufficiently high ok. So, this depletion width will have a depletion capacitance which is in series with the oxide capacitance. So, this quantity will be in series combination with the oxide capacitance which is this. So, this in series with this will give you the total capacitance. So, as you keep increasing a positive voltage more and more and more which means you are sweeping to the right, your depletion width keeps going up and up; your depletion width keeps increasing, which means your depletion capacitance keeps decreasing.

And if the depletion capacitance keeps decreasing, then the series combination of depletion capacitance and the oxide capacitance will also decrease and that is why your capacitance keeps decreasing and decreasing. The ratio of the total capacitance by the oxide capacitance which was one initially, with positive gate voltage will start decreasing more and more and more and more, why? Because as you are applying more and more positive voltage, your depletion width is getting wider and wider; a wider depletion width means less lower depletion capacitance; a lower depletion capacitance means series combination of that with oxide capacitance also will be low.

That is why with more and more positive gate voltage, your total capacitance of the system will keep coming down and down and down. Remember the oxide capacitance is constant, which is given by the dielectric constant of the oxide divided by the thickness of the oxide which is constant, but this total capacitance will keep decreasing and decreasing and decreasing because your depletion width keeps increasing and increasing and increasing. However, at very high positive voltage, you are going to get sufficient band bending and I told you that this intrinsic level E_i will bend so much that it will initially touch the Fermi level; that condition is called weak inversion and the start of weak inversion. Eventually will go beyond that and the point where you will have this bend so much that it is as much

band below the E_i as it is above the E_i here or the band bending has become twice of this; that is called a strong inversion. And a sheet of high-density electrons will form here and as soon as the high-density sheet of electrons forms here; which is this point, you have a strong inversion. And strong inversion, beyond that, your depletion width will not extend; beyond that, your depletion width will not extend because this is a high-density charge that you have generated, and this is a minority carrier electron. But it is a very high density nevertheless.

Whenever you apply a small signal here, whenever you are applying a small signal here, what is what is going to happen, I mean whenever not only small signal if you want to go at higher this is not small signal; this is the positive bias only, small signal is riding on this positive bias in a capacitance. When you are increasing the voltage on here, a small a very small bend in the band can exponentially increase the electron concentration, that is one reason. And secondly, this high density of electrons that are formed will screen the electric field and will not allow the depletion width to increase further. That is why the moment is strong inversion has formed or the strong density of, you know, high density of electrons has formed here, after that the depletion width will not increase because this will screen out the electric field from the gate.

And also remember there, a small change in the band is able to accommodate a large change in the in the density here. So, you will not have any excess you know a depletion width that will go here. So, the depletion width the maximum depletion width will be somewhere here and that will correspond to the minimum capacitance. This is the minimum capacitance value. It is called the minimum capacitance and after that the capacitance might either rise or it might stay flat depending on the frequency of the small signal you are applying.

So, essentially if because there is a DC bias here that you are applying which is this, but on top of that you are actually applying a small signal, that is able to modulate the charge here. So, after this point if you apply when you apply a small signal; if the small signal is of very low frequency, say hundred hertz or less than hundred hertz, then the movement of the you know that sinusoid signal is so slow or you know it is so, so slow that the minority carriers here can essentially move in and out in other words there is enough time for minority carrier to be generated within this region. So, that the minority carrier can respond to a change in the signal here, a small signal here; in that case, this carrier can

move in and out of here; the depletion capacitance will no longer matter. Because this small, you know, the small signal here will be able to modulate the minority electron charge, this charge essentially, the sheet charge from here.

The minority carriers will get enough time to respond, to generate ok; to generate thermally otherwise inside the inside the bulk of the semiconductor to move in and out of here. So, any change that you apply here will essentially add or subtract charge here. So, you again have only the oxide capacitance in series because a change in voltage here is able to modulate the charge here. So, the only oxide capacitance is the capacitance. So, the total capacitance again after that will come back to the oxide capacitance. So, the ratio will stay at 1.

However, if the frequency of small signal, you are applying here is very high in the range of say kilo Hertz for example. Then or megahertz, if you apply very high frequency signal, then its switch, this small signal here is switching so, it is moving, so, it is basically changing so fast that you are not giving enough time to the minority carrier to be generated in the bulk to move in and out of here. So, any extra voltage that you are applying here has to have a corresponding charge that you add somewhere here. Initially it was here when the signal was slow, but if your signal is fast, then you will not get enough time to generate minority carriers to add and subtract the charge here.

So, the excess charge that you have to add and subtract when you apply a small signal here has to be at the end edge of depletion because the depletion is formed by pushing and pulling out the majority carrier holes and holes can respond very fast of course. Because they are majority carriers, holes can a, holes are everywhere they do not they are not limited by minority carrier lifetime and so on.

So, any small signal that you apply here no matter how fast, I mean within the range of course, kilohertz or megahertz for example, if you apply fast moving ac signal here, this minority cannot carrier cannot generate movement in and out here; the excess carriers will have to, the delta, the ΔQ that you are going to add or subtract in response to this will be added or subtracted at the edge of the depletion because the majority carriers will move in and out of here, the majority carriers will move in and out of here. So, then this capacitance series capacitance of this in series with this oxide capacitance, which is this value will sustain and it will keep going like that.

So, because any chance, change here is basically being a change here, that is why it is a series capacitance of this and this oxide capacitance, which is this and remember that this value of the capacitance is the minimum value of capacitance because this corresponds to the maximum value of the depletion width. There is an equation that you can use to find out what is the maximum value of the depletion width is, if you know what is the maximum value of the depletion width, then you can find out the minimum value of the depletion capacitance.

If you know the minimum value of the depletion capacitance, you can add the series combination of this oxide capacitance to that, you will get the total minimum capacitance of the system. And any high frequency signal will be able to will lead to basically moving in and out carriers from the majority depletion area here. So, the total capacitance of the system will basically get fixed at the lowest or the minimum total system capacitance at here, that is what it means.

And this dotted line means that, if it is neither very slow nor it is fast, then it will be intermediate between them ok. So, you can see that, at 0 voltage and left, this is accumulation, towards the small right of 0 voltage, you will initially have depletion and after that you will have weak inversion. When you will start to bend the bands so much that, the conduction band is approaching the in the intrinsic level E_i is now touching the Fermi level does interface that is a weak inversion, after sometime it will be strong inversion; at strong inversion, you will essentially have very high density of carriers you can all for all practical purposes, you can consider this tip here to be actually the strong the inversion although it is likely to the right here, but for simplistic you can assume that this is the inversion this point inflection point.

And after that either it will rise up to again the oxide capacitance; if it is a small slowly varying signal or it will basically remain flat at the minimum capacitance value corresponding to the maximum depletion depth if the signal is very fast, ok. That is basically what it means in that capacitance voltage curve here, I hope you are able to clear now you know understand it clearly what is happening here.

There is also a plot here you see this is going down and down and down and of course, is a reverse, forget about this part, but it is going down and down and down you know why?

that happens when you essentially change that forget the small signal. You change the DC signal so fast from suppose you are going from minus 5 volt to 5 volts here.

If you go from minus 5 volt here to 5 volt here, very fast, like very fast, very quickly. If you are sweeping in very fast, not the small signal the small signal is riding on that dc bias, but I am talking about is dc bias itself. If you are changing the dc bias very fast, then this elect minority electrons will not get enough time to actually generate and form the inversion itself, which means, if you sweep the dc voltage very fast, you will not give enough time for inversion charge to even form. The inversion charge, the band bending will take some time.

Now, this band bending, the band will bend, this band bending also you will not give any time, you will not give any time for band bending. So, what will happen is that the inversion will never form, why? because you have changed it too fast. In that case there will be depletion because depletion is majority, that depletion will keep extending more and more and more and that is why, the capacitance will keep coming down and down and down and down. Because, you have not given a chance for the inversion to form, that is what it basically it means.

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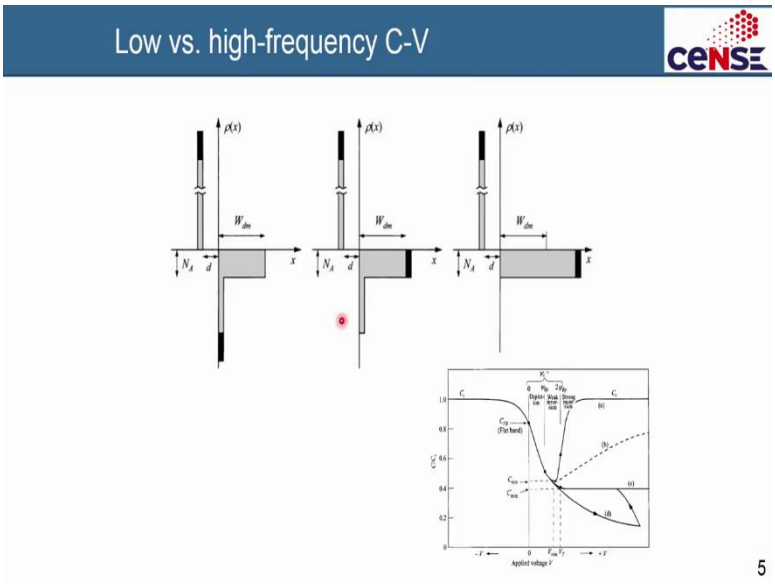

So, this is again I will tell you the low frequency versus high frequency, you know, curves here. For example, this particular figure will correspond to a low frequency; a C-V which corresponds to this branch of the capacitance voltage characteristics. You can see that any

small change that you are applying on the gate voltage you know minority gets enough time to move in and out of the minority inversion charge. So, this is the charge that you are modulating when you are applying a ac signal in the gate. It basically boils down to a dielectric capacitance here, which is this, but the moment you have a very fast-moving signal, then the minority will not get enough time to generate and move in and out of here. So, majority has to move in and out of the depletion region a small ΔQ charge will move in here and this small ΔQ will be added or subtracted from the edge of the depletion region. This is the maximum depletion region that has formed.

So, your capacitance will be series combination of this depletion with a maximum depletion capacitance, oh sorry, the minimum depletion capacitance in series with oxygen oxide capacitance will give you this small value and it will stay flat there. Of course, if you do not give any charge for the inversion to form, this is the inversion layer by the way; this is the inversion layer by the way, if you move the dc signal very fast, then you do not give any time for the inversion layer to form here.

So, the depletion region keeps going up higher and higher and higher and that is why you keep getting a lower and lower and lower depletion. Remember this situation arises when the dc bias is swept very fast. This is called the deep depletion. Under this circumstance, you move the dc so fast that inversion layer has not gotten the time to form, that is why it is going down and down because the you are able to deplete it more and more. The reason you cannot deplete here more is because the inversion has formed that is screening of the field. But the moment is inversion is not formed, there is nothing to screen out, you will actually give keep depleting in more and more and more. That is why your capacitance goes like that ok; that is why capacitance goes like that.

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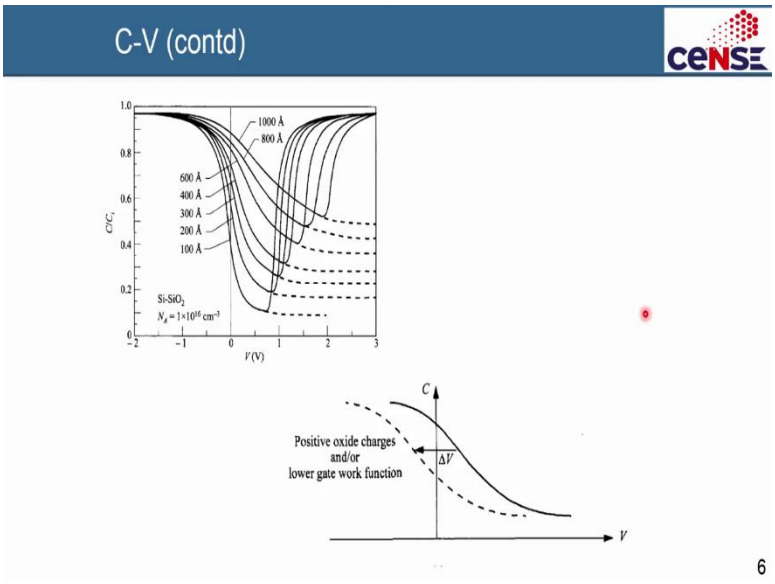

Now, I will come to this quickly.

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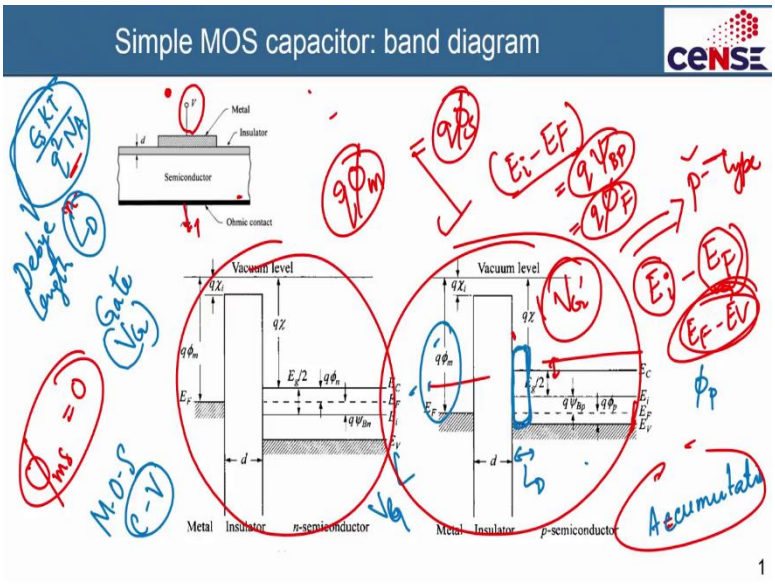

So, now please remember that initially when we had discussed the situation, we had taken a case of this, we have taken a case of this, where the Fermi level up does metal and the Fermi level of the semiconductor were already exactly equal at equal position or they were exactly aligned when before you join them. So, after you join them, they stayed aligned as it is and the bands were flat, this is called flat band condition and this flat band condition happened at V_G equal to 0. Because even before I applied any voltage on the gate, the

bands were already flat. This is called flat band condition and this flat band condition will come at 0 voltage in this situation, ok. So, at 0 volt for example, as when I apply 0 volt, this is a flat band condition.

The bands are all flat because the Fermi level was already aligned. In other words, the metal from if the metal semiconductor work function difference was 0. So, the Fermi levels are exactly already in aligned place. So, this is 0 volt. So, if you look at the capacitance voltage curve here carefully at 0 volt, this is the flat band voltage, you see at 0 volt, there is a capacitance which is not exactly equal to the oxide capacitance. This is the oxide capacitance, it slightly lower than the oxide capacitance at 0 voltage on the gate.

In other words you can say this is the flat band voltage which is 0, you will eventually see that this flat band voltage need not be 0. Because if the metal and semiconductor work function difference was not the same, was not 0, then as soon as you join the, as soon as you join the metal and semiconductor, they will not be flat. They will be tilted, the bands will be bent because the Fermi level has to come down; you remember metal Schottky junction, the same thing; will come to that you know very quickly.

So, at 0 voltage, you have a flat band capacitance and this value is not exactly 1 or this is not value exactly oxide capacitance. What happens is that, when you have a flat band condition like this, when you have flat band condition like this, a small signal that you are applying on the gate will be able to modulate a small charge here, there is no depletion per say this, there is no depletion here, but there is a small depth to which the small signal can modulate the charge; a small depth until which your small signal can modulate the charge. Do you know what it is called? the small depth up to which you can modulate, that is called Debye length, Debye length, and that is given by L_D.

So, basically when you apply a small signal at the gate, you are able to modulate a small area in the semiconductor, that depth of that area is called L_D or the Debye length and that Debye length expression, you know if you remember, the Debye length expression is given by square root of I think q^2 kT sorry; it is not q^2 kT, it is ξ semiconductor KT by q square times the doping, that is the value ok.

$$L_D = \frac{\xi_s kT}{q^2 N_A}$$

If your doping is high, then the Debye length also a small. Essentially, Debye length gives you an idea of what is the depth in the semiconductor to which you know you can modulate the charge if you are applying a, if you are applying a small signal on the gate. So, that Debye length also tells you that the minimum this is the minimum length over which your capacitance voltage profiling technique will be accurate or reliable.

So, that Debye length will be very small and that will give you a capacitance, a corresponding to Debye length, you know, that will give you a Debye length capacitance so the capacitance with respect to the Debye length when you have a small and this is not inversion, this is not accumulation; this is just at flat band.

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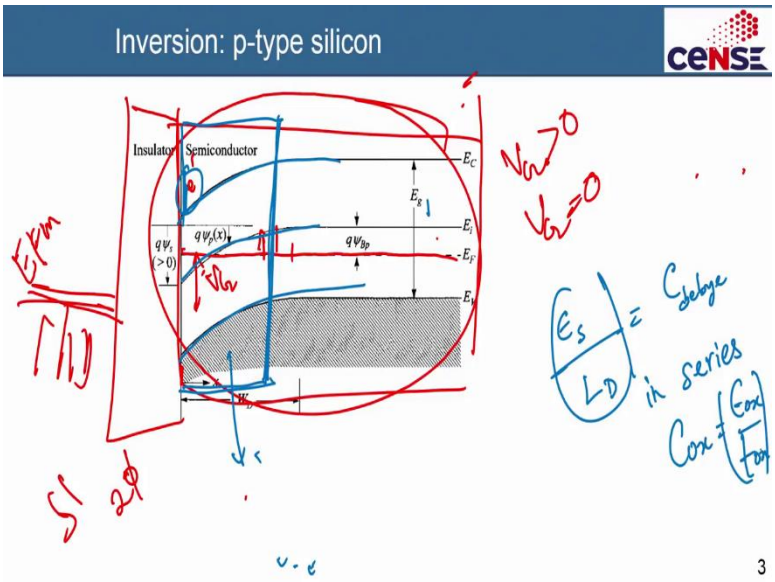

So, that the Debye capacitance will be given by ξ_S/L_D; this is your Debye capacitance ok. This Debye capacitance will be in series with oxide capacitance C_{ox} which is equal to ξ_{ox}/t_{ox}. So, both of this series combination will give you, both of the series combination will give you this; your Debye, your flat band capacitance. This is actually nothing but the series combination of oxide in series with the Debye capacitance, ok.

The Debye capacitance comes because you are able to modulate a small width in a semiconductor here by applying a gate voltage here; it is not accumulation, it is not inversion, it is just a Debye capacitance. So, that comes there. Now though we have to do a little bit of mathematics very small amount of mathematics, but before that I would like to tell you that if your metal and semiconductor work function is not, if your metal and

semiconductor work function is not 0, then you are not going to get all these things, there will the flat band voltage will be different, the flat band voltage will be different. So, for example, let me do that, I will give you a new slide here may be.

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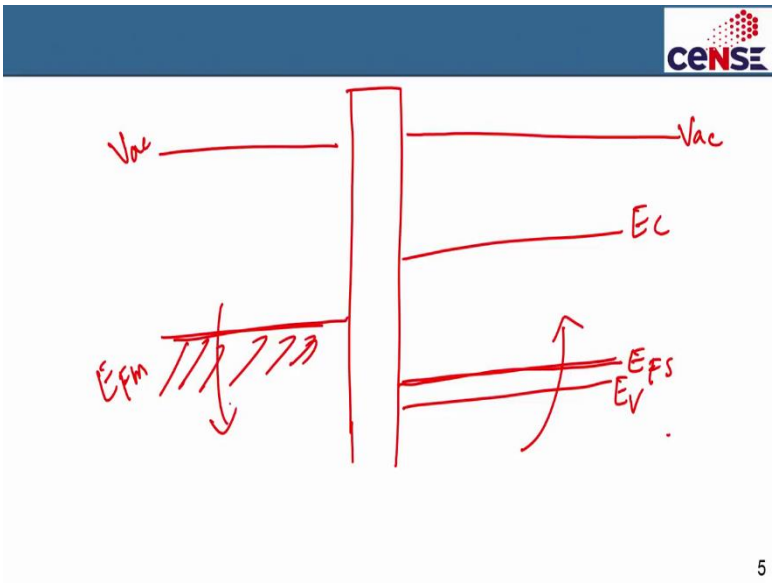

So, for example, suppose you have the vacuum level here and the metal Fermi, Fermi level is here E_{Fm}, but now the semi, this is the dielectric here this is a dielectric here. Now the semiconductor initially the semiconductor I told you the semiconductor Fermi level is also exactly here. When you align them, it basically forms like this ok. It is a flat band condition, but that is an ideal situation, really does, in realistic situation, it does not happen like that.

Realistically, what will happen is that, if this is the flat, this is the vacuum level, your you know your semiconductor Fermi level will be different for example, suppose your semiconductor Fermi level is here p type right. So, suppose your semiconductor Fermi level is here. This is a semiconductor Fermi level, this is the semiconductor valence band, this semiconductor conduction band here ok.

So, then if you, if you join them together, this is not equilibrium, if you join them together, the semiconductor Fermi level has to align with the metal Fermi level which means this has to come up, this has to come down in a way right, this is to come up this is to come down in a way. So, what will happen is that the band diagram in equilibrium, in equilibrium at V_G is equal to 0 will be that you will have the Fermi level aligned here ok

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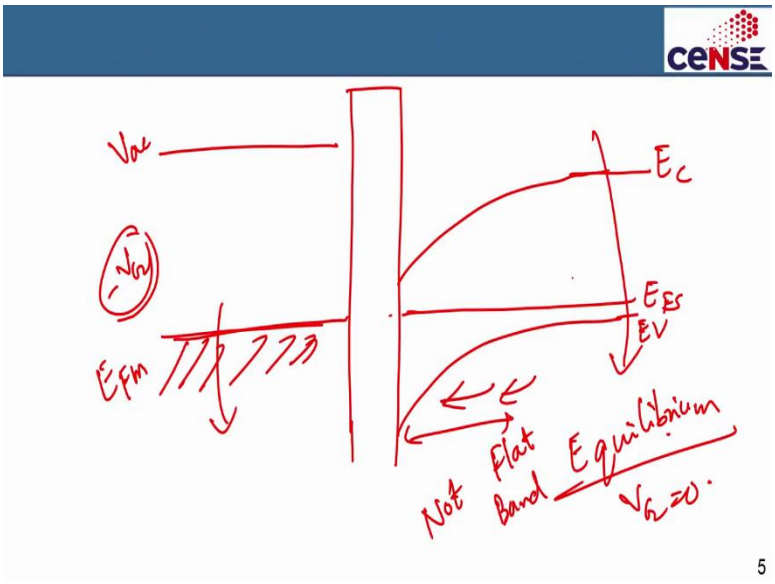

The valence band, the conduction band far away will be basically the same as before, except that it will, it will be something like this. You see this is equilibrium, this is equilibrium, this is equilibrium, and this will be your V_G equal to 0 ok. This is what the band looks like that, this is not a flat band condition. This is not a flat band condition ok. To make the bands flat you have to apply an additional voltage here, what you will have to do? You essentially have to apply a negative voltage on the, you have to apply a negative, because this part is depleted of holes.

So, you have to apply a negative voltage here, a negative voltage here so that you attract holes this side and you basically bend, you basically, when you apply negative voltage here, you essentially are trying to push it down here so that the bands become flat ok. The bands will become flat. So, when you apply an appropriate negative voltage and the negative voltage that you have to apply to make sure the bands are now flat will be equal to the metal semiconductor work function difference.

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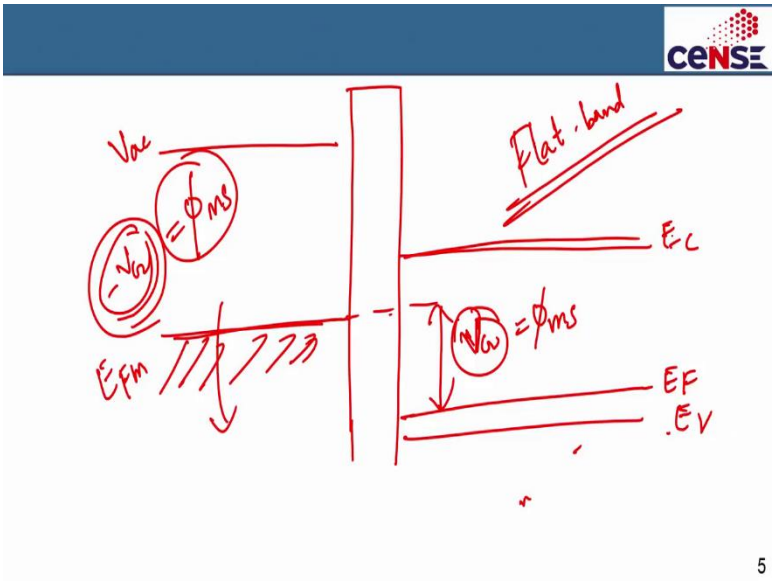

Only in that case the bands will be flat, so, will push it down right. So, eventually what will happen is that, it will have, if you apply negative voltage on the gate, it will look like E_C, E_V, this is your Fermi level and this gap between the Fermi level, the Fermi level between the metal and a Fermi level the semiconductor, this will be the V_G that you are applying, as a negative voltage that you are applying which is equal to φ_{ms}, the metal semiconductor work function difference, you have to apply to make sure that the, this is called flat band condition.

So, this flat band condition is very important. Initially we assume that the metal semiconductor work function of the difference is 0. So, the flat band was there, but actually in reality you might have to do something, either apply a negative voltage or positive voltage depending on the band diagram to make sure that the bands are flat, to make sure that the bands are flat. So, let us stop for today's lecture here.

So, we have discussed the capacitance voltage profiling. We have qualitatively understand or tried to understand the C-V, the different regions of the C-V, the accumulation, the weak inversion, the strong inversion. We have not started mathematics yet; there is no equation till now. We are only trying to understand quant qualitatively physically what is happening; when I apply small voltage on the gate, how is the charge modulating and what is the depletion region, what is the inversion charge, how are they responding? Based on that we try to understand the capacitance voltage curve. And this is of most importance in

the most paramount importance. This capacitance voltage curve in many of your exams, in many of your interviews, it is important to understand MOSFET. So, this is very important. So, till now we have not started any equation ok. We have just written down, we have just had to understand qualitatively what is going to happen. I told you about the flat band condition, Debye length and so on.

So, in the next class we will write some simple equations, we will write some simple equations and try to see how we can quantitatively define the capacitance voltage profiling ok. And once we do that we will discuss some real capacitance problem like there will be oxide charges and interface charges that will shift the capacitance values. So, those things we will consider and then after one or two lectures I guess, we can start MOSFET after that. So, we will wrap up the class here today.

Thank you for your time.