Fundamentals of Semiconductor Devices
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Lecture – 30
MOS: Introduction

Welcome. So, we have finished BJT, now we will go to a different kind of transistor which is the most common, the classical device, any semiconductor device textbook will talk about, which is called MOSFET, M O S F E T this is a metal oxide semiconductor field effect transistor. MOSFETS are the most common transistors in the world that enable your logic memory devices, your laptops, computers, cell phones they all have processes memory devices mostly it is CMOS devices which are based on MOSFET. So, it is very important for us to understand MOSFET thoroughly, at least to a first order, we should be able to understand how MOSFETS work.

So, we will today start a new topic, and everything that you have learned till now will be used in understanding these devices. A MOSFET the fundamental building block of a MOSFET is a MOS capacitor, metal oxide semiconductor. If you have a semiconductor, on top of that you have an oxide or a dielectric, on top of that you have a metal, it is called metal oxide semiconductor system; MOS. It is not a transistor yet, it is just a metal oxide semiconductor capacitor. So the MOS, M O S capacitor is the first thing that we have to learn to understand MOSFET.

So, today we will start to understand, you know in the next couple of lectures, we will try to understand how metal oxide semiconductor capacitors work and how we can understand their basics, ok. So, we will go step by step, whatever we have learned till now in a band diagram, conduction band, valence band everything will be very important. And it is assumed that you understand all of those very clearly, because MOS capacitor will depend heavily on those, ok. So, will come to slides today.

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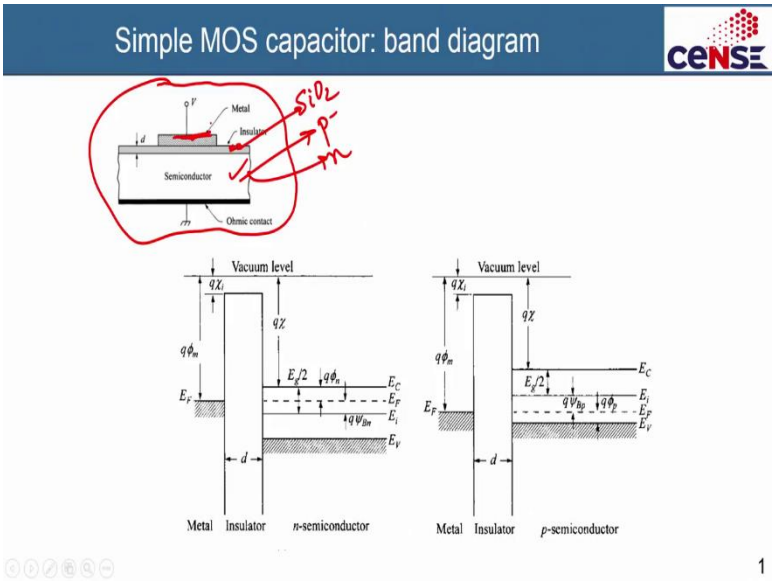

So, let us come to slide here. You will see, this is what am showing you in the slide. Let us not get very disturbed or perturb, let us go step by step. This is the schematic of a metal oxide semiconductor. So, you see the top you have a metal here, this is the metal, this is an oxide semiconductor, oh, sorry it is an oxide like an insulator, ok. And this is the semiconductor. This semiconductor can be p type doped or this can be n type doped whatever, ok. And this insulator that is there, it is an oxide typically it is a silicon dioxide. And this is the metal that you can put, aluminum, nickel, whatever you know. So, this is your, this is your essentially metal oxide semiconductor system.

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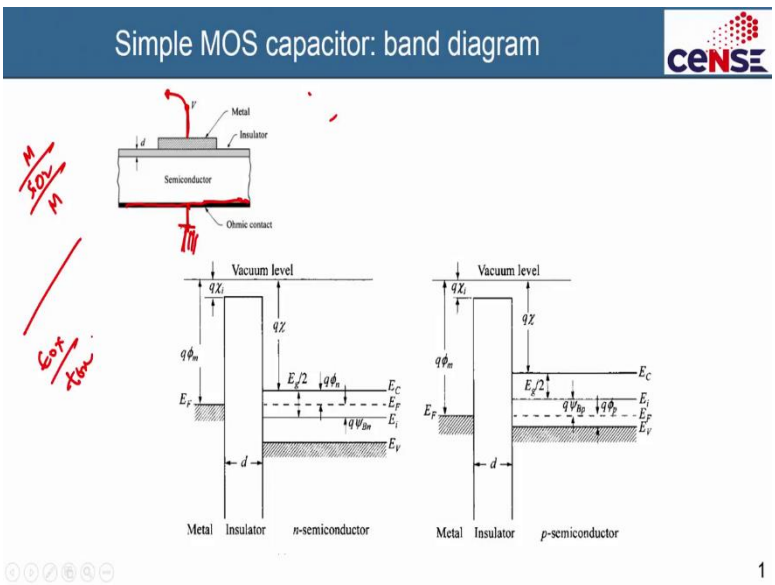

So, the idea is that you apply a voltage to the metal here, you can see the voltage is applied here and there is an ohmic contact with the semiconductor. An ohmic contact to semiconductor which is grounded, it is ground.

So, the idea is that, this is a capacitance system, because there is a metal, there is a semiconductor and there is a oxide layer there, ok. If it was a metal semiconductor, if it was a metal oxide and again metal, ok. So, this is silicon dioxide, this is metal, then capacitance will be flat, because that will be given by the thickness of the oxide;

$$\frac{\xi_{ox}}{t_{ox}}$$

that is the capacitance. But here it is not like that, because the semiconductor will have some funny things that going on, ok, that will be going on, because semiconductor can deplete for example. So, now the question is on the metal if you apply a voltage, how will this whole thing behave?

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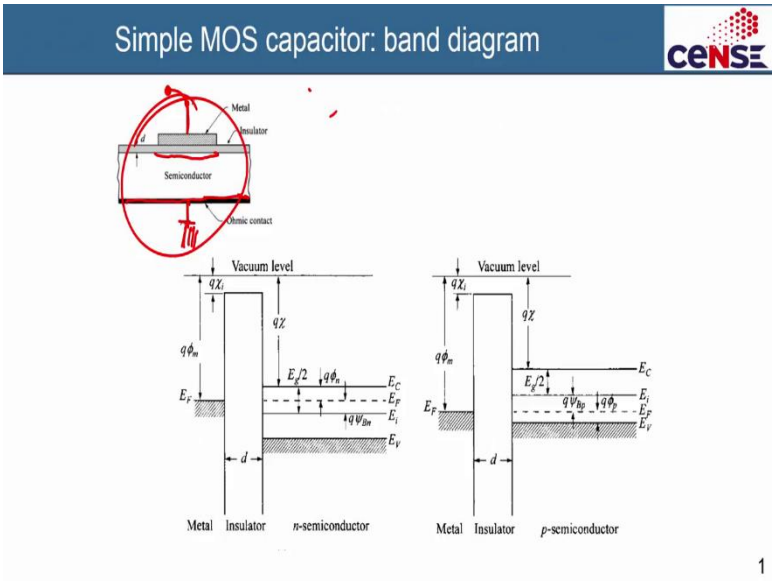

You know depending on the voltage applied there might be a depletion here, ok. So, that things are very important in understanding the MOS capacitor. So, let us not worry so much about it, but this is the schematic that we have. So, now, we will come to energy band diagram. Let us not get very disturbed looking at things initially.

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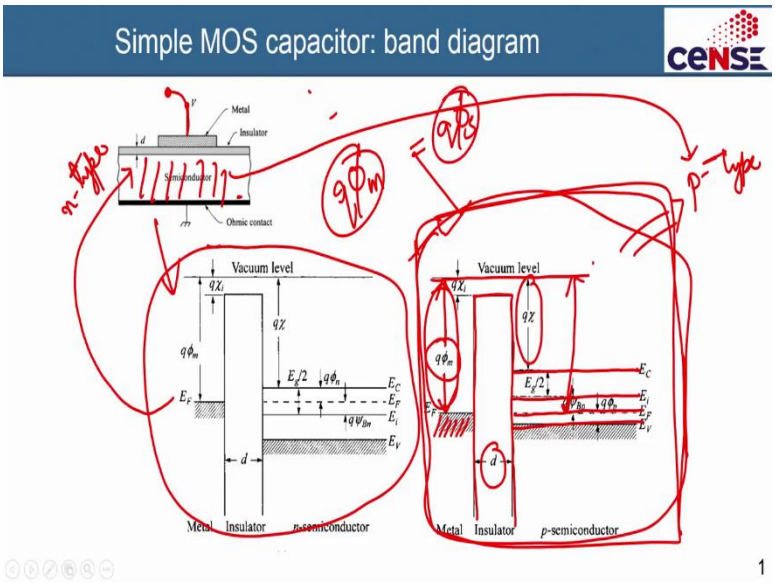

These are two energy band diagrams of metal oxide semiconductor system. We will come to the energy band diagram very clearly, this for p type semiconductor. If this semiconductor is p type, then this will hold true and this band diagram will hold true if this is an n type doped semiconductor, this will be then n type doped semiconductor. So, you are essentially, this semiconductor can be added p type or n type. So, if it is p type, it is this, if it is n type, it is this; that is what it means. So, let us look about this, if the semiconductor is p type. Why you will? It will become clear little bit later, it can be either way, but we will focus on semiconductor that is p type, semiconductor to this p type.

If you look carefully now, there is always a vacuum level, ok. This is the band diagram, the energy band gap of dielectric which is very large, ok. This is the dielectric oxide, it has a thickness of d that is oxide and is very large. This is metal Fermi level and vacuum level to metal Fermi level, this is the metal work function. $q\varphi_m$ this is the metal work function, ok.

Then this is the semiconductor the conduction band is here, the valence band is here, the intrinsic level E_i is mid gap that you know, and the Fermi level is close to the valence band, why? Because it is p type doped. In a p type doped semiconductor, the Fermi level will be close to valence band. So, that is why the Fermi level is close to the valence band, ok. The assumption is that, ok. The assumption is that when you join this system, when you make the system the metal work function, this one is exactly equal to the semiconductor work

function; this is the electron affinity, and this is the work function to vacuum level to the Fermi level.

So, the assumption is that the metal work function φ_m will be equal to semiconductor work function, so that when you join the metal and the semiconductor with the dielectric in between, the Fermi level will be aligned. So, if you can see again clearly, ok, if you see very clearly, your metal Fermi level is aligned to the semiconductor Fermi level. There is no band bending.

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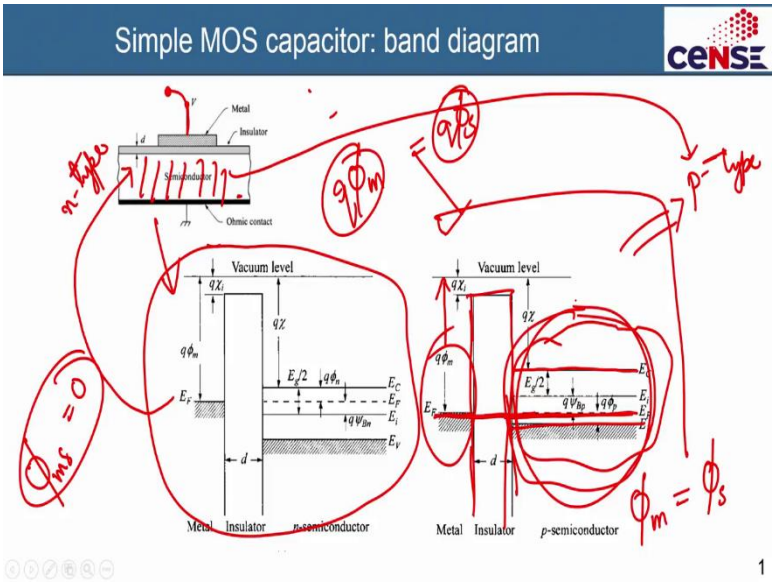

In equilibrium, everything is flat, this is flat, this is flat, which means the metal some Fermi level and the semiconductor Fermi level were already aligned before joining the system, before the system was formed.

So, the metal Fermi level and the semiconductor Fermi level are at the same level, after joining also, they are at the same level and the bands have not moved, the bands have stayed flat. So, this is the assumption that metal Fermi level, the metal work function and the semiconductor work function is same. In other words, the semiconductor metal work function difference is 0, in which case the Fermi level in the metal side and the Fermi level on the semiconductor side are aligned even before you join the semiconductor and the metal.

So, even after joining, they are flat; everything is flat. So, this is the dielectric that is there in between, ok. This is the dielectric in that is in between, ok, this is the metal Fermi level, this is the semiconductor side, this is the n-type semiconductor side. So, when you form a junction, it looks like this. Now it is very important to look at different numbers that are given here, different notations that are given here. Of course your E_C - E_i will be half of band gap which is given here right, because the E_i is the middle of the band gap.

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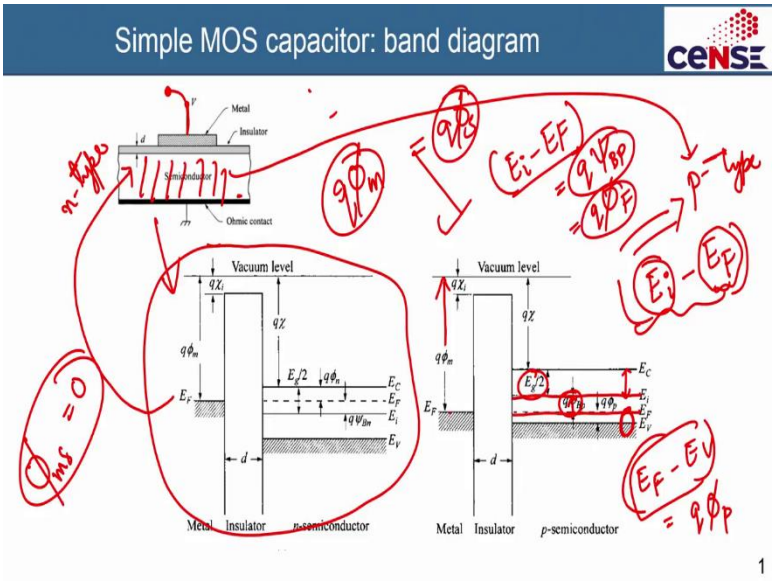

Now this difference between E_F - E_V, you see, that difference tells you how much holes are there, that is referred to as, $q\varphi_p$, that is, that is the basically the gap between the Fermi level and the valence band on the bulk of the p semiconductor and then this gap, it is very important that gap essentially is E_i, the mid gap minus the E_F, the Fermi level, how below is the Fermi level from the intrinsic level. You have an intrinsic level here; compared to the intrinsic level, how below is the Fermi level, ok. Please remember that.

That gap, this gap E_i - E_F how far below the intrinsic level is the Fermi gap, it is called $q\psi_{BP}$, but I can also give a different name, it is just a nomenclature, different textbooks use different nomenclatures to look make it look better, I will call it $q\varphi_F$, ok. You can also call it ψ_{BP}, but I will just call it φ_F, because that is how I will be using in the equation.

So, let us see again, look at this band diagram very carefully, ok. Look at this band diagram very carefully. Let me choose a different color maybe.

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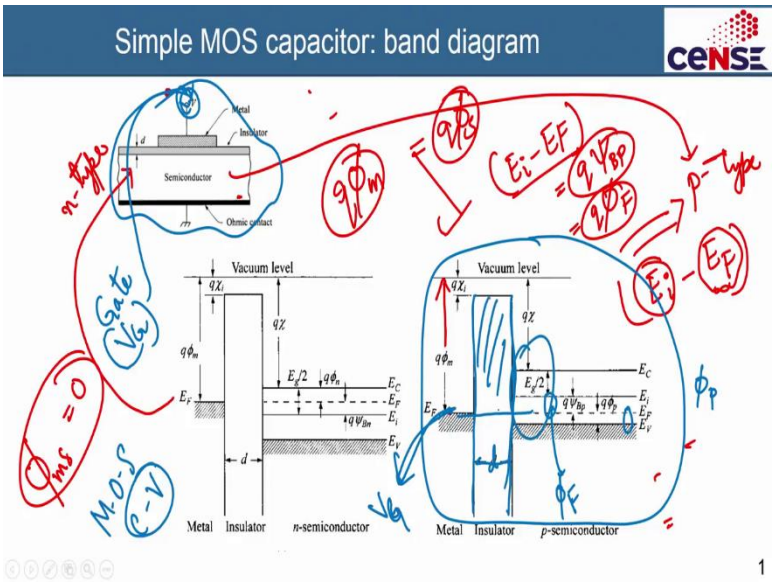

You see, this is just a schematic of a metal semiconductor, metal oxide semiconductor and this is the band diagram at equilibrium. When the metal semiconductor and oxides are all joined together and the metal and the semiconductor work functions were equal even before, they were always equals. So, after joining also they are equal, that is what it means, ok. Now you see carefully these different terms repeat please, ok. The Fermi level and the valence band difference is called φ_P. The intrinsic level and the Fermi level difference, I will call it φ_F.

And the Fermi level is aligned, nothing happens. The thickness of the oxide is "d". So, what is it that we have to study now. What we have to study is when I apply voltage on the gate, when I apply a voltage on the gate, I call it VG that I apply here, right. So, here, if I apply a voltage VG on the gate, either positive or negative, how will the band diagram look like and what will happen? That is what we have to study. That will give you, this is a system is MOS, metal oxide semiconductor, that will give you the capacitance-voltage characteristics.

How will the capacitance of the system vary with respect to voltage that you apply on the gate? See this insulator is very-very good actually. So, we will assume that there is no leakage current through this oxide, it is completely insulating, there is only a field, it will apply be applied from the metal that will basically change the band diagram on this side, but there is nothing that will leak through the oxide, that is the assumption.

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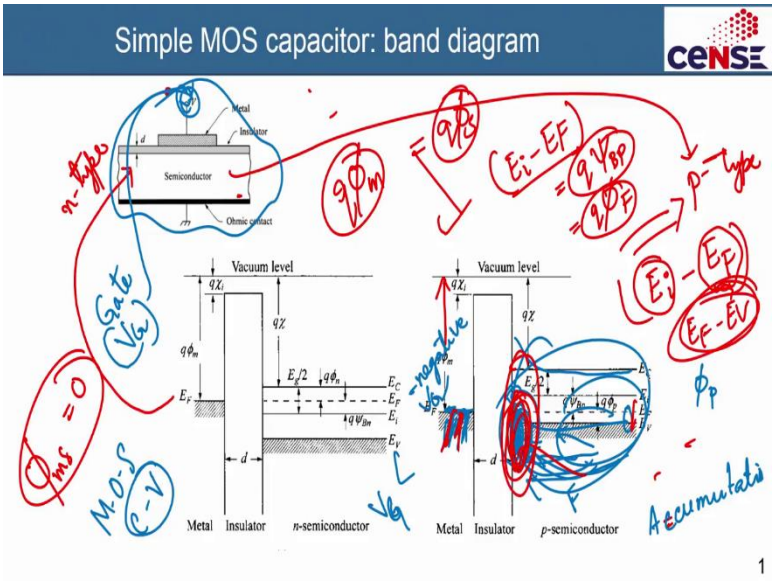

Now, if you look very carefully, if I apply a negative voltage on the gate. If I apply a negative gate voltage, then what will happen is that, intuitively speaking or logically speaking, if I am applying a negative voltage and again and this is p type, so, there are holes there so, the holes will get attracted towards the negative voltage that I am applying.

So, more holes will try to come and accumulate near the interface here. The holes will try to come and accumulate near the interface, because I am applying a negative charge. So, holes will all come and try to dump here, ok. So, the bands will band upward, what I mean is that the bands will band upward like this. When a holes will come here and accumulate and dump here, we call that accumulation, we call that accumulation.

And in accumulation there will be more holes at this point than there will be holes at this point, which means, see, at you know, if you have more holes. then your Fermi level and valence band gap should decrease, which means at this point when you are attracting more holes because of a negative bias, there will be more holes at the surface. So, at this surface, the Fermi level and the valence band difference should be less compared to the difference here. Are you seeing my point, it will, the bands will have to band up like this.

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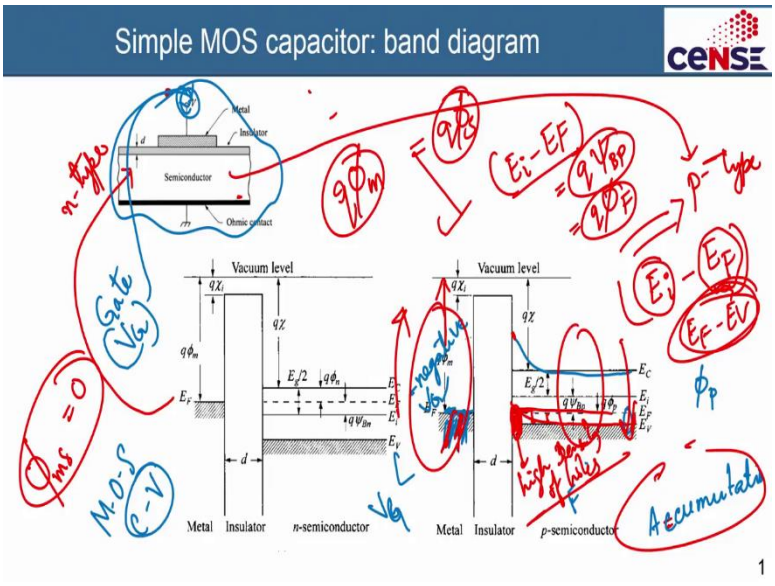

So, the Fermi level and the valence band difference has to reduce and eventually, it will be almost there; There will be a very high density of holes here, very high density of holes here, ok. And that will be called accumulation, there is an accumulation of holes here ok, right. There will be an accumulation of holes here. So, and because in general if you apply negative voltage, this side if you apply negative voltage this will try to move up the band this side, it will try to move down the band. So, you will have a band diagram like, you know, this bands will if you try to push this down.

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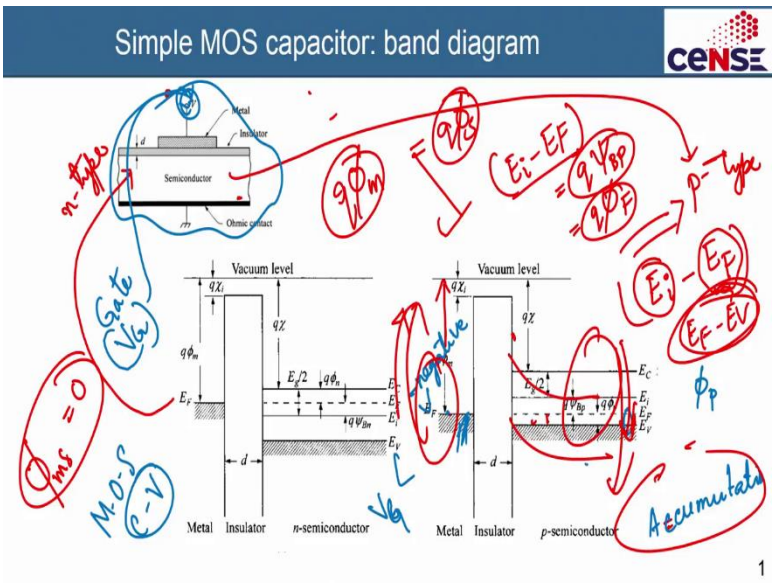

If you try to push this up, then the band will look like this, but eventually the Fermi levels have to align. The Fermi levels have to align, because, no they will not be aligned sorry. The Fermi levels will be separated by a spacing which is given by the gate voltage that you apply, but there will be no current flowing through the oxide.

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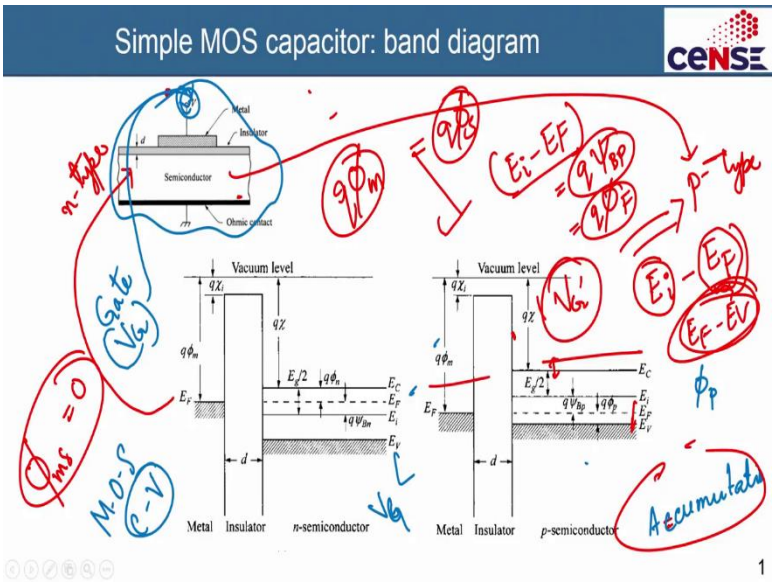

So, the Fermi level, the quasi Fermi level on both side will be flat, but there will be gap in the difference in the Fermi level that will be given by the gate voltage. So, what I am trying to say by that?

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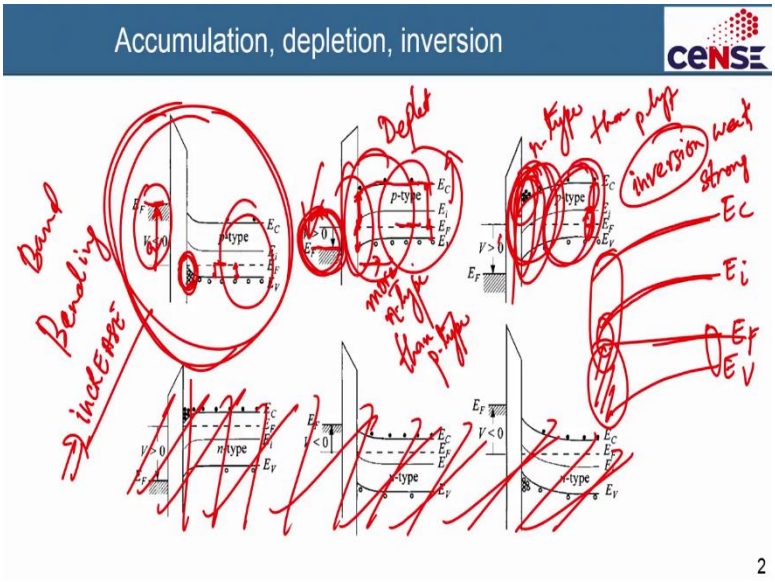

So, this is what I will say, forget about this, because these are we, these are important as much important, but will only talk about when the substrate is p type doped, when the substrate is p type doped. There are three conditions, there is accumulation, there is depletion, weak inversion and strong inversion. These are the terms that might seem to be a little bit unfamiliar to you, but these are very easy to understand actually. So, this is what I was talking about in accumulation.

If I apply a negative voltage to the gate, holes will be attracted and say there will be more holes here. You see there are more holes that are accumulating there. So, the bands will bend up, you see the Fermi level and the valence band difference, that will keep reducing and eventually it will almost become, Fermi level and valence band will almost become merged, because the hole density is now very high. So, the Fermi level has to come closer to the valence band. And this Fermi level of the metal and this Fermi level of semiconductor, these are separated by this gate voltage that you are applying, ok. There will be a large number of holes here, ok.

In the other case, when you apply a small positive voltage on the gate, because this is holes in the p type, this positive voltage will repel away the holes. So, near the surface, the holes will be pushed away and you create a depletion region here, you create a depletion region here, because you are pushing away the holes because of the positive bias or you can say that positive bias pushes this bands down, ok. And then pushes these bands up, ok. So, that is why there is a curvature like this, like this, like this.

So, essentially what is happening is that it is becoming less and less p type, because at the interface, far away from the junction nothing is changing, far away from the junction nothing is changing, but at the interface, if you look carefully at the interface, you are actually pushing away holes. So, there is a depletion here, the bands are bending. So, there is a depletion here, there will be fewer holes here than the bulk.

Bulk has very high holes as you have doped, but this part will be depleted, because the holes are being pushed away, bands are bending downward, ok. Fermi levels will of course, not be aligned, the metal from function is here, the semiconductor function is here. The difference is the positive voltage that you are applying, but you see as you are depleting this area the, the, the Fermi level is flat of course, but the conduction band of course, is very far away from the Fermi level.

The valence band is very close to the Fermi level, but close to the interface, the conduction band is coming closer to the Fermi level and the valence band is moving away from the Fermi level, right. So, because the conduction band is coming closer to the Fermi level or intrinsic band, you will, you are trying to get more n type, this surface is becoming more n type. This surface is becoming more n type than the background p type, ok. This is a background p type, but here, if you look carefully, this is the Fermi level and this is the intrinsic level, ok.

This is the conduction band and this is the valence band. Initially, valence band and Fermi level are very close, because there is p type doped, but at the surface, the valence band and Fermi level this gap has increased, which means it has become less p type doped, because the holes are being repelled away, there is a depletion.

Additionally, the intrinsic Fermi level is approaching the Fermi level, this gap is very small and the conduction band also is approaching the Fermi level which means it is starting to become more n type, but of course, the n type nature has not become very strong, but if you apply a very high positive voltage here on the gate, you are bending this further. That band bending, the band bending, the band bending will increase; the band bending will increase.

You are applying a more positive bias, so, the band bending will increase like that. And what will happen is that, you see there will be more and more, you know E_C, the conduction band is becoming very close to the Fermi level. The valence band is now moved away from the Fermi level at the interface, the intrinsic level E_i has actually crossed or touched the Fermi level now.

So, which means the Fermi level now is in the top half rather than on the below half of the semiconductor. You see in the faraway junction; in the faraway junction, the Fermi level is in the bottom half, this is the bottom half, this is the top half. Fermi level with in the bottom half which means it is p type doped, but when you have a very high positive voltage on the gate, you see the Fermi level is in the top half actually, this is the Fermi level, this in the top half which and this is not in the bottom half, which means it is more n type, it is starting to get more n type than it is p type, ok. There will be more electrons here, because you are bending the bands in this way.

So, this is called inversion, it has basically the inverted the channel, it has inverted the channel and form electrons at the interface although the substrate is p type doped. Although you are depleting the carriers from the substrate and you are making this depleted, the depletion is there, but at the same time because of higher positive voltage, you are going to get more electrons at this interface, because of the band bending and you are getting something called inversion.

So, the channel is now formed, or you can say the semiconductor is now inverted from p type to having electrons at the top interface here; that is called inversion that has happened, this is accumulation, and this is depletion, ok. Now this inversion can be also weak inversion, or this can be strong inversion. In weak inversion, it is just barely bending but in strong inversion, it will have a very high density of electrons at the surface compared to the bulk, ok. The same thing actually applies to n type semiconductor also, except that we are not discussing it here, but it also applies to semi n type semiconductor.

So, depending in, the polarity will be changed here. In an n type semiconductor, at negative voltage on the gate, you will be getting inversion eventually, ok. So, that is something that we can keep in mind, but not very- very critical thing, I mean once we can, once you understand p type, we can understand n type also.

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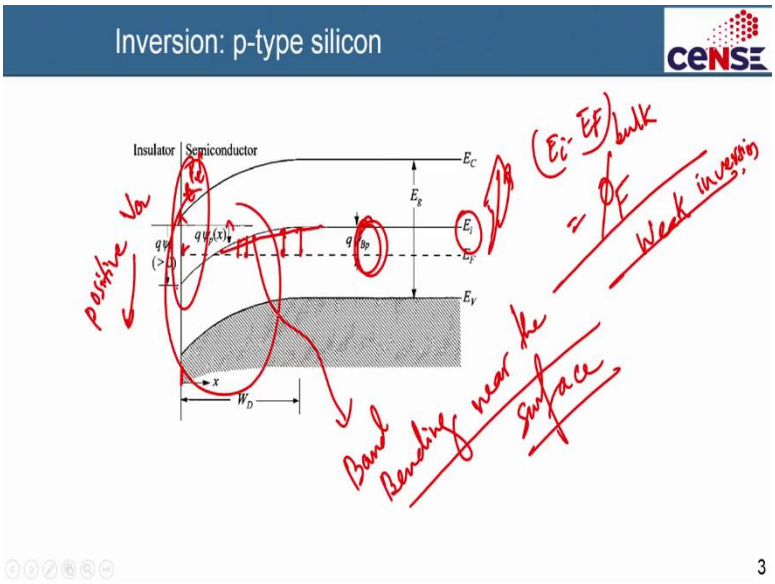

So, now we will spend some time on looking at the band diagram where you are inverting the channel. So, let us look again, you have a Fermi level which is flat, this the Fermi level,

right. This is the Fermi level, the Fermi level is flat, because there is no motion of current here, ok. Although this is displaced by the gate voltage, ok. You are trying to bend the band diagram like this, because you are applying a positive voltage on the gate, a positive voltage on the gate, pushing it down, pushing it up.

So, essentially you are getting a band like this. Your intrinsic Fermi level which is the mid gap is also bending and you see, the Fermi level is now in the top half. So, it has become more n type not in this bottom half. So, it has not become it is not, it will have electrons rather than holes, although the semiconductors p type doped in the bulk, ok. Everywhere it is the uniform doping. So, one of the most important characteristics of this MOS, this band diagram is that, what is the band that you are having here. What is the band that you having here? This is the band, right. What is the band that you are having here? You are having a band bending at the surface near the surface, right. This is band and band is bending near the surface.

So, the band is bending near the surface. So, this measure, this quantity gives you how much band bending is happening at any point x, ok, at the surface at this point x equals 0, the band bending is the max, the band bending is the max and electrons are appearing here, starting to appear here, because the conduction band is now closer to the Fermi level than the Fermi level is closer to the conduction valence band, it is now getting n type, right. This quantity is very important quantity that is called E_i - E_F in the bulk. This is defined in the bulk of the semiconductor, like how far below intrinsic level is the Fermi level in a p type semiconductor. I call this quantity as φ_F.

They are calling it ψ_{BP}, but it is the same thing. This is the φ_F, that gap reduces eventually, becomes 0 and goes to negative almost on the other side. What it means is that, that gap tells you how much it is p type, ok. And since as the gap the Fermi level is staying flat, but the gap is reducing here it means, it is becoming less and less p type, it is becoming more and more n type, eventually its bending beyond that. So, this is strong inversion, now this is inversion, sorry, when this particular part has electrons that itself is called inversion.

So, first we have weak inversion, first we have weak inversion. What weak inversion means is that this bending has such that at the surface, this is not, this particular figure is not in a weak inversion, but weak inversion is when this band bending is such that this comes and reaches the surface here. The intrinsic Fermi level E_i will be bending and

eventually it will at the surface, it will be mid gap. So, essentially, you are, it is going below that. So, you are getting now electrons here and below that, that is the onset of weak inversion, below that you have weak inversion. So, this is a weak inversion situation for example.

So, as soon as this E_i, the intrinsic level reaches the mid gap, we say this is the onset of weak inversion and after that, its weak inversion until it reaches strong inversion and at inversion, you will have electrons here. At weak inversion, you will have fewer electrons, at strong inversion, you will have a large number of electrons the, because the bands have bent large.

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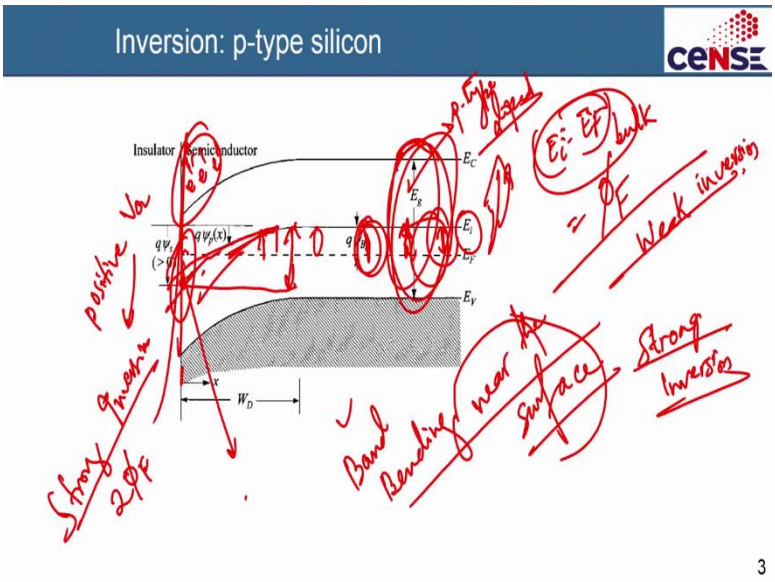

So, when will strong inversion happen? Strong inversion will happen when this band below this line, the band below this point, this point, is equal to this, which means the intrinsic level E_i is as much above the Fermi level in the bulk as it is below the Fermi level on the surface, that is called strong inversion.

If you recall again, strong inversion is defined when the Fermi level and the intrinsic level difference here, if you see in the bulk, is exactly the same difference that you see on the surface, but in the opposite direction, like the Fermi level is now on the top of induction, the intrinsic level, Fermi level here is below the intrinsic level. What it means is that, the number of electrons at the surface which is increasing, number of electrons at the surface is exactly equal in density to the number of holes in the bulk.

So, this material is p type doped; this material is p type doped. In a p type doped material, how many holes are there? Density, the hole density that is exactly the same as the electron density on the surface, because the bands are bending and inversion is being formed, that is called strong inversion.

So, in strong inversion, the band bending, the total band bending that is happening is actually from this point to this point, right. This is the total band bending that is happening. In strong inversion, in strong inversion, your total band bending will be equal to this which is this plus the same amount. It will be equal to 2 times φ_F. Are you getting my point? φ_F is this E, E_i - E_F. So, essentially, that difference between Fermi level and intrinsic level in the bulk is exactly the same as the difference between the intrinsic level and the Fermi level on the surface, but flipped, the sequence is flipped.

So, the index, intrinsic level, not induction, intrinsic level is above the Fermi level here, sorry below the Fermi level here, intrinsic level is above the Fermi level here. So, in a way, this has as many electrons per unit area as this has holes per unit area, ok. So, that you have to consider. So, in that case, you are saying that you know, we can say that strong inversion has taken place and there are large number electrons that have come here, ok.

So, you will get, although the semiconductor is p type doped, you will get a large number of electrons at the surface here, because of band bending, this is called strong inversion. And now, after we have considered the strong inversion and the weak inversion and all these things, we can derive the mathematics of everything that we have discussed and shown till now.

So, in depletion, in accumulation, in, you know, in weak inversion strong inversion, you can define the expression for the different, different parameters like you know band bending and all these things and we can solve Poisson equation and whatever equations are there to essentially come up with a quantitative model of this band bending and various expressions associated with it.

So, you know, we have accumulation. If you look in the previous slide again, we have accumulation, we have depletion, we have inversion. First, we have weak inversion and then, we have strong inversion; first we have weak inversion, then we have strong inversion. So, this is a picture that is to show the bands and all those things.

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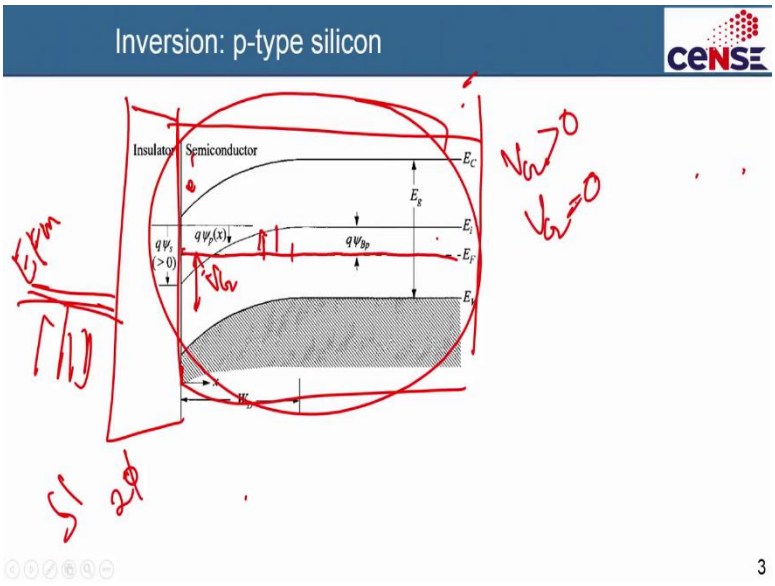

Now, we shall basically start this is a looking this looks like a very scary figure, but actually is not. So, we will basically now start looking at the capacitance voltage characteristics of this particular junction, this is insulated, right here, ok. There is a insulator here and then, there is a metal here. There is a metal here, metal and the metal Fermi function is here. Semiconductor Fermi function is here, the gap is the VG that you are applying. So, how will the capacitance of this system look? For example, if I look at this, if I apply voltage here and this is grounded and how will the capacitance look.

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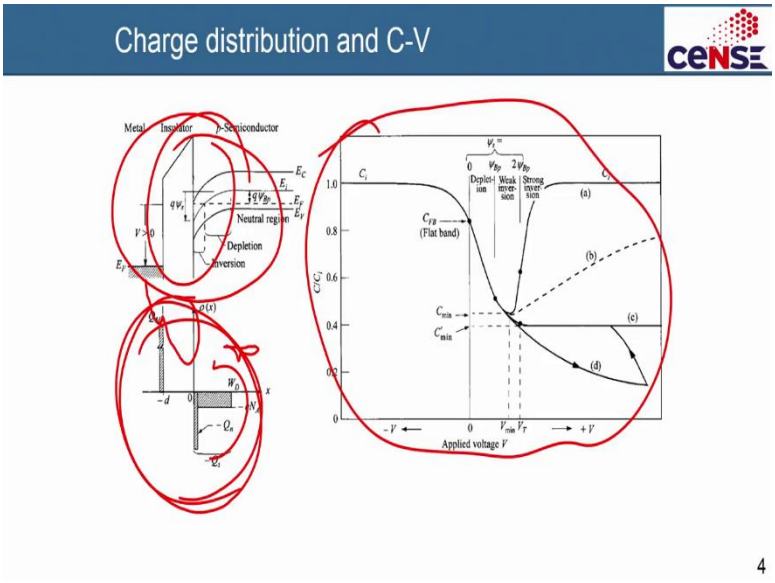

So, the capacitance will actually look like this, which is a very weird kind of figure. but there will be different regions of depletion, weak inversion, accumulation and inversion and so on. It will take some time, but still we will do that. So, if you look carefully, everything that we need to know for the capacitance will come from this diagram. So, this is only when $V_G > 0$, ok. Large, much greater than 0. At $V_G = 0$, you will have a figure like this which is flat band. At V_G equal to negative voltage, you will have a figure like this, ok this where you have accumulation of holes.

Now we have to understand the capacitance in terms of the charge, where is the charge stored? what is the charge profile? And how will the capacitance change with the charge profile? That is what we have to learn now. So, let us wrap up for today. And in the next class we shall start from the capacitance voltage characteristics of a MOS capacitor.

We will distribute the charges, we will come to understand the charges and how the band diagram will correspond to different charges that are here. And based on these charges in the band diagram, we will be able to understand how actually the capacitance voltage characteristic change in a silicon MOS capacitor because there will be very many exciting and interesting features which you should keep in mind and you should be aware of. So, in the next class, we will start with MOS capacitor again, the band diagram and the charges and how different parts of capacitance voltage curve correspond to accumulation, depletion, strong inversion and so on.

And everywhere, we shall have to keep the band diagram in mind, the charge distribution in mind. Whatever we have learned in today's class is just an introduction to the schematic of MOS capacitor, the various regions of operation depending on the gate bias, whether it is positively biased or negatively biased, you can either get more holes or fewer holes at the surface, we call it accumulation or depletion. Go to more depletion, we will eventually hit inversion where the Fermi level on the surface is closer to the conduction band than in the bulk, so that means, that the surface you will get more electrons than what is actually expected. And in very strong inversion, the number of electrons at the surface will be equal to the number of holes in the bulk, as many holes, ok. So, that part we have cleared till now.

So, let us meet in the next class. We will start from the MOS capacitor, band diagram and the charge distribution together, ok. So, we will see in the next class. In the meantime, you should please revise this MOS capacitance again; the two very good books, one book is called MS Tyagi and one book is by SM Zee, both are very good books to study. Many of the figures that I am showing you here are from SM Zee's book, ok. So, will meet in the next class.

Thank you.