Semiconductor Devices and Circuits
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Lecture – 55
Tutorials Session -3

Hello, I am Oppili Prasad serving as teaching assistant along with mister Prasenjith for the Semiconductor Devices and Circuits course. So, in the earlier tutorial session, you would have solved many problems from various topics from this course. So, in the session, we will continue with a few more problems relating to topics like MOS CV characteristics, MOSFET and also some other problem from circuits.

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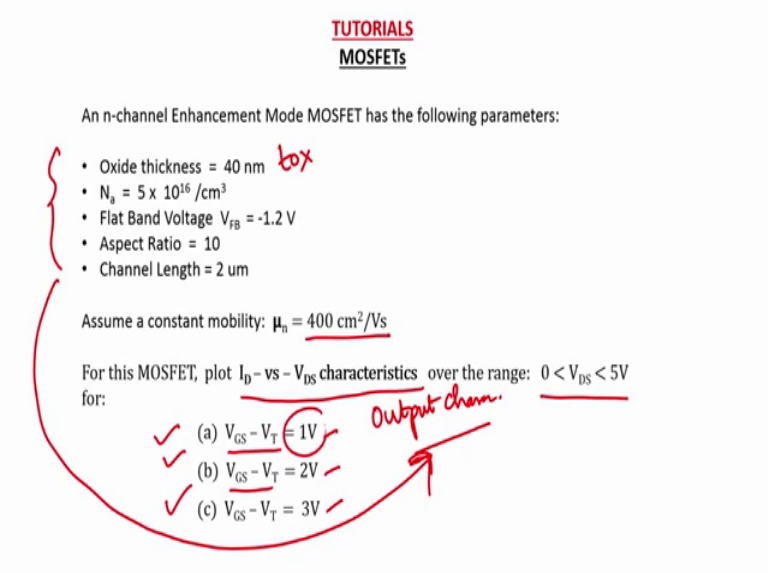

Let us move on to the first problem mode. So, this is a problem from the MOSFET topic, the problem reads like this an n channel enhancement mode MOSFET has the following device parameters which is basically oxide thickness is given tox and doping concentration, the flat band voltage is minus 1.2 volts the aspect ratio is 10. And, the channel length is given and you are asked to assume a constant mobility of 400 centimeter square per volt second and for this MOSFET device, you are asked to plot the I D versus V DS characteristics which is nothing, but the output characteristics of the MOSFET over the range of V DS values from 0 to 5 volts. And, you have given different

gate over dry voltage, which is nothing, but this V GS minus V T values to be a 1 volt 2 volt and 3 volt and your ask to plot this ID versus V DS curve.

So, with regards to a problems in MOSFETs, there can be 2 interesting types of problems. Firstly, where you are given device parameters like this and you are asked to you know kind of plot the I D versus V DS curve and the transfer characteristics by you know substituting the values in the current equation to get these characteristics. And, the other kind of problem can be vary a given the transfer or output characteristics and there asked to extract various parameters of MOSFET like mobility threshold voltage and etcetera. So, before starting to you know exactly solve this problem that is refreshing you know concepts for with regards to MOSFET characteristics.

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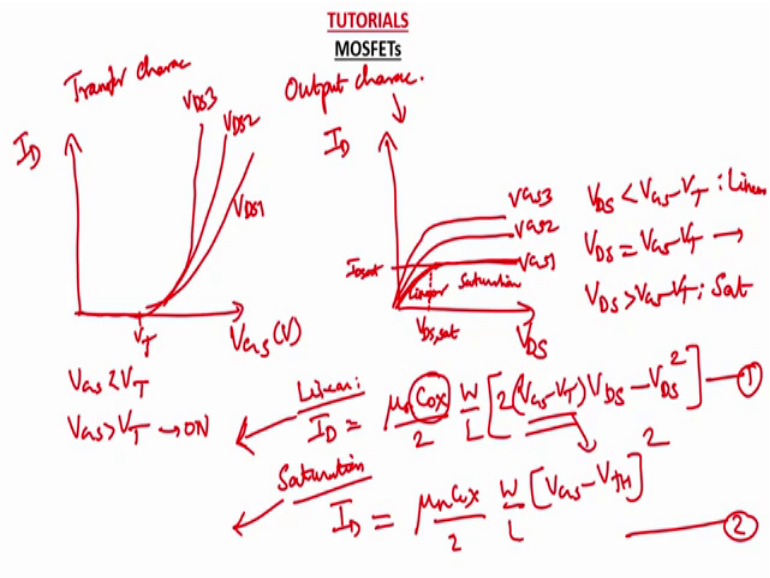

So, you might know that there is something called transfer characteristics and there is something called output characteristics for the MOSFET. So, this transfer characteristics looks at the variation in the drain current with respect to the gate source voltage for different VDS value, which is nothing, but the drain to source voltage.

So, MOSFET is off some values and you know this it is on after the threshold voltage and this can be VDS 1 and VDS 2 and VDS 3; so, VGS less than VTS, where MOSFET is off and VGS greater than VT, which is a threshold voltage. So, a MOSFET is on and the output characteristics looks something like this, where it is nothing, but the plot of

drain to which is the drain current versus drain to source voltage for different gate to source voltage values for different VGS values.

So, there is something called this linear region, where the current looks like this and the there is a point, where the current saturates and this is the ID sat value and there is a point which is called the you know VDS sat, which is nothing, but the pinch of point after which the MOSFET enters saturation and till that the MOSFET remains in the linear region and this is the saturation region. So, you can you know kind of define the curves like this, which is VDS when it is less than VGS minus VT, the gate over dry voltage, the MOSFET is said to be in linear region. And, VDS exactly equal to VGS minus VT is nothing, but the pinch of point and when VDS greater than VGS minus VT you say that the MOSFET is in the saturation region.

And you can also recollect from your lecture slides that in the linear region the drain current equation for a MOSFET looks something like this is nothing, but mu n Cox by 2 W over L into you have 2 term here VGS minus VT into VDS minus VDS square. So, for very low drain to source values, you can see that the plot is almost a straight line and in the saturation region, you can say that the current equation looks something like this I D equals mu n Cox by 2 W over L into VGS minus VTH the whole square.

So, this is for the linear region and this is for the saturation region and you know you can also see that in the saturation region the drain current value is remains independent of the drain to source voltage it is almost constant. So, this is for you know a MOSFETs ideal MOSFETs, where there are no channel length modulation effects. So, when there is channel length modulation effect present then, you can see if there is a slope present in the output characteristics of the MOSFET.

So, in that case the saturation drain current value is also a function of the VDS value. So, this is a fix summary of what we have learnt in the lecture slides regarding MOSFET output characteristics and transfer characteristics. So now, just looking into the particular problem, where you are asked to calculate the ID versus VDS characteristics for the given device parameters. So, looking at the so, you need for this particular problem, you need to find the you know current equations for various gate dry or the gate over dry voltages in the linear region and also in the saturation region and you also have to find out what is the pinch of point for each case.

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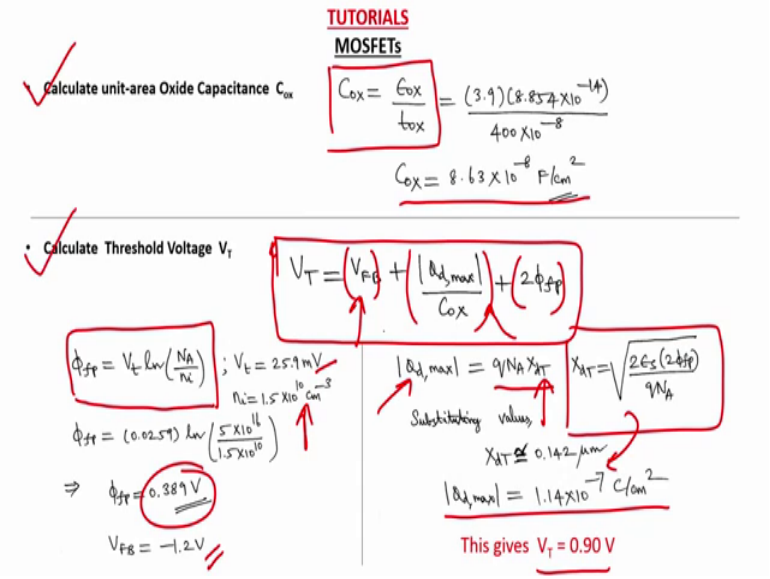

So, use you can you can see that you are given the mobility value and you have given you know the different values like W over L. So, what you need to kind of first do is find out calculate 2 values, which are unknown to us which is basically the Cox and this VT So, we set off with calculating what is the value for Cox which is nothing, but the unit area oxide capacitance of the MOSFET device. So, you know that Cox is nothing, but epsilon ox over tox. So, plugging in all the known values, you can find that Cox comes out to be is 8.63 into 10 power minus 8 farad per centimeter square.

Secondly, we you know calculate the threshold voltage for the MOSFET device from the given parameters and you can recollect that this threshold voltage has you know a different components like this, which is basically this flat band voltage 2 phi fp term and this depletion charge term q depletion by Cox term. So, to calculate threshold voltage first we try to find out what is this phi fp which is nothing, but VT lan N A by ni. And, you are given the thermal voltage to be 25.9 millivolts and you are given the intrinsic carrier concentration from which you can find that phi fp comes out to be 0.389 volts and in the question you are also given that the flat band voltage is minus 1.2 volts.

And to calculate the threshold voltage the other value, you need as the input is this depletion charge, which is nothing, but qNA into XdT. So, this you are calculating at a point, where the you know maximum space charge width is achieved. So, at maximum space charge width, you have this relation relating to phi fp and qNA. So, substituting

values you get X dT the maximum spare charge width to be a 0.142 microns and substituting values further you get Q d the depletion charge value per centimeter coulombs per centimeter square.

And plugging in all the known values you find the threshold voltage for the device to be 0.9 volts. So, we have calculated 2 unknown parameters, now which is basically the Cox unit area oxide capacitance on the threshold voltage for the device.

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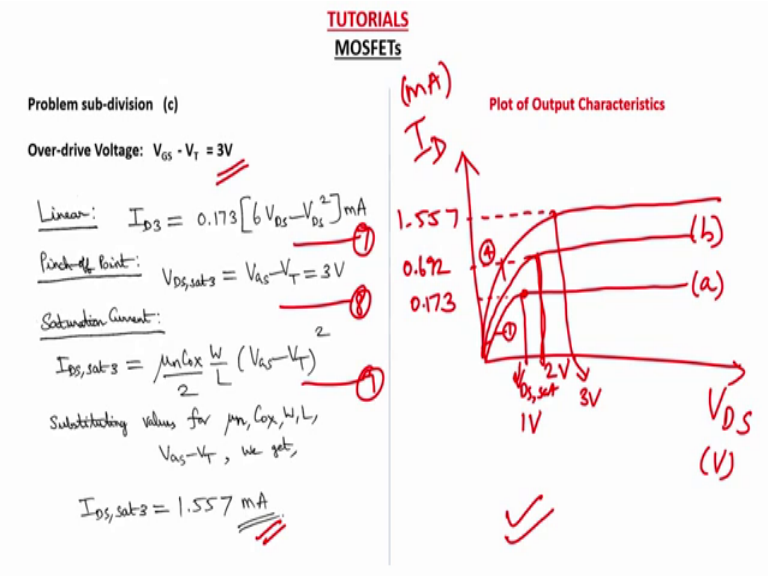

So now, next we set off to you know kind of plot the main requirement for the question which is nothing, but the output characteristics I D versus VDS in volts this kind of in probably in milliamps. So, first we you know extract the needed equations for the a gate overdrive voltage for VGS minus VT equal to 1 volt.

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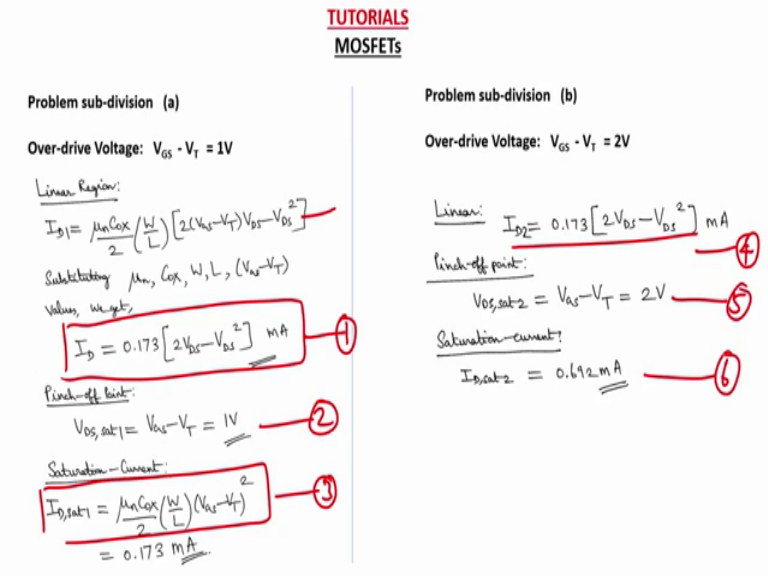

So, for VGS minus VT equal to 1 volt, you see that in linear region, you know you take the known linear region equation by substituting, all the known values. Now, we have got Cox and VT and all the known values plugging in back you get that the drain current takes saturation for VGS minus VT equal to 1 volt which is nothing, but 0.173 into 2 VDS minus VDS VDS square in milliamps.

So, we can try to plot this curve here in the linear region. So, this curve is represented by the equation 1, which you have just obtained and the pinch off point is nothing, but we know that it is nothing, but VGS minus VT that is when the MOSFET enters saturation and that is given to be VDS sat and this is 1 volt for this curve. And, then we you know kind of calculate the saturation current equation, the saturation current value by using the saturation current equation and you know you find that the saturation current value turns out to be 0.173 milliamps.

So, we plot that here so, from then on the MOSFET into the saturation. So, this is for gate overdrive voltage given in question a. So, a subdivision a of the question and for subdivision b of the problem again you take the other gate overdrive voltages and find the linear MOSFET equation in the linear region and you know also find the pinch off point and also the saturation current value. So, let us plot for the subdivision b here, sorry if I am not drawing it to scale. So, here the pinch of pinch of point comes out to be 2

volts and this equation is given by linear region equations given by equation 4 and the saturation current value is 0.692 milliamps.

And for gate over dry voltage being 3 volts the linear region equation takes a form like this and here the pinch off point is VGS minus VT which is nothing, but 3 volts and the saturation current value is nothing, but 1.557 milliamps. So, this is the required output characteristics for the MOSFET given in the question ok.

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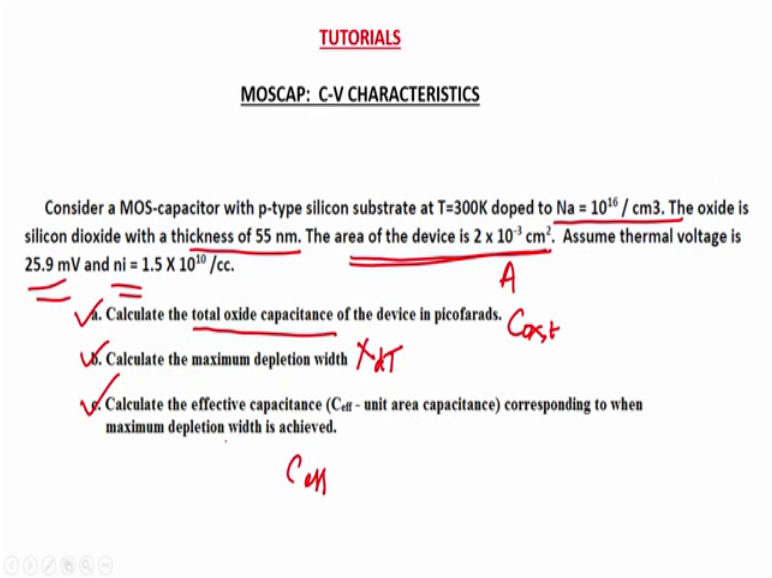

So, let us move on to the next problem. So, this is a problem from MOS cap a MOS capacitor topic and the CV characteristics of a MOS capacitor and I guess this problem was given in one of your assignments and we thought that we will just replicate this problem here and you know discuss the solutions ok. So, that a question drains like this.

Consider a MOS capacitor with p type silicon substrate at t equals to 300 Kelvin dope to doping density of 10 power 16 per centimeter cube given, the oxide thickness to be 55 nanometer and the area of the device, which is the total area A is also given in a 200 10 power minus 3 10 centimeter square and you are asked to assume some values for thermal voltage and the intrinsic carrier concentration and I asked to find out calculate 3 values for this question, which is nothing the nothing, but the total oxide capacitance of the device in picofarads, which is nothing, but Cox total the total not the unit area capacitance, the total capacitance of the device.

And you are asked to calculate the maximum depletion width it can be denoted as a X dT and the effective unit area capacitance at a point, where the maximum depletion width achieved in the mass capacitor ok.

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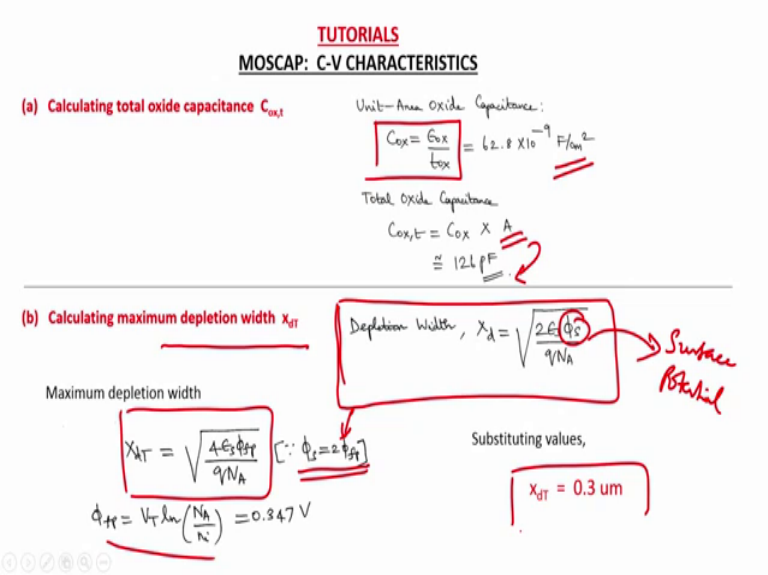

So, the solution goes like this. So, it is very straightforward that Cox is epsilon ox over tox and this is the unit area capacitance, the total capacitance is very straightforward and it is that nothing, but the product of unit area capacitance and the total area of the device. So, when you plug in values, you can see that it is 126 pico farads and next we you know a move on to calculate the maximum depletion width for the device. So, you know that the depletion width for the mass MOS capacitor takes a relation like this which is nothing, but root over 2 epsilon s phi s by qNA this phi s nothing, but the surface potential for the device.

So, at a point when maximum depletion width achieved, you can you can reclaim from your lecture slides that this phi s value takes value of 2 phi fp. So, your maximum depletion width takes some form like this four root of 4 epsilon is phi fp by qNA and we know that phi fp is nothing, but VT lan NA by ni. So, plugging in known values, you can substitute the values to find that the maximum depletion width is 0.3 microns.

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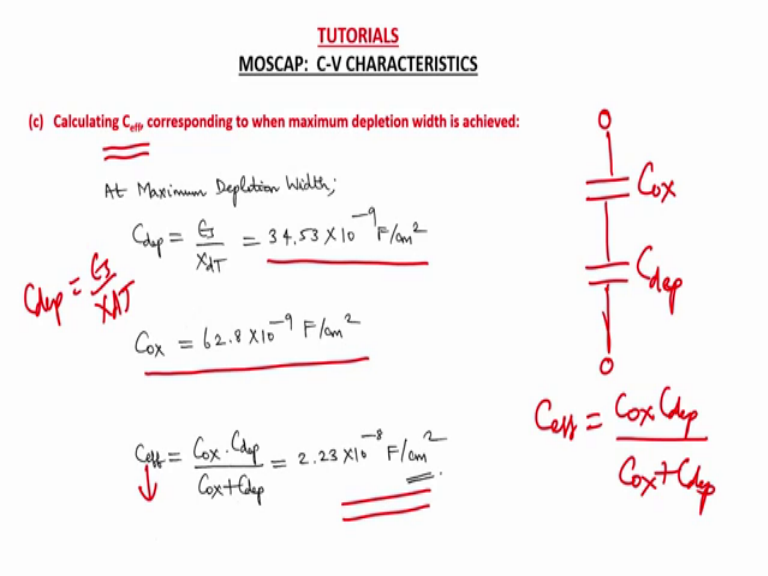

And in the last part of the question you are asked to calculate the effective capacitance c effective corresponding to when maximum depletion width is achieved. So, when you recollect your MOS capacitor, you can see that it is nothing, but the serious combination of 2 capacitances, which is nothing, but Cox here and C depletion. So, these 2 capacitors come to gather in C ess in a MOS capacitor. So, already we know the unit area capacitance Cox been calculated in the earlier section of this problem and we need to calculate, what is this C depletion? C depletion is nothing, but the epsilon s corresponding to when maximum depletion width is achieved epsilon s over XdT.

So, when you plug in values you can find that this is 34.53 into 10 power minus 9 farads per centimeter square and when you have 2 capacitances in C ess the effective capacitance comes over to be Cox into C depletion by Cox plus C depletion. So, and you are asked to find the effective capacitance in terms of unit area capacitance. So, you arrive at this number for this problem.

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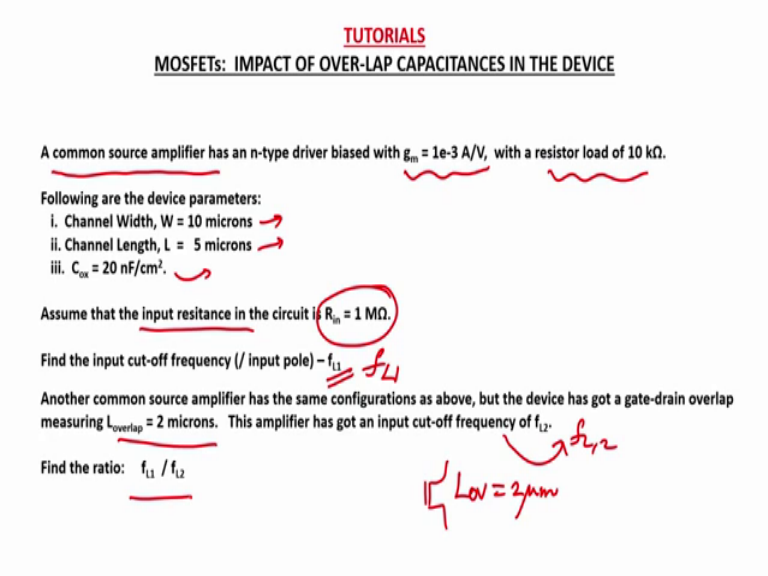

So now, we will move on to the next problem, which is the aim of this problem is to give insight as to what kind of impact the overlap capacitances in a MOSFET device has when it is being used in an amplifier circuit. So, you are given a given that the common source amplifier has an n type driver biased with gm value and a resistive load and your given a various device parameters like channel width channel length and the unit area oxide capacitance and also you given that for this amplifier, there is an input resistance measuring R in equal to 1 mega ohms.

And you are asked to find out, what is a input cutoff frequency for this amplifier which is the that is where the input pole lies, which is nothing, but this f L 1 value. And you are also given that another common source amplifier has the same configurations as above, but except that the MOSFET device in that amplifier has got an additional Lov, which is nothing, but this L overlap measuring to be 2 microns.

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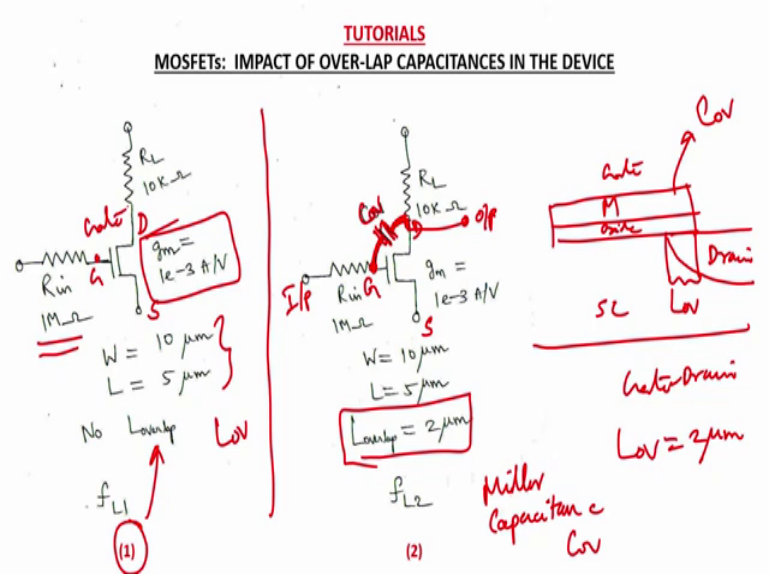

So, you are asked to find out what is the cutoff frequency for this amplifier which is f L 2, this amplifier 2. And you are also calculate: what is the ratio of both the input cutoff frequencies. Let us represent this problem in terms of a circuit diagram to understand what we really need to calculate here?

So, this is nothing, but a common source topology with resistive load, this being the source terminal drain terminal in the gate terminal, you are given that the input resistance here is 1 mega Ohms and this is resistive load of 10 kilo Ohms, you are just shown a part of the circuits, it is shown that the a trans conductance turns out to be 10 power minus 3 amperes per volt and they are given the aspect ratio and for this amplifier 1, you do not have any L overlap Lov, which is nothing, but the overlap length in the device.

And you have another amplifier circuit with the same configurations with, but with an additional overlap length of 2 microns. So, I would like to refresh this concept from the circuits week of the lecture metal and you know, we have this oxide here and you have semiconductor and you would have seen that in the course that there is a drained region here and this is nothing, but the overlap region, which is nothing, but the gate here metal gate here. Since nothing, but the gate to drain overlap in the device and you are given that the overlap length comes out to be 2 microns.

So, this adds to additional capacitance of C overlap which is nothing, but a capacitance coming directly between the gate terminal and the drain terminal of the device in this is

the source terminal. So, this directly this overlap length of 2 microns leads to additional parasitic capacitance between directly between the gate and the drain terminal of the device and you know that for this common source, a configuration this is nothing, but the input terminal and you take the output here.

So, this overlap capacitance acts nothing, but like a miller component directly because this is a component directly connected between the input and the output terminals. So, you would like to know: what is the miller capacitance at the input terminal, due to this Cov.

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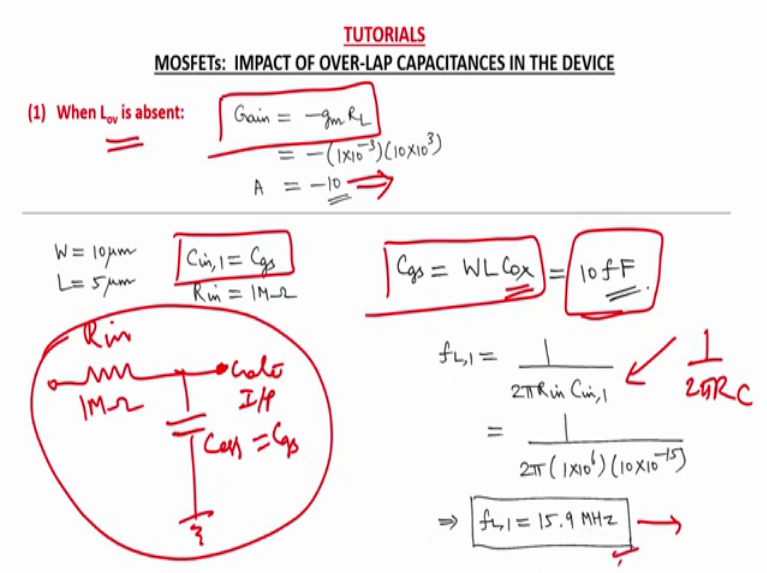

So, first let us analyze the first case, where there is no Lov present. So, in for this amplifier this is let us call, this to be amplifier 1. Here you can represent the effective network at the input terminal assume that this is the gate terminal ok. So, this is the gate. terminal.

So, what is the effective network here? And here we have R in to be 1 mega ohms and between the gate and ground terminal, you have Cg let us call that the effective capacitance between the gate and the ground terminal as C effective and for this device this is nothing, but the Cgs value. So, the C effective this is the effective capacitance of the gate input terminal is nothing, but Cgs for this configuration and you have given R in value and for a common source topology, you know that the gain is nothing, but minus gm RL.

So, from the given trans conductance value and resistive load we can find that the gain comes out to be minus 10 x n a inverting stage. So, the gain is negative now we move on to calculate: what is the cutoff frequency for this input, cutoff frequency for this amplifier. So, which is basically determined by this RC network at the input so, you also know that the gate to source capacitance can be calculated like this is which is nothing, but the total a Cox is a unit area capacitance in the total Cgs is nothing, but WL into Cox.

So, when you plug in values, you can find that this is almost 10 fem to farads at the input terminal. So, the input cutoff frequency is nothing, but a 1 by 2 pi RC at the input. So, where R is the effective input impedance input resistance and C is nothing, but the Cgs value. So, plugging in values you can see that for this amplifier with you know no overlap, you find that the cutoff frequency comes around to be 15.9 megahertz.

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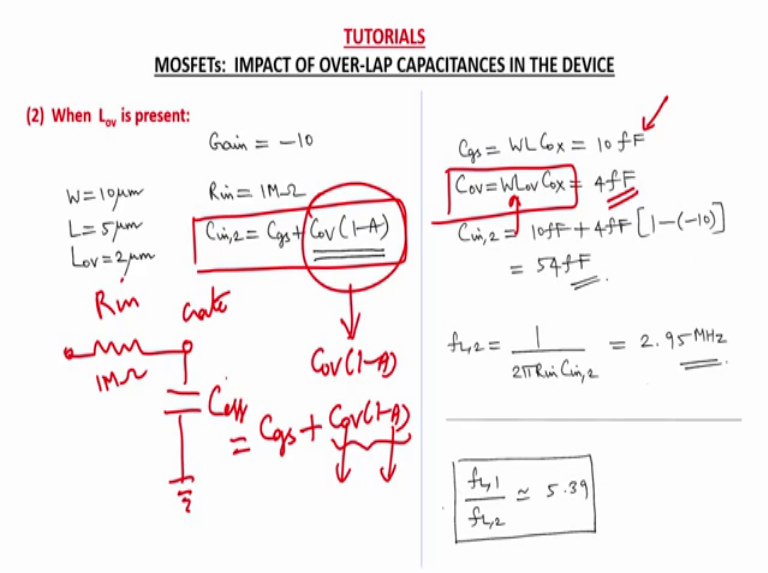

And now let us next move on to analyze this case where Lov of 2 microns is present in the device. So, again we you know kind of draw the equivalent RC network at the input which is the gate terminal here, R in and it is 1 mega Ohms and here again we calculate, what is C effective. But here you see that it is not just Cgs, but in addition you have this gate to C overlap coming directly between the gate and drain terminals, which is a miller component and for a miller component, you know that the can be replaced at the input effectively by a by a capacitance like this and here this is the miller component, where

Cov into 1 minus C is the additional capacitance, which gets reflected at the input, which means that the Cov here gets amplified as Cov into 1 minus A at the input.

So, the effective capacitance of the input is nothing, but Cgs plus Cov into 1 minus A with where this is the miller component. So, you know: what is the gain which is again ten for this and you know that and you have to find: what is Cov which is nothing, but only the overlap length to be considered for calculating the Cov capacitance. So, it is Wo into Lov into Cox, which is nothing, but 4 fem to farad and again Cgs is 10 femto farads here.

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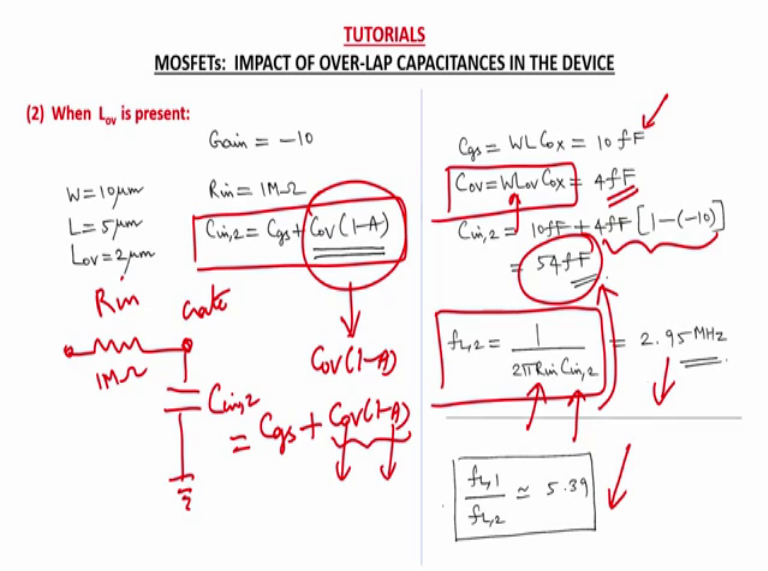

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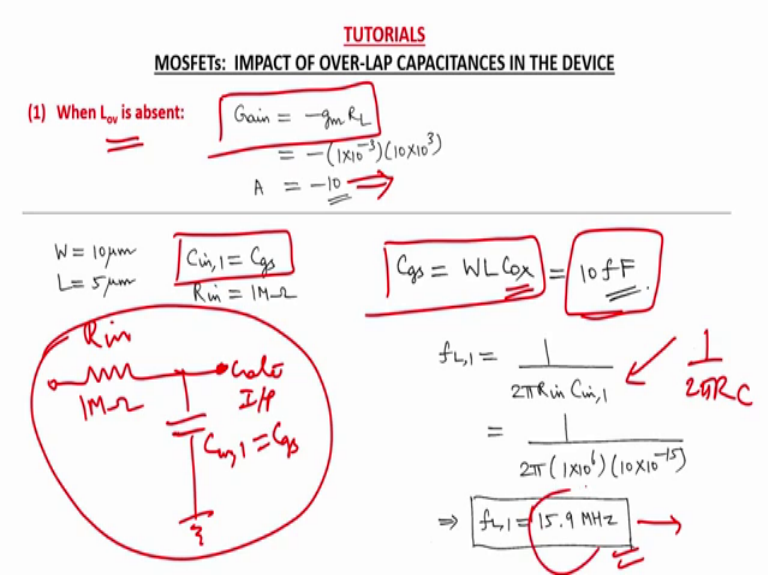

And so, what is the effective capacitance of the input? So, I have I think I have again. So, we have representative with the terminology called C in 2 in for the previous thing it is nothing, but C in 1. So, sorry that I have put it C effective here ok so, C in 2 is nothing, but Cgs plus Cov into 1 minus A. So, when you plug in values, you can find that the total capacitance at the input is nothing, but 54 femto farads. So, you see that due to this miller effect a Cov of 4 femto farads gets amplified and reflects as this much of capacitance at the input terminals.

So, the effective a total capacitances 54 femto farads for this amplifier configuration so, the cutoff frequency is nothing, but again 1 by 2 pi RC, but we use R in to be 1 mega ohms and C in to be the effective value calculated in this problem. So, we can find that the frequency comes down and it is just 2.95 megahertz compared to 15.9 megahertz in the previous problem. So, you see that due to this presence of overlap capacitance, you can see almost a 5 times increase in the capacitance at the input terminal and. So, it affects the operating frequency such that the operating frequency goes down by almost 5 times than the overlap capacitances percent.

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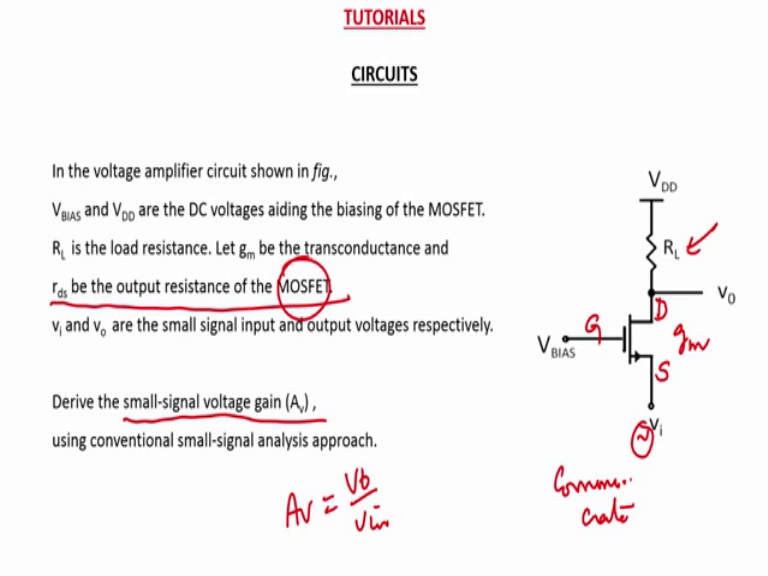

Now, we will just move on to the next problem in this tutorial session, which is a simple problem in the circuits topic of the course hopefully in course lectures, you would have analyze different configurations like common source amplifier with resistive load and common source amplifier with active loads etcetera. And, you would have studied, what is the DC biasing and you know DC analysis of the circuit and also a small signal analysis of the amplifier circuits, where you try to calculate the voltage gain of the circuit and the input impedance output impedance of the circuit.

And here is another one such amplifier circuit, there your small signal input is given at the source terminal and the small signal output is taken at the drain terminal of the a device and you are given at the gate terminal constant DC voltage is given and you have a resistive load RL connected to VDD. So, this is called as a common gate topology. So, in this question you are asked to find out, what is derive the small signal voltage gain AV which is nothing, but VO by V in for the amplifier and you are given that V bias and VDD are the DC voltages aiding the basing of the MOSFET and RL is the load resistance and gm is the trans conductance of the device.

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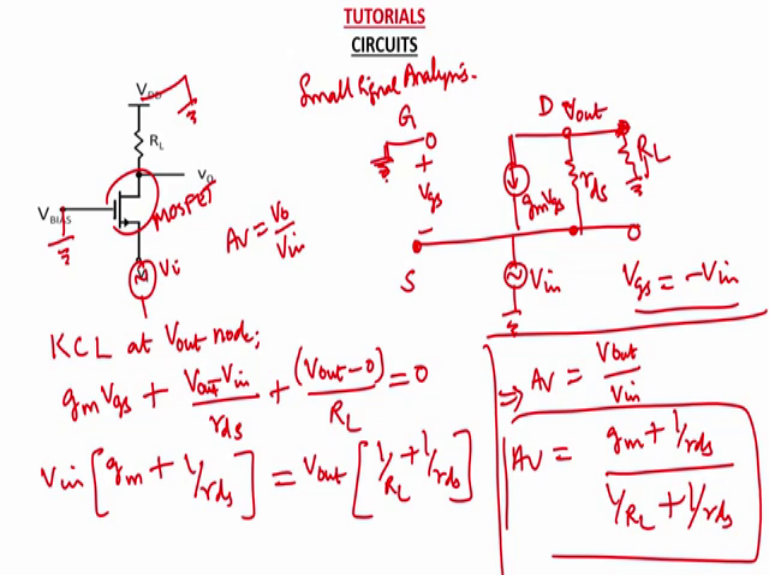

And let r ds be the inherent output resistance for the device itself and you are asked to find out what is the small signal gain of the amplifier. So, here what you would like do is like we do something called as the small signal analysis, where you first ground all the DC voltages, you make them 0. So, you see that your input is applied here and you see V out here and for the small signal analysis, you replace the MOSFET device with it is equivalent small signal model, which looks something like this for a MOSFET device.

So, you have the gate terminal here and you have the brain terminal here and you have the source terminal here. So, this VGS is at the input side and you have a current source measuring gm VGS between drain to source and the rds, which is the inherent output resistance of the MOSFET device coming between drain to source.

So, this is the you know simple first order small signal equivalent model for a MOSFET device and for this particular a common gate topology, you we try to do the small signal analysis to find out what is the voltage gain? Which is nothing, but VO by V in. So, here we represent all the voltage values for here, you set this to ground and VDD and you have set RL, which comes between drain and ground. So, which is RL here and at the source you apply a input small signal input here and you see that the small signal output is being taken at the drain terminal.

So, this is the equivalent circuits small signal equivalent circuit for the goal amplifier circuit. So, here what you would like to do is to derive for the gain expression, you do a Kirchhoff's current law at the V out mode, which is nothing, but the drain mode. So, you

see that there are 3 branches here. So, we write the KCL equation for this which is nothing, but gm VGS plus v out minus V in V out minus V out minus V in by rds plus V out and RL between V out and ground.

So, V out minus 0 by RL so, the summation is 0 and you also see that source here and you know vn is between source and ground and here its ground here and VGS comes like this. So, what it effectively means is VGS is nothing, but minus V in. So, substituting values and you know rearranging, you can you substitute that VGS is minus V in and you know rearrange all the terms, you can find that V in into gm plus 1 by rds is V out into 1 by RL plus 1 by rds ok.

So now, AV this is nothing, but V out by V in is gm plus 1 by rds by 1 by RL plus 1 by rds. So, this is the you know expression for small signal gain for this topology and you can see that when rds is very high, then you can see that this all gain is almost gmRL and you see that there is a a positive term in this expression. So, it means that this common gate stage is a non inverting stage unlike common source amplifier, where you know it is acts as an inverting amplifier.

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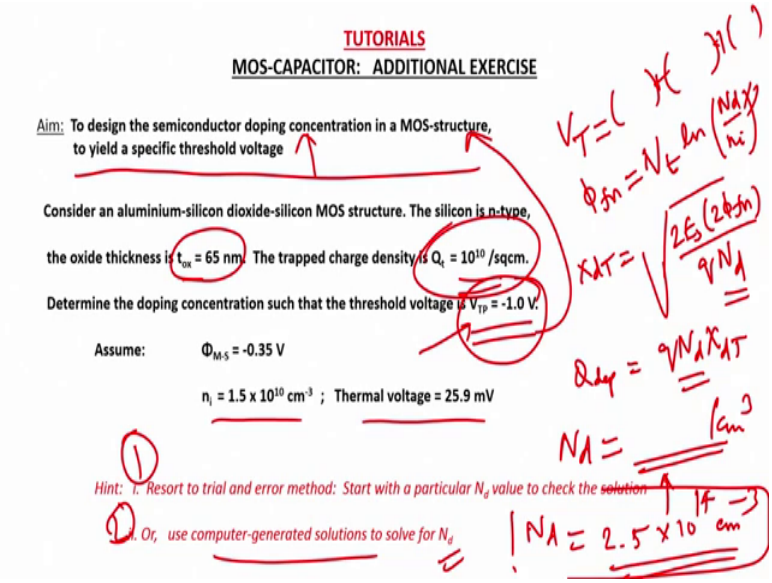

And at this point, we thought we will just give you an exercise problem from the moss capacitor topic, which you can get off look at, you can take it up as your, you know at your leisure time to solve this. So, the aim of this problem is very simple it is nothing, but you intend to calculate the doping concentration for a MOS structure, where you are

decide the threshold voltage is given. So, unlike in the pre and unlike in your assignment questions, where you are being given the doping concentration, all the equations here you given that you need a specific threshold voltage and you know you have to back calculate, what is the required doping concentration to achieve that specific threshold voltage.

And you are given other parameters relating to device such as t ox and what is the and you are also given that there is some, you know interface trap charges and the density of that is given and you are also given the phi ms value. And, you are also given constants like intrinsic carrier concentration and thermal voltages, you know that this threshold voltage, it has got this main 3 components 2 phi f and the depletion charge component and flood band voltage component.

And you can see then in each and every expression this doping concentration comes in. So, which is for example, here V phi fn is nothing, but VT lan Nd by ni. So, since this is a n type substrate, you see that the doping concentration is Nd and the maximum space charge which is nothing, but 2 phi s into 2 phi fn by q Nd and depletion charge is given by qN d into XdT. So, we can see that it will almost all the expressions, this you know Nd term appears here in there.

So, there are 2 approaches to kind of solve this problem, the first approach is to kind of resort to trial and error method, where you assume some value for the doping concentration. You assume that you take some value as this is the doping concentration in per CC value and you plugging those values two kind of see that if you reach to the specific threshold voltage. And if you do not, you refine this doping assumption and you know kind of it towards the unit threshold voltage.

And the other you know way is to use a computer generated solution to solve for these equations to directly find out what is the Nd value. So, you can kind of take this problem as an exercise and when you solve this, you can find that the answer comes to be 2.5 into 10 power 14 into centimeter cube. So, I guess with this we have almost come to the end of the tutorial session and also to end of all the video lectures for the semiconductor devices and circuit course. All these your you know welcome to ask any questions and post all your doubts in the forum and with regards to these tutorials. If you have any

specific questions or you need any further explanations for the tutorial problems, you can always post it in the forum.

Thank you.