Semiconductor Devices and Circuits
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Lecture - 52
Thin Film Transistors

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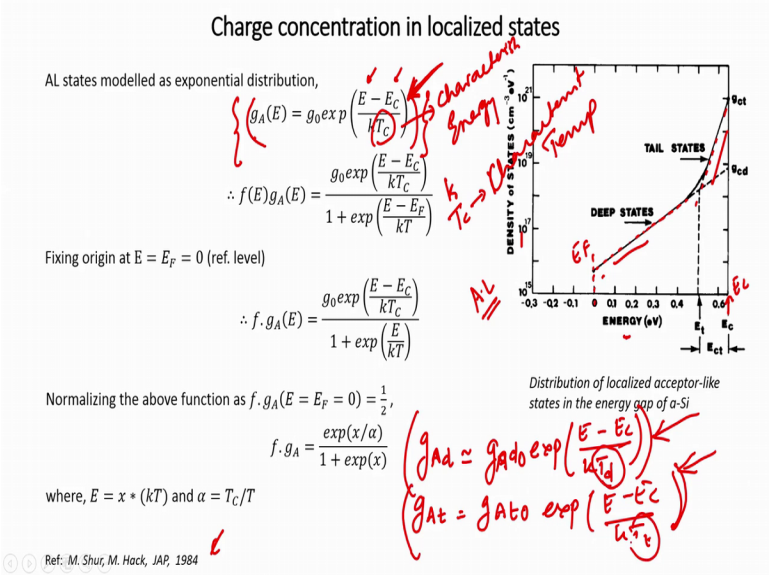

So now let us try to quantify the number of trap charges ok. So, it is not only the qualitative understanding of the disordered semiconductor that is important, but also the methods and the means to quantify these estimates. And from this point on we will study a lot of the methods and tools used to quantify and calculate carrier concentrations and therefore, the currents and disordered semiconductor based devices.

But since the mathematics can get quite involved please keep in mind that the focus is not to be on the mathematics, but on the general approach to solving these problems. So, to start with the primary difference between crystalline materials and disordered materials is the states inside the gap and therefore, the trapped carrier concentration inside the gap. Now inside the gap the trapped carrier concentration is simply the density of states into the fermi function f of E

In the case of crystalline material density of states was 0 and therefore, the trapped carrier concentration was 0, but in the case of disordered materials this density of states has to be defined and a key towards understanding the density of states the key towards

understanding the carrier concentration and disordered semiconductors is the definition of the density of states. So, on this page let us just look at you know how one would go about in quantify the density of states.

So, this particular picture is taken from this reference and it identifies the density of states picture for amorphous hydrogenated silicon. And such a picture can be developed for any disordered semiconductor. So, this is just being used as an example. So, in order to the experimentally estimate the density of states, a one could perform different experiments such as the deep level transient inspector scopy. And one could get an experimental; one could get experimental confirmation has to what the density of state distribution is with energy. Now what is shown here is the acceptor like density of states in the case of this particular material, where this could be considered to be the fermi level and then you have the acceptor like deep states and you have the acceptor like tail states and that is your conduction band edge. Now how does one quantify how does one model the density of states? A very common model is typically if you have a density state distribution that looks like this.

Wherein the deep states the logarithm of the density of states versus energy for the deep states is like a straight line, and the same holds true for the tail state distribution with the exception being that the slopes are different ok. So, how does one go about modelling this? A good way to approach this is by defining the density of states to be exponentially dependent on the energy. So, we say that the density of states is some pre factor into the exponential of E minus EC divided by a fitting parameter which is called as the characteristic energy.

So, here EC k is nothing but the Boltzmanns coefficient and TC is a parameter which is called as the characteristic temperature or one could also use the equivalent which is the characteristic voltage which is k T C by q. So, this can also be called as the characteristic voltage. Now using this fitting p arameter TC one could define a characteristic energy that fits this definition that fits the experimental data using this kind of a model. Now this is a general expression and therefore, you could have one characteristic temperature for the deep states and one characteristic temperature for the tail state. So, one could say that the density of states. So, this is a very general expression. So, this is not is only to define there approached modelling.

One could say that the density the acceptor like density acceptor like deep states have a relation which is says some god which is some pre factor that needs to be estimated from the experimental data into the exponential of E minus EC by a characteristic temperature for the deep states. And the acceptor like tail states is given by say g AT naught into exponential of E minus EC by k Tt which is the characteristic temperature for the tail states.

And similarly one could a define the donor like deep states and the donor like tail states based on the experimental data found. So, the donor like states are not shown in this picture here. So, this is the first step towards any modelling which is to define the density of states and we can define this using an exponential definition and with something called as the a fitting parameter called as the characteristic temperature.

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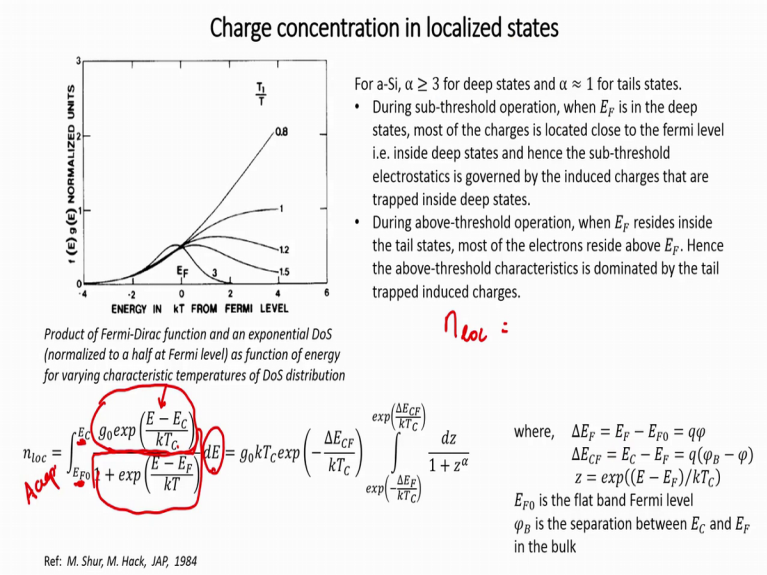

So, the next step is to calculate the total number of localized carriers. So, what do you mean by localized carriers? These are carriers which are trapped and are sitting in the gap states. And how do we define the carrier concentration of localized carriers? It is simply all carriers that set from the fermi level to the conduction band edge. So, here again we are looking at only the carrier sitting in the acceptor like states. So, from EF O to EC. And that is nothing but the product of the fermi function. So, here you can see the fermi function into the density of states we had defined a density of states which is got a characteristic temperature and exponential dependence on energy. So, that is the density

of states into the fermi function and this integral is performed the respected d from fermi level to the conduction band edge. So, which implies that we are integrating and calculating all the carriers that are present in this region here, which are our trapped carriers in the acceptor like states.

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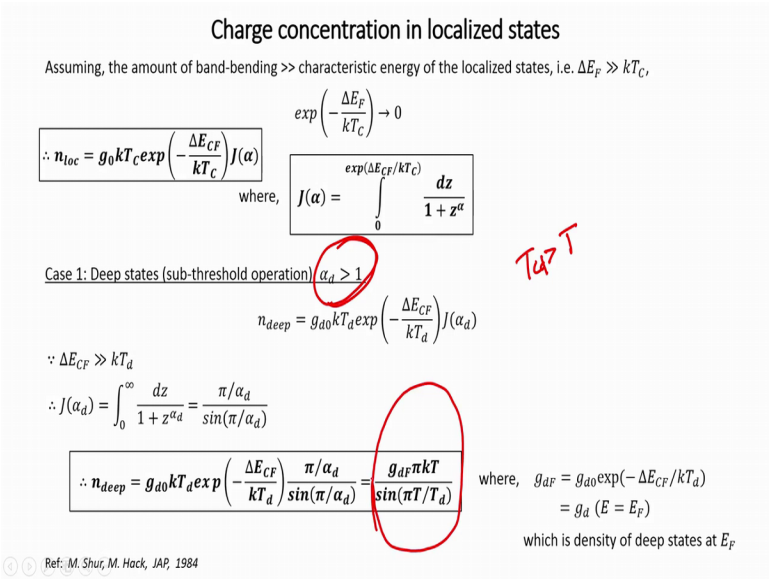

Now this integral can the mathematics here is quite involved, but do not focus on the mathematics depending on the what you say the characteristic temperature.

So, here I should define this particular parameter alpha. So, this particular parameter alpha is nothing but the ratio of the characteristic temperature to the ambient temperature. And depending on what alpha is or what the value of alpha is, this integral can be the answer to this integral can be different. Now it is so, happens that in this particular case for this particular example, if the alpha is greater than one which means if the characteristic temperature is greater than your ambient temperature, which so, happens in the case of deep states, then the number of localized carriers in the deep states turns out to be this particular answer here.

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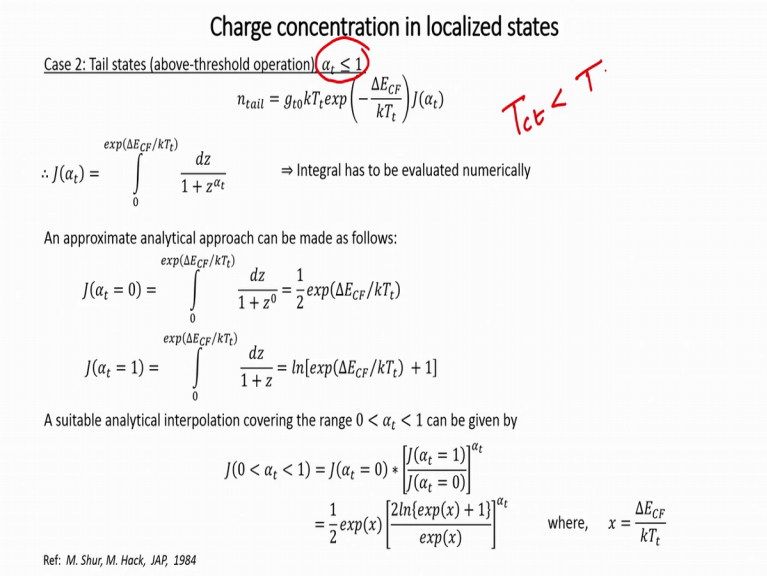

And on the other hand if the alpha is less than 1 which so, which happens to be the case in the case of tail states.

So, the characteristic temperature for the tail states is less than the ambient temperature and therefore, this integral the same integral turns out to be a very different gives you a very different answer which looks like this.

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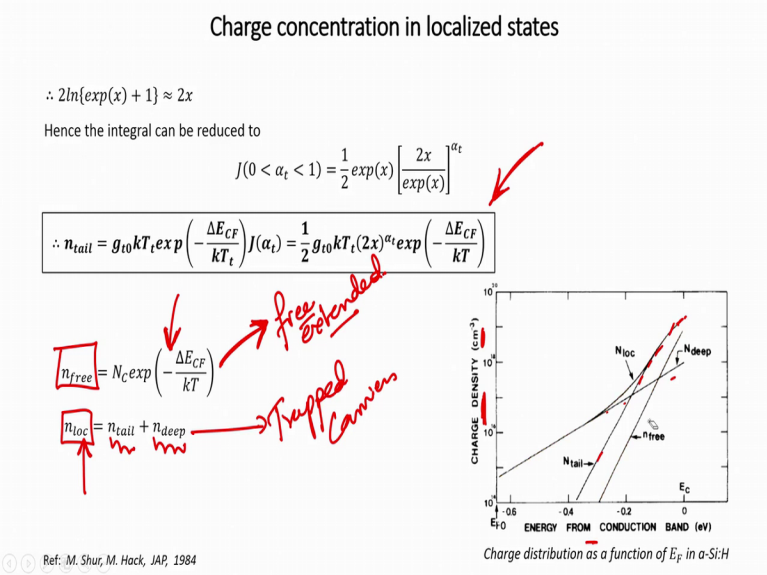

So, as I mentioned in the mathematics is a bit involved, but I am trying to keep the focus on the approach. So now, we can have a complete definition of the carrier concentrations.

So, here are the localized carriers. So, there are 2 kinds of carriers and disordered materials.

You have trapped carriers or localized carriers. So, these are nothing but the trapped carriers which are trapped in the states in the gap. And you have the free carriers which are sitting in the extended states. So, these are the carrier sitting in the extended states. So, these are the ones that can that can provide that posses a large mobility and which can contribute to the current.

So, the number of free carriers per unit volume is given by an expression that you are all very familiar with, which is the density of effective density of states into E to the power EC minus EF minusEC minus Ef by kT. So, this is this expression is very similar from the k compared to the case of crystalline silica. But this is something new which does not exist in the case of crystalline silicon which is the number of carriers that are trapped per unit volume is given by the total number of trapped carriers in the tail states plus the total number of trapped carriers in the deep states.

And those answers are given here for this particular example. So, here is a nice picture. So, here is the charge per unit volume versus energy. So, you can see that the free carrier concentration goes like this. And the trapped carrier concentration is shown here right this is all due to the deep states and that is all due to the tail states. So, it is quite important to note that at thermal equilibrium it could so, happen that the trapped carrier concentration is much larger than the free carrier concentration.

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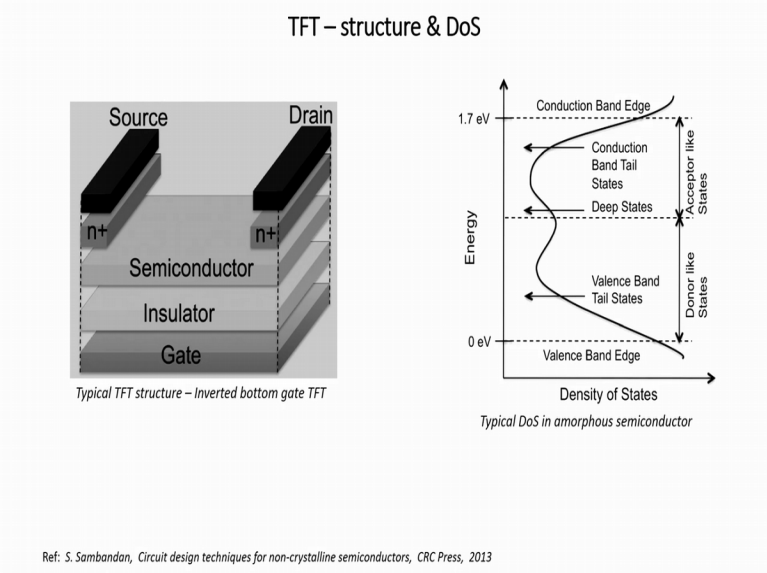

So, having given that introduction to disordered semiconductors let us now look at thin film transistors. And we will see we will look at the techniques used to model thin film transistors, which are basically the field effect transistors using disordered semiconductors and using a thin film process flow. So, asI mentioned before the thin film transistor has got thin film metallic gate, a thin film insulator, a thin film of semiconductor and your source and drain contacts which are tailored such that you have good carrier injection and therefore, low contact resistance.

Now a key point to note is if you are building transistors out of many organic inorganic materials or many organic materials the density of states largely determines the kind of thin film transistor. Again what I mean by that is regards to whether that transistors n type p type or whether the process allows a complimentary mos device and that is got to do with the density of states picture. And we will have a look at the working of the thin film transistor to understand this.

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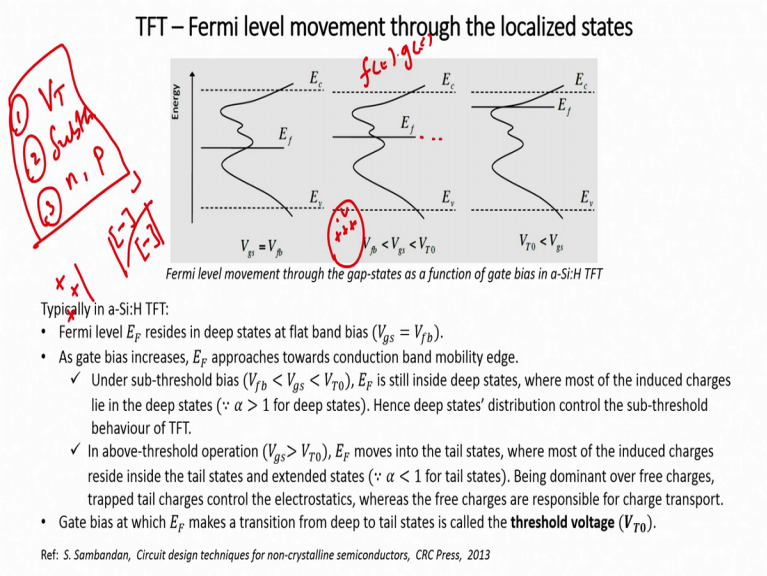

Now how does a thin film transistor work? Now as we so, what we have to look at here is the density of states picture. So, let us say we have a we have applied a gate voltage we built a thin film transistor and we start throwing in positive charge on the gate.

Now in the case of crystalline silicon, what was the consequence of us putting positive charge on the gate? In the case of crystalline silicon, if we looked at the, the band gap was very free and the Fermi level was free to move about or in other words the band bending was very, very free. So, in crystalline silicon we had a device structure wherein we had a doped semiconductor. And we had a insulator and the gate and the consequence of us adding positive charge was firstly, be achieved flat band and then if you use aP-type silicon body, we saw that the we first achieved depletion. Here we had our intrinsic fermi level bend towards the fermi level or in other words the conduction band and valence band began to bend towards the fermi level; we first achieved a depletion where in all the positive charge here was compensated by the negatively charged ions acceptor like ions in the bulk.

And then by adding more and more positive charge, we could achieve a significant amount of band bending; the band bending became very significant and the intrinsic fermi level bent below the fermi level near the interface. And therefore, the moment Ef became greater than Efi Ei we found that electrons began to appear at the interface and we had a region of operation called as the inversion region of operation. And these

electrons where the ones that enabled carrier transport between source and drain so, that was the working of the crystalline silicon semiconductor.

Now in the case of disordered semiconductor the fermi level is not free to move. There is band bending, but it strongly depends upon the density of states. Now as we add positive charge in the gate of a non crystalline semiconductor MOSFET or in other words the thin film transistor is that, the fermi level tries to start moving towards the conduction band edge ok. In other words if you think off the band bending picture the conduction band attempts to bend towards the fermi level.

But since there are so, many states sitting in the band gap, the movement of the fermi level towards the conduction band implies that these states must now be filled with electrons before the fermi level can make progress and move towards the conduction band edge. Or in other words all the positive charge that we are on the gate is being compensated by the trapped charge that is appearing in the gap states as the fermi level makes it is move towards the conduction band edge.

So, let us say this is the let us say that figure 1 is the position where your Vgs is equal to flat band. So, all bands are flat at this point.Now as we add more and more positive charge on the gate, we find that the fermi level starts moving towards the conduction band edge or in other words the conduction band tries to start bending towards the fermi level, but since the fermi level is now climbed up by this distance as compared to it is flat band point all these states are now filled with carriers there all filled with electrons and that occupancy depends upon the product of the fermi function and the density of states.

Now it is these electrons that are going to compensate for the positively positive charge that we have applied on the gate. In the case of crystalline silicon we found that it was the band bending. And it was the exposed dopant ions that was contributing or compensating for the positive charge on the gate, but here it is the trapped charge or these electrons that are occupying acceptor like states that are going to contribute to the charge balance. So now, the meaning of acceptor like states becomes very clear right.

So, as the fermi level moves up these states were filled with electrons. And therefore, they all became negatively charged. So, they are playing the same role as the doped acceptor like ions in the case of an n channel MOSFET. So, as the fermi level moves up the acceptor like states get filled with electrons and this charge compensates for the

charge on the gate. So, as more and more positive charge is applied on the gate, the fermi level starts heading closer and closer to the conduction band edge.

And at some point there will be enough free carriers sitting in the conduction band edge above the conduction band edge in the extended states to permit significant current. And this point is defined as your threshold voltage ok. So, look at the clear difference between the operation of a MOSFET and that of a TFT.

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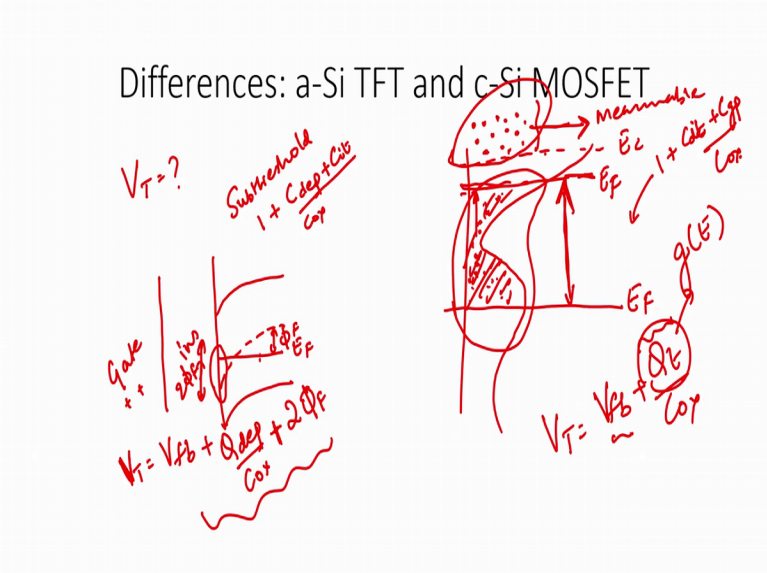

So, let us spend some time looking at this difference in the case of crystalline MOSFETs what defined are threshold voltage what was the threshold voltage in.

The case of crystalline silicon MOSFETs, we had a gate and we had an insulator and when we do the band bending diagram then since the band gap was very clean the conduction band could move to move towards the fermi level very freely. So, at first we had to achieve flat band. That was the first milestone and then. So, that was the let us say that is the intrinsic fermi level and that was the fermi level with the p type doped semiconductor.

So, first we achieved flat band, but then as we started adding more and more positive charge, the fermi level moved closer to the conduction band or in other words there was some band bending. There was some band bending. And all the positive charge in the gate was compensated for by the depletion charge in the semiconductor. So, the next

milestone toward achieving flat threshold voltage what is that we need to deplete the semiconductor enough in order to get the bands in order to get the bands to bend significantly. And finally, we had to achieve inversion. And how was the inversion point defined? It was that point at which the band bending was.

So, significant that the electron concentration of the interface managed to match the hole concentration in the bulk. So, we said that this was equal to phi F and therefore, the surface potential had to be 2 phi F in order to achieve threshold voltage. So, this had to become 2 phi F and this point we said that there is a enough inversion charge that we considered to be the and we considered the MOSFET to be working above threshold voltage. So, that was our definition of threshold voltage. What about crystalline non crystalline semiconductor a amorphous semiconductors? In this case there is no, there is nothing like a depletion layer.

The semiconductor is intrinsic there is nothing like a depletion layer. There is nothing like achieving these 2 phi F. So, all this there is no there is no inversion point where in the surface potential achieves to phi F. So, these definitions do not exist in a similar manner as in the case of crystalline semiconductors. Instead what we have is we have a conduction band we have states inside the band gap. And let us say this is the fermi level at flat bands. So, yes you do have flat band. So, we have the first milestone to crosses the flat band, but threshold voltage is defined as that voltage, wherein the fermi level gets close enough to the conduction band edge.

So, that all the states above the conduction band edge the extended states are populated with some amount of free carriers that in enable a measurable level of conduction. So, that is the definition of threshold voltages which is a very vague definition. Because it depends upon your density of states profile. So, the density of state distribution is very large. You need to trap a lot more carriers before the fermi level can climb till that point.

And therefore, your threshold voltage is going to be much larger ok and therefore, the threshold voltage the proper definition of threshold voltage. So, let us say that this is the location of the fermi level when the carriers and there is significant carrier population in the extended states. So, the definition of threshold voltage is that, the fermi level needs to, needs to climb up and passed.

These gaps or passed all these states which implies that all these states first need to be filled with electrons and therefore, all this negative charge will balanced all the positive charge applied on the gate. And therefore, the definition of threshold voltage is the flat band voltage plus this total trapped charge in all the states divided by COx. So, how much of charge do we need to trap in all these states so, as to get the fermi level close enough to the conduction band edge.

So, as to get enough carriers in the extend with states. So, that is the definition of threshold voltage. And this depends upon the density of states picture. So, we can see how the density of states is controlling the operation of the MOSFET. Now there is another point, let us look at the mobility of carriers. So, in the conduction band states ok, let us look at the transients; let us look at the transients. Now as the fermi level moves through the states.

We have something called as a sub threshold operation. So, here was the flat here was the flat band voltage. So, there was the flat band voltage and between this point to that point we have sub threshold operation. So, in sub threshold mode of operation the fermi level sits mostly in the deep states. It is only when you are close to threshold voltages of the fermi level as climbed far enough that has gone into that it has gone into tail states. So, in sub threshold operation the fermi level sits in the deep states.

But then as the fermi level makes it is climbed the speed at which it is make it makes it is climb towards the conduction band depends upon the density of states here. So, let us say that that there are a large number of states to be filled. The fermi level will climb very, very slowly. Because it needs to fill all these states with the electrons before it can move upward. But then if there are very few states to be filled then the fermi level can climb a little faster.

So, depending. So, let us say that the fermi level let us say that the density of states looks like this. The fermi level is climbing through very slowly because there are large number of states. And then it increases it is speed and then it goes up very, very quickly through this region because there are very few states. And then it becomes slow again because there are a large number of states again.

So, this implies that the threshold slope or the sub threshold swing would reflect this behaviour you will find that the current is growing very, very slowly because the fermi

level is moving very slowly through the gap states and then in this region as the fermi level begins to move quickly you will find that the current also increases a rapidly. And once the fermi level enters these states you will find the current increases slowly and then the MOSFET get enters above threshold operation. So, in some sense the sub threshold slope and the sub threshold swing are all dependent on the nature of the density of the deep states. So, that is the second difference.

So, therefore, in the case of crystalline silicon, we found that the sub threshold slope if you look at the sub threshold slope it depended on something called as 1 plus C depletion by COx. And because we had interfacial trapped charge, you have see interfacial. But here one can define the sub threshold slope as 1 plus C C interfacial plus C gap states by COx. The third point the third point to note the third point to note has go to do with the mobility of carriers. So, why did we say that why did we say that the amorphous silicon semiconductor has more n type behaviour as compared to p type behaviour. And the answer to that also lies in the density of states (Refer Time: 25:57).

So, let us say we have 2 options we have the fermi level sitting here at flat band and we would by applying positive voltage like to move the fermi level closer to the conduction band edge, as compared to moving the and by applying negative voltage we would like to move the fermi level closer to the valence band edge. Now let us see which of these is more feasible.

Now it so, happens in amorphous silicon, that the density of states in the valence band or that valence band or the donor like tail states has got a much larger density as compared to the acceptor like tail states. So, you can see that this slope here is very, very sharp. Whereas, this slope here is very, very large. Now because this asymmetry you have a very different different is got a very direct consequence on the practicality of having hole type transport or electron like transport.

So, in order to create holes, in order to allow holes to transport, be the transport be the carriers of current transport, we need the fermi level to move towards the valence band edge. But this because of the large density of states this can happen only at very, very large negative voltages. On the other hand it is much easier to get the fermi level closer to the conduction band edge because of the smaller density of states and the tail states.

So, the presence of gap states determines. Firstly, the threshold voltage secondly, the sub threshold slope and thirdly the type of transport is at n type or a p type transport. And this is the significant difference between disordered semiconductor based MOSFET which are called as thin film transistors and the crystalline semiconductor based MOSFETs.

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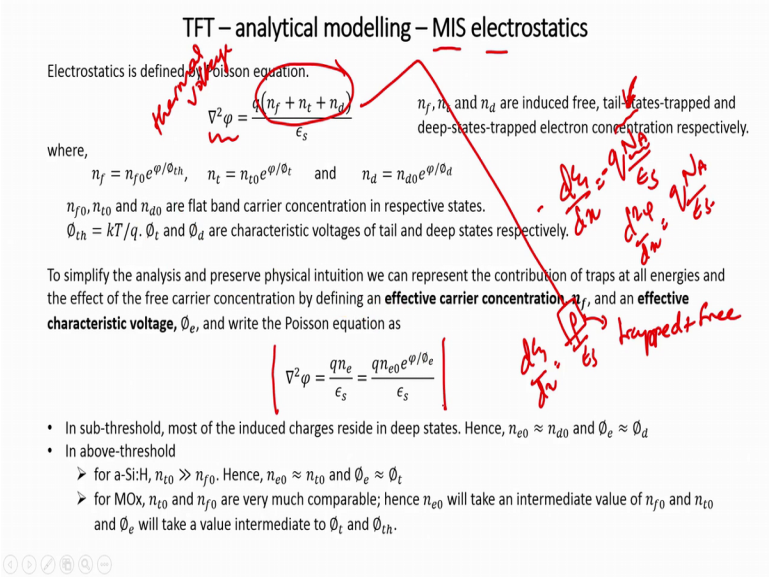

So, let us now look at, let us use all these information to try and see you know the methods is to develop analytical models for thin film transistors. So, again here the mathematics might be very involved, but the focus should be on the approach as compared to the details of the derivations. So, the first step is let us look at the MIS electrostatics. Which is equivalent to your MOS capacitor the electrostatics of there MOS structure. So, the first step is to write down Poissons equation. In the case of you know your crystalline silicon MOSFETs.

We found that Poissons equation was enough you write it in terms of the electric field, it was given by d by d axis q NA by epsilon s where NA was the acceptor ion concentration in the P type bulk which we had used to develop our MOSFET. And in terms of the potential, it was d square phi by dx square is q NA by epsilon s.

Now in the case of amorphous semiconductors, what determines the Poisson equation? So, what determines the charge carriers. So, this charge carrier concentration is given by the trapped charge. So, what constitutes all this charge carriers is the trapped charge, plus the free charge. So, if you go back to this general picture of which you know we looked

at the movement of the fermi level through the gap states, we saw that all these trapped charges were the ones that were responding to the applied electric field or the applied gate voltage. And we also had some amount of free carriers depending upon the location of the fermi level. So, any electrostatics with regards to the band bending or to identify the electric fields inside the semiconductor must consider the trapped charge concentration and this free carrier concentration.

So, therefore, we now have a Poissons equation which is got a free carrier concentration, which is got a trapped carrier concentration. And this is the trapped carrier in the tail states and the trapped carriers in the deep states. So, you have 3 terms, which is the free carrier sitting above the conduction band edge, the trapped carriers in the tail states and the trapped carriers in the deep states. Now each one of these terms depends upon the potential that is applied.

So, therefore, this is a Poissons equation which will also have the potential term on the right hand side. And all of you are familiar as to the means to solve this particular equation. But the free carrier concentration will have an e to the power phi by phi th term where this is the thermal voltage, the trapped carrier concentration in the tail states will have an E to the power phi by phi t term, where this is the characteristic voltage of the tail state trapped charge. And the deep trapped charge carrier concentration will have an E to the power 5 by phi d term where phi d is the deep the deep state characteristic voltage.

So, using these 3 terms one can write out poissons equation and solve it in all it is detail, but for the purpose of these slides what we have done here is we have merged all 3 exponentials and defined an effective carrier concentration. And an effective characteristic voltage and written the sum of these 3 terms as simply this particular exponential ok. So, this need not be this is definitely not the most accurate approach, but it is being done only for the purpose of this example here. So, what is this mean? It says that if the trapped carrier concentration is the largest if say one of these 2 is the largest than any o this term will d will contain of mostly trapped carriers. And this characteristic voltage will tend towards one of these characteristic voltages.

On the other hand if this term here has got mostly free carriers then any o will tend towards this particular concentration that the concentration of nf o. And this term here

will tend towards phi th. So, that is the implication of having this exponential. Now all that is left for us to solve this particular exponential.

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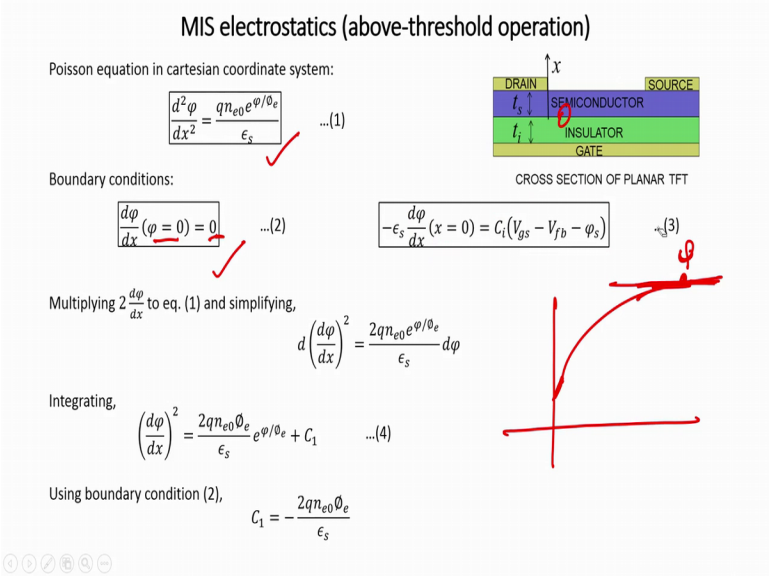

And here is the details of all the solution. So, we have this Poissons equation to be solved and there are there are 2 boundary conditions. The first boundary condition says that at. So, when you have band bending in the semiconductor the point at which phi is 0 that is when we achieve flat band, we have defined phi the reference potential as on the potential in the bulk. So, when phi is 0 you have a 0 electric field. That is when the bands become flat the electric field is 0. The second boundary condition has got to do with the interface.

And what we say there is that the electric displacement which is the permittivity into the electric field at x equal to 0 is given by Ci into Vgs minus V fb minus the surface potential. So, that is the second boundary condition. So, by applying these 2 boundary conditions and going through all this mathematics, we will find that this is the expression for the electric field and you know going through all this mathematics by applying both the boundary conditions we find that the surface potential is defined in terms of a Lambert W function.

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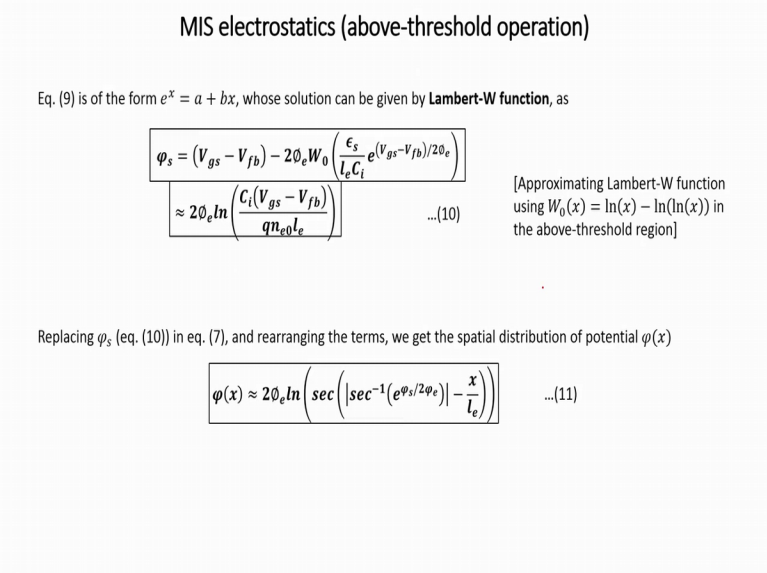

Which can be approximated as this particular expression here. And the surface potential therefore, is and the potential through the semiconductor not the surface potential, the potential through the semiconductor is given by this particular expression. The surface potential in particular is the potential at x equal to 0.

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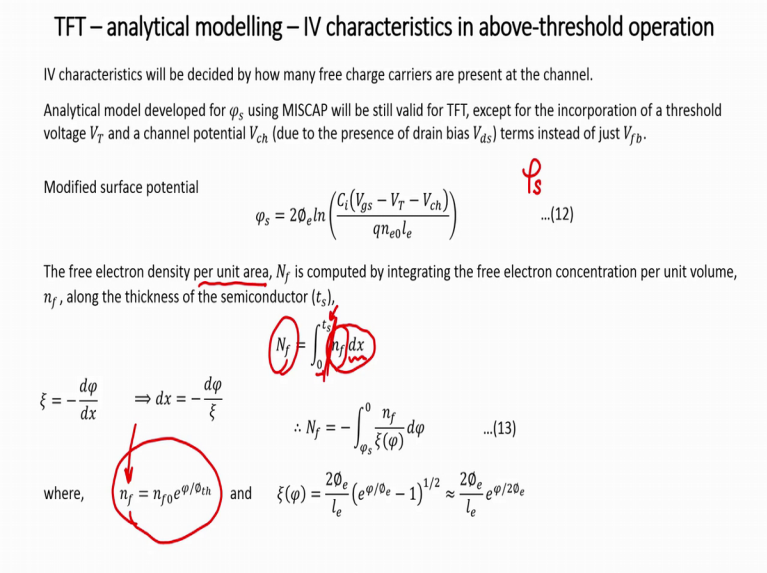

Now, the next step towards modelling is now, we have the potential function and we have this surface potential. Now the surface potential determines the free carrier concentration per unit volume. Because of free carrier concentration per unit volume is

defined by this particular expression here which is your nfo into e to the power phi if e to the power phi by phi th, but the surface potential defines the free carrier concentration per unit volume near the surface. But however, for the definition of your current densities it is useful to define the free carrier concentration per unit area.

And the way this is done is by integrating nf in thickness and you integrate it from 0 through the thickness of the semiconductor. So, the point is thin film transistors are made up of thin film semiconductors. And this thin and what we are saying here is that nf is the free carrier concentration through the entire thickness of the semiconductor. And by performing this integral we identify the free carrier concentration per unit area.

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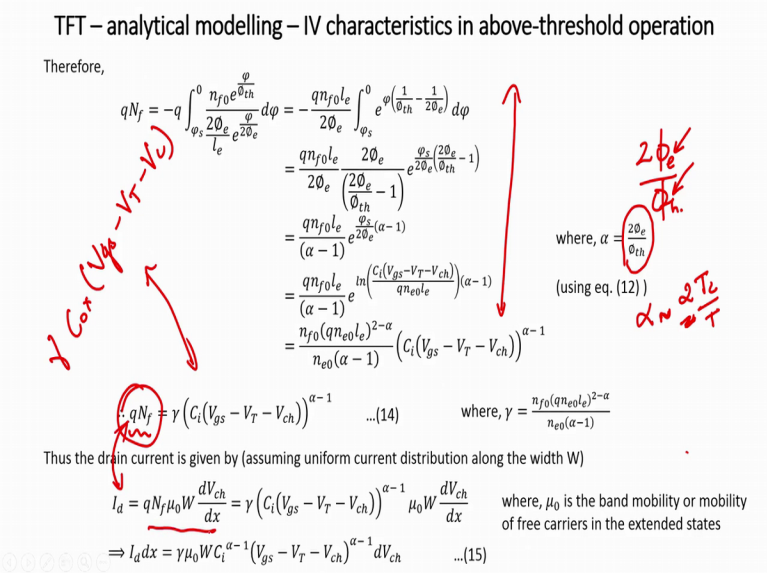

So, that that integral is solved out here in full detail. And we find that the free carrier concentration per unit area is given by this particular expression here. And you see 2 parameters that did not appear in the case of crystalline silicon MOSFETs. In the case of crystalline silicon MOSFETs the free carrier concentration per unit area was simply Cox Cox into Vgs minus VT minus Vc. But here you have 2 other parameters you have an exponent which is called alpha minus 1 and you have a pre factor which is called as gamma.

So, what are alpha and gamma? Alpha is your twice your effective is 2 times the effective voltage divided by your phi th. In other words your alpha is nothing but the

term that we defined earlier which is your twice your characteristic temperature divided by the ambient temperature.

And in the case of crystalline semiconductor materials, this characteristic temperature was the same as the ambient temperature. Or in other words phi e was known to be the same as phi th. And therefore, alpha was the same as 2. And therefore, this term here became 2 minus 1 which was 1. So, therefore, crystalline silicon MOSFETs did not have any factor there. But this is the more general version of the semiconductor and you find that alpha is twice TC by T.

So, that is your parameter alpha. That depends upon the characteristic temperature of the gap states. And what is gamma? Gamma is defined by this particular term. The key point here is that gamma defines the number of carriers in the free states divided by the total effective number of carriers.

Which in some sense includes the carriers in the trap states plus the carriers in the free states. Therefore, gamma as an indicator of this ratio of the free state carrier concentration by the total carrier concentration. And using this particular relation, which is number of the number of carriers per unit area in order to define your current voltage characteristics we find that the current voltage characteristics is given by this expression which can then be integrated to define the current voltage characteristics of your TFT.

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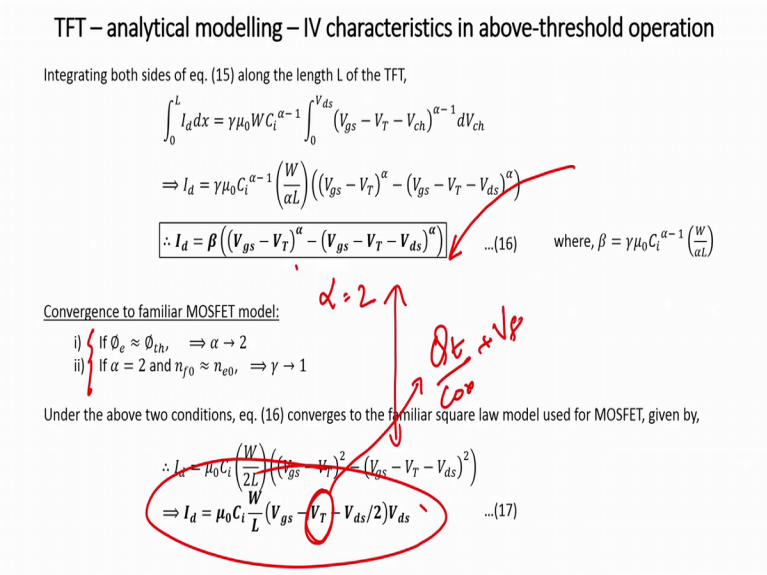

Ok. So, in the case of MOSFETs alpha was simply 2 and we ended up with this particular relation, but even in the case of TFTs if these particular assumptions are made then you will find that there character is that current voltage characteristics of a TFT is quite similar to the current voltage characteristics of a MOSFET. So, in some sense this is a summary of how one goes about with regards to deriving there current voltage characteristics of a TFT. Now as we saw this term threshold voltage in the TFT is given by the total trapped charge concentration by Cox plus the flat band voltage.

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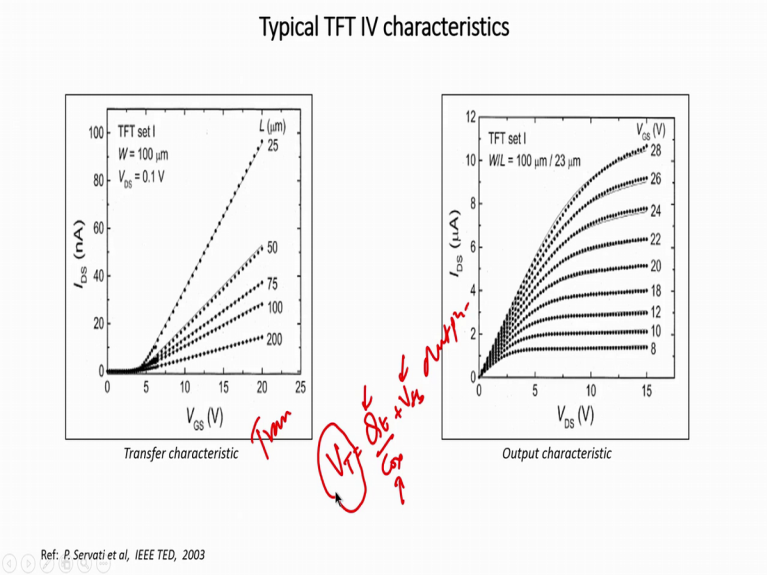

And this plot here shows that typical transfer and output characteristics for a TFT. Now since the threshold voltage is nothing but the trap charge by Cox plus Vfb this is a trapped charge per unit area divided by Cox plus Vfb the threshold voltage ends up being a very dynamic quantity.

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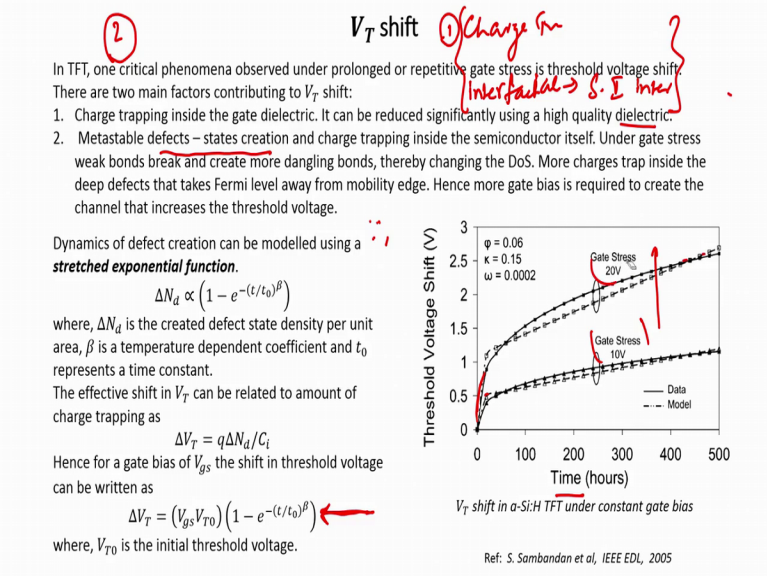

And once C is a very unique phenomena in disordered semiconductors which is something called as the threshold voltage shift. So, what is this mean? So, in the case of crystalline silicon MOSFETs the threshold voltage was more or less a fixed quantity. I mean we once you know the threshold voltage at the MOSFET you used it for modelling your circuit behavior. But in the case of disordered semiconductors when a MOS when the thin film transistor is an operation.

So, let us say you apply a certain gate to source voltage and you apply a certain drain to source voltage. Then when this thin film transistor is an operation you find that the threshold voltage in a thin film transistor becomes a function of time. In other words as the MOSFET current as the MOSFET is driving current, the current in the MOSFET begins to decrease in time. Why does this happen? So, this is a very key phenomena which is very peculiar to disordered semiconductors.

Now there are 2 mechanisms which result in threshold voltage shift. The first mechanism can be said to be both these mechanisms are related to charge trapping, but the first mechanism is charged trapping in the dielectric and in interfacial states. So, although it is not written here, you can say it is dielectric and interfacial states, that is at the semiconductor insulator interface. So, these 2 are the first parameters of mechanisms that contribute to charged trapping.

There is another mechanism which is which contributes to charged trapping and that is related to something called as defect state creation. So, what is defect state creation? So, we saw that there was a certain density of states in the semiconductor. So, that was the energy and this was that density of states. Now its so happens that as the MOSFET is in operation. So, you have your fermi level here, the MOSFET is an operation or the TFT is an operation.

So what happens is that due to the disorder in the semiconductor and due to electrons interacting with these weak and dangling bonds, stronger defects are created. In other words new states are created deep inside the band gap ok. So, the presence of these new states results in all the free electrons now getting trapped in these states or in other words it appears like as though the fermi level is slipping down in energies even though we have a large gate voltage.

And this movement of the fermi level down in energy simply because of the creation of defect states results in it appearing like as though the threshold voltage of the transistors increasing with time. So, it is a very dynamic phenomena and one finds the threshold voltage the transistor increases with time and is given by a relation that looks like this.

Ok something called as a stretched exponential function and that experiments show this which is if you apply a certain gate voltage and if the there is a that the gate voltage is larger the rapidity with which the speed at which the threshold voltage increases will also be larger. So, this is a phenomena that is quite unique to disordered semiconductors and it is of quite some importance.