Semiconductor Devices and Circuits
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Lecture – 49
Amplifiers using MOSFET- continued

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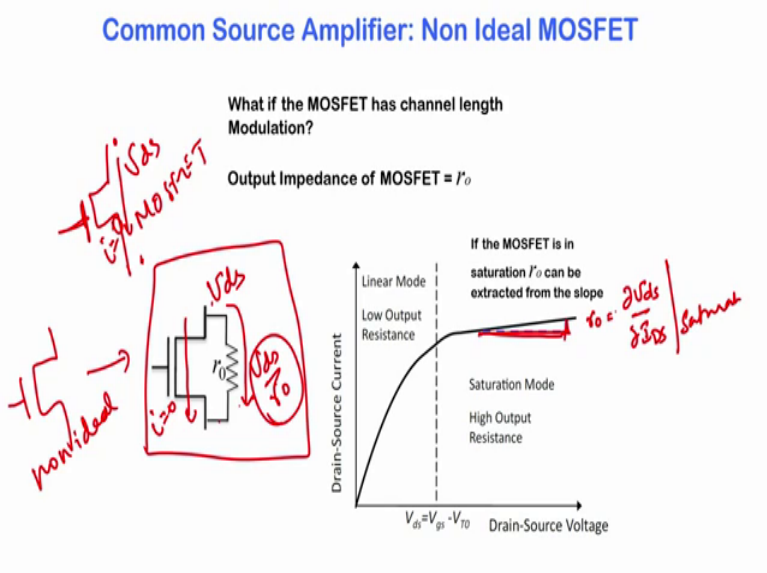

So far we have been assuming that if the MOSFET is in pure saturation say saturation, and it is if it is an ideal MOSFET, then any fluctuation in the drain to source voltage does not create a current. There is no current. But if there is channel length modulation ok, so ideally the MOSFET so far we have been looking at MOSFETs that look like this, but if there is channel length modulation the MOSFET characteristics would look like that. And technically speaking a small fluctuation in V d s, now will cause a fluctuation in I DS here ok. And the way we want to take into account this channel length modulation effect is we will consider two circuits in parallel.

From now on whenever we say channel length modulation is important, we will say that there is a MOSFET that is where there is a no channel length modulation and a finite output resistance in parallel to this MOSFET, which takes into account this channel length modulation term. This r o is essentially the slope it is a dou V d s by dou I D S when the MOSFET is in saturation ok, so that is the output impedance that we are going to add on to the MOSFET in this parallel fashion.

So, now when we say that there is a V d s fluctuation there is going to be no current in this MOSFET, but there will be a current here. And this current is basically the channel length current of the non ideal MOSFET. So, the non ideal MOSFET is a represented as a combination it is a parallel combination of an ideal an a ideal MOSFET an a resistor in parallel and that resistor corresponds to the channel length modulation. So, now this is the physic, this is the connection to the device physics, because you all understand what channel length modulation is.

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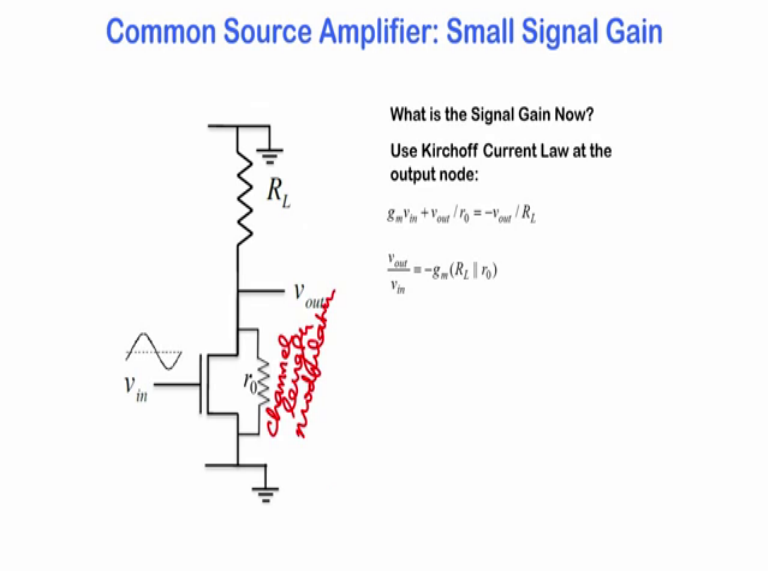

But, now let us see what impact it has on circuits. So, now let us redo the understanding of the gain ok. What is the small signal gain now, now we will consider non ideal MOSFET ok. So, you see this there is now a channel length modulation resistor. So, then we have a non ideal MOSFET. So, what is the gain? So, we solve Kirchoff's law here current law.

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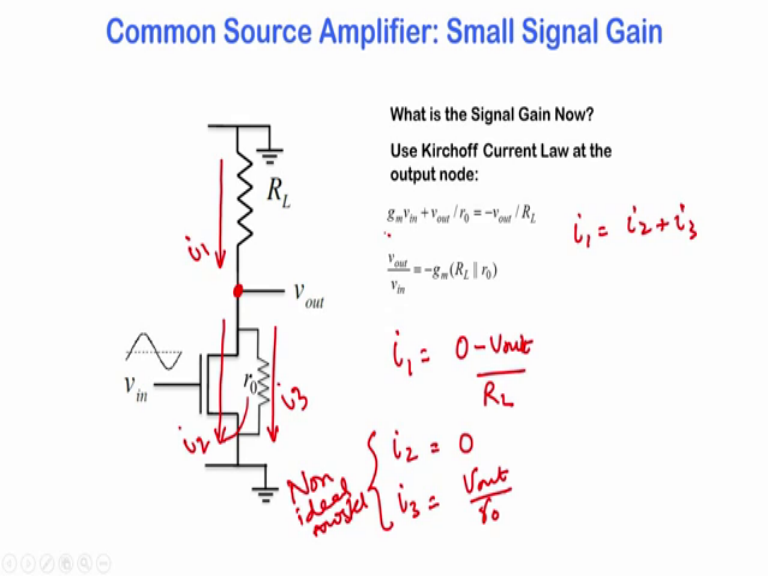

So, the current coming down this node is the current through this, and the current through this ok. So, let us call that i 1, i 2, i 3. So, i 1 is nothing but 0 minus V out by R L, i 2 is 0, because this is an ideal MOSFET. In parallel to this ideal MOSFET is the channel length modulation parameter. And therefore i 3 is V out by r o. And these two together give you the non ideal MOSFET ok. So, therefore, we have i 1 is equal to i 2 plus i 3 and therefore, you have this equation which is I am sorry your.

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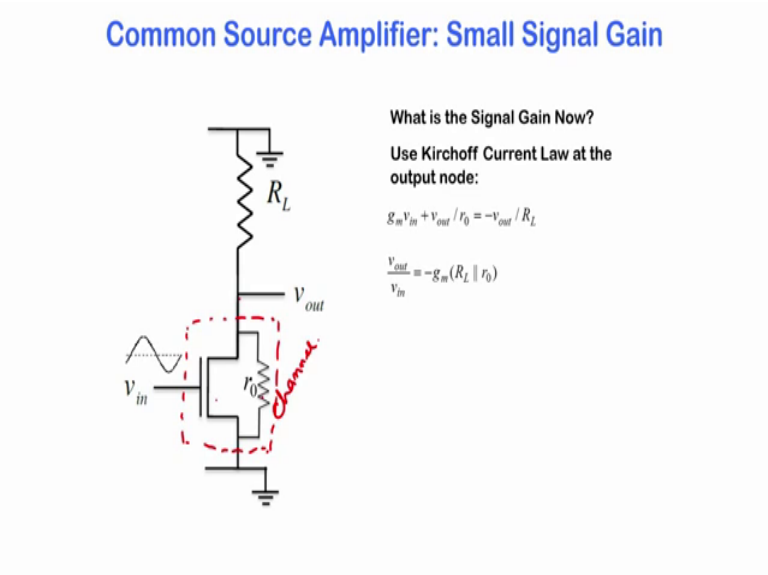

So, let us now consider using the non ideal MOSFET in your amplify it is a exact same circuit as we discussed before, but the only difference is we now have a non ideal MOSFET ok, which is essentially the combination of this ideal MOSFET and this channel length modulation resistor. Now, what impact does channel length modulation have on the voltage gain of your circuit ok. So, once again we will solve Kirchoff's law at this point.

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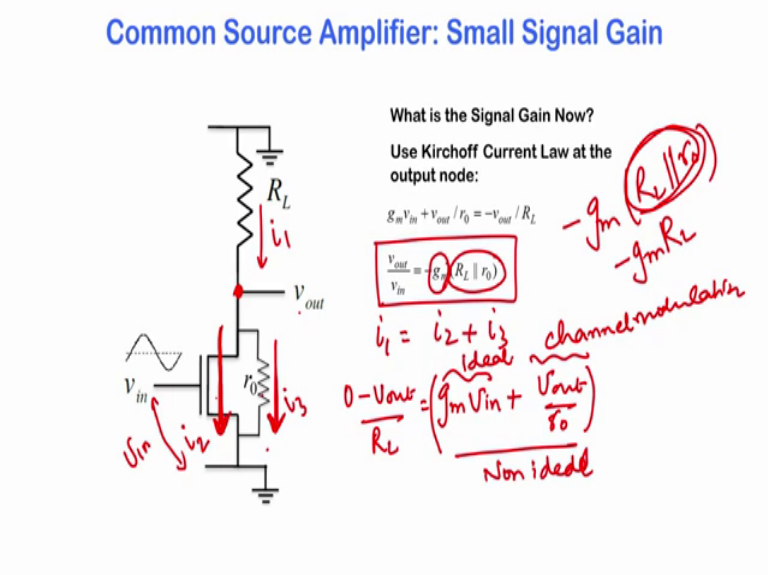

We will have we will call that current i 1 the current through the MOSFET is i 2 this is the ideal MOSFET, and this will be the channel length modulation parameter, which in combination with i 2 gives you the non ideality effect. So, now what is i 1? So, we need i 1 equal to i 2 plus i 3. What is the i 1, i 1 is 0 minus V out by R L. What is i 2, i 2 is going to have there is going to be no impact of V out on i 2, because this MOSFET is now ideal ok.

And all the channel length effect has been take channel length modulation effect has been taken into account in r o. So, this current due to V out is going to be 0, but there is a gate to source fluctuation, which is V in. So, i 2 is going to be g m times V in. And i 3, which is a channel length modulation effect is going to be V out by r o.

So, these two together represent the non ideal MOSFET, which is ideal MOSFET with no channel length modulation, and this is the channel length modulation effect. So, this will result in a gain being minus g m R L parallel with r o. So, earlier with no channel

length modulation if recollect the gain or simply minus g m R L, but now the channel length modulation resistance will appear in parallel with R L ok. So, it reduces the gain a little channel length modulation reduces the gain a little.

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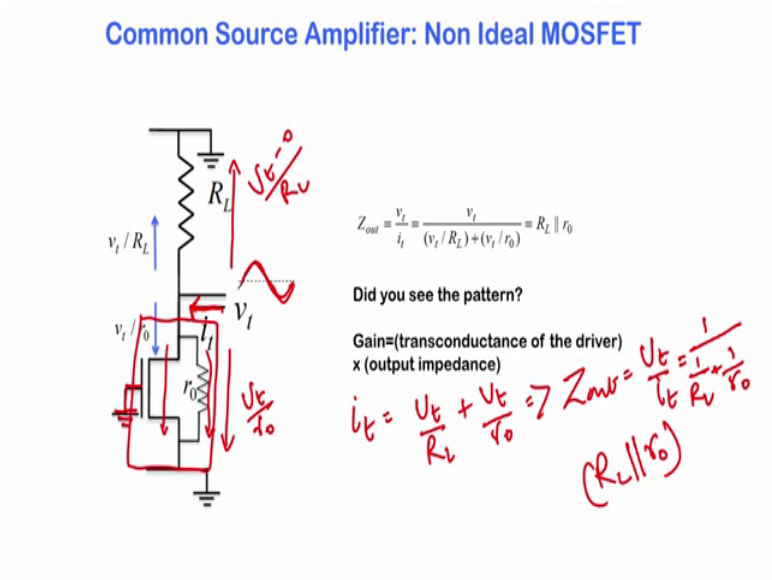

So, now what is the output impedance of the non ideal MOSFET. So, we will do our same experiment, we will apply a test voltage, and we will measure the test current that is going in. And we will forget about any input voltages etcetera we will ground all those nodes. So, what is the current through this branch now through these two devices. This unit will not take any current, because the fluctuation in v t does not matter, but there will be a current due to channel length modulation effect.

And therefore, this node will carry a current of v t by r o. And what about the current through that resistor it is going to be v t minus 0 by R L. So, therefore, the total current is going to be v t by R L plus v t by r o, which is basically saying that my Z output is v t by i t is 1 by 1 by R L plus 1 by r o, which is R L parallel with r o so that is the output impedance. So, again you can see the pattern here. You can see the output impedance into the effective trans conductance is the gain ok, but that is how you calculate the output impedance. So, you are now familiar with using small signal analysis to calculate different circuit aspects.

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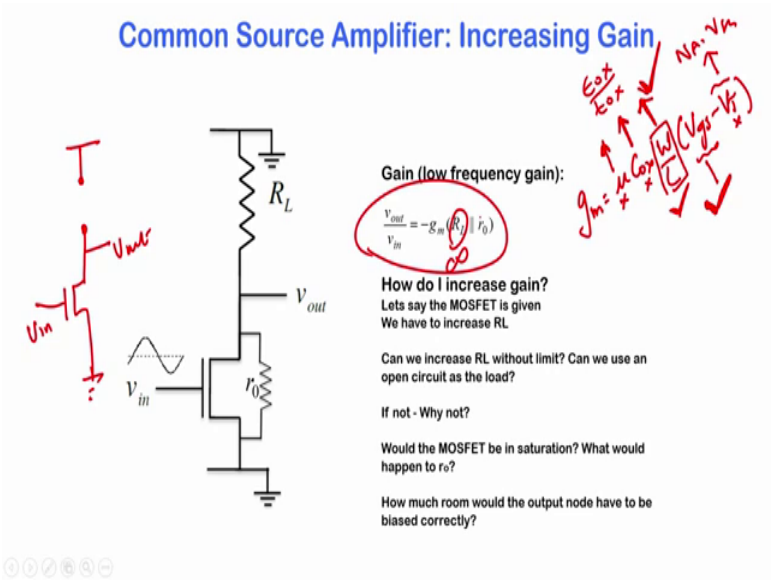

So, now let us look at the next question. So, we know what the gain of the circuit is. So, how do I increase gain ok. I want to make the gain higher, how do I increase gain ok. The first since this is going to be the gain, how do we increase, the first could be try and get rid of channel length modulation, but that is not really a very practical solution right. You cannot get rid of channel length modulation. So, r o is not going to change that is there to stay. What about changing g m, now that is possible, because what is g m, we said that g m is mu C ox W over L into v g s minus V T.

So, how do I change gm, I can increase the mobility, but not that is not very practical, because mobility is defined by a semiconductor, and it is the foundry that decides the kind and the quality of semiconductor they use. Can I increase C ox, it is possible, if you ask the foundry to use a higher epsilon ox and a lower t ox ok, but that is again in the hands of the foundry or the person who makes the devices for you.

Can we increase the aspect ratio, most definitely, because that is an under your control. You do the layout, you do the design, you can decide the channel width in the channel length as long as they fall under the design rules of the foundry. And therefore this is something you could definitely use to improve g m ok. What about the gate to source voltage, yes we can increase that, but only to a certain limit right. We cannot make it greater than the maximum supply voltage used for the technology.

And what about VT, VT cannot we cannot play around with VT too much, because it is the foundry that decides the dopant concentration the flat band voltage etcetera, etcetera. So, this is not something that we can clear round with. So, these are not things that we can play around with, but the aspect ratio, and v g s is definitely something we can adjust.

So, let us say we have done our best, and picked the best possible g m. We have played around with this. We cannot do anything with the channel length modulation. What about the load resistor, can we increase the load resistor, technically yes you can increase the load resistance to give you high gain, but there is a certain limit right. You cannot make the load impedance very very large.

Say for example, let us say I keep I say I am going to continue to I am going to continue increasing the load resistance, and I am simply going to have an open circuit that. So, this is going to be my amplifier circuit. So, I have my V in here, I have my V out there does it mean there I am going to have very high gain.

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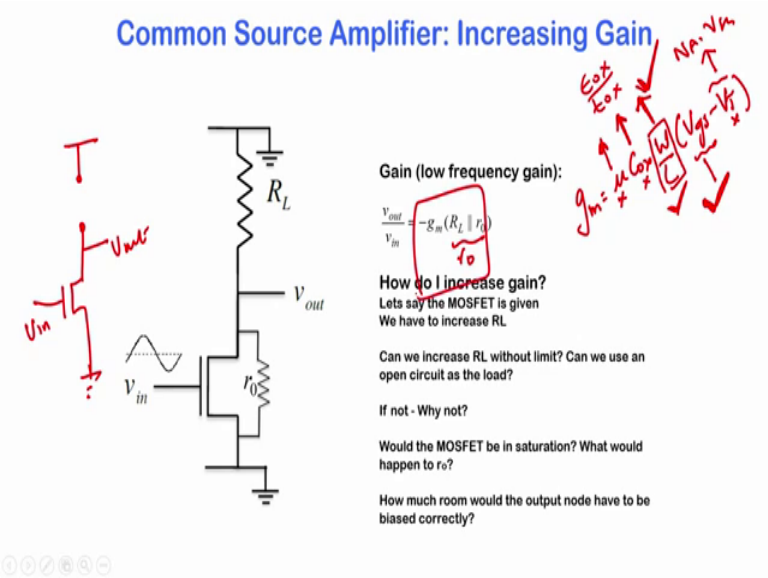

Can I use this equation, and say that R L is infinite, therefore infinite and to the let us say r o r o limits everything infinite, and parallel with r o is basically, r o and therefore my g m is very very large. Can we say that? The answer is no, because clearly you can see that the V out here is not going to remain V out it is going to go down all the way till 0.

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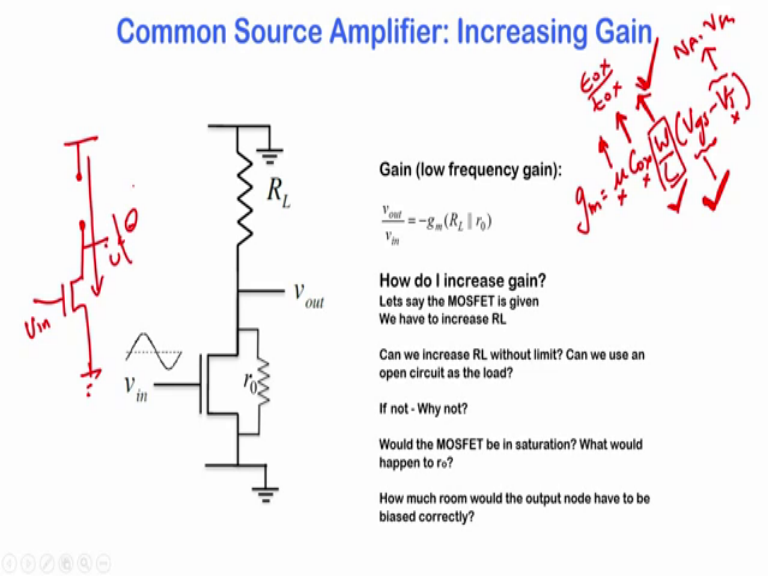

R is going to become very very small. And there is going to be no current in the circuit ok. So, there are it does not seem like a solution that that is going to be readily that is going to solve your problem.

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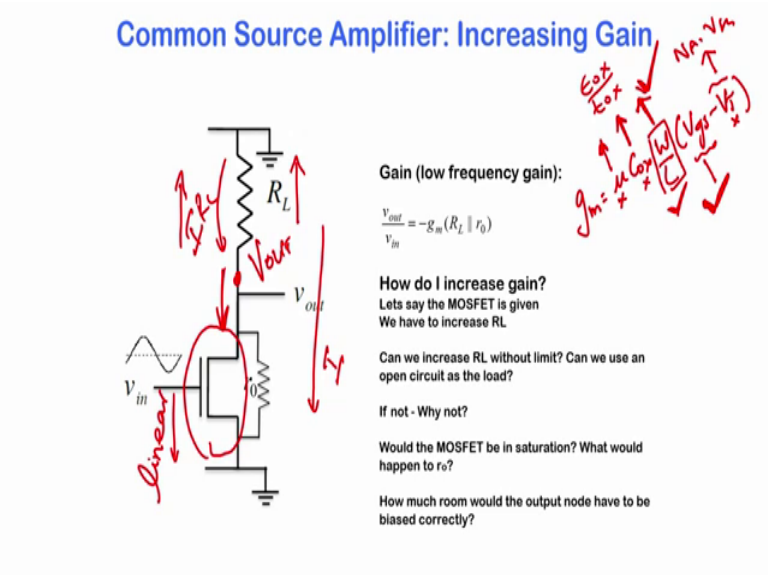

So, what is the what is the catch here, so what is it that you observed, so, as you increase R R L you will find that the D c value of the output node starts dropping ok, because if I want to set a constant current let us say the current is kept constant. And we start increasing R L ok.

The voltage drop here becomes IRL. If the voltage drop starts increasing, and therefore V out the Dc voltage the V out starts dropping. And if it drops too much, if you keep increasing R L, and if the voltage drops too much, then this transistor will move out of saturation, and it will enter linear region of operation it will sort operating in a linear mode.

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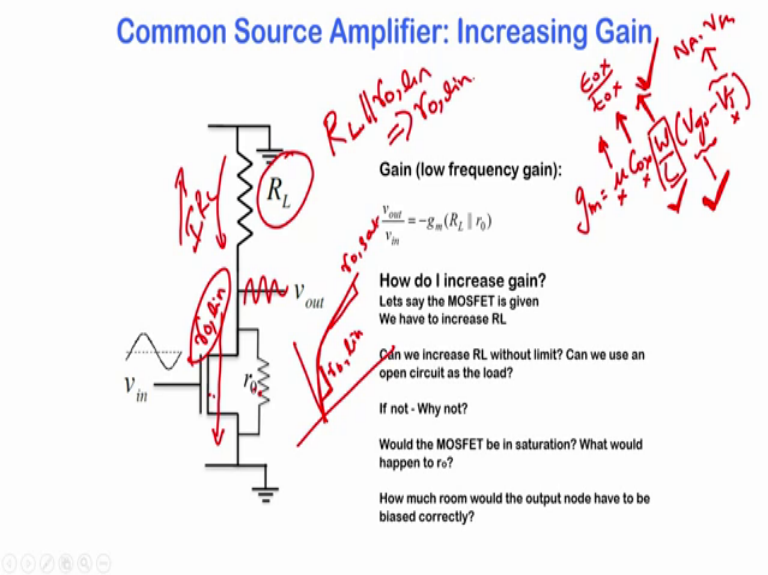

And what is the problem in linear operation, the problem in linear operation, when you use it as an amplifier circuit is that any fluctuation in V out will now start pushing a lot of current through this device, because, now this device has got the resistance of r o linear ok, which is very very small. It is much smaller than r o. And because if you if you recollect your output characteristics of the MOSFET, this is the linear resistance that is r o as you have shown it here, because that is r o, and saturation, and this is the r o and linear. And this these two are pairing in parallel will simply be dominated by r o linear. And the effort of all your large R L in order to achieve this will essentially be limited, because this parallel combination is also going to be there may be a linear.

So, in you cannot increase R L forever so that is the message of the story plus there are many other factor such as your swing of your output goes down etcetera, but nevertheless you cannot increase R L forever. You can you can increase it a little, but not forever, but there is a limit to it. This you cannot do anything and this you can definitely

increase, but and it you can increase it by improving your aspect ratio, but now let us say I am not happy with the situation.

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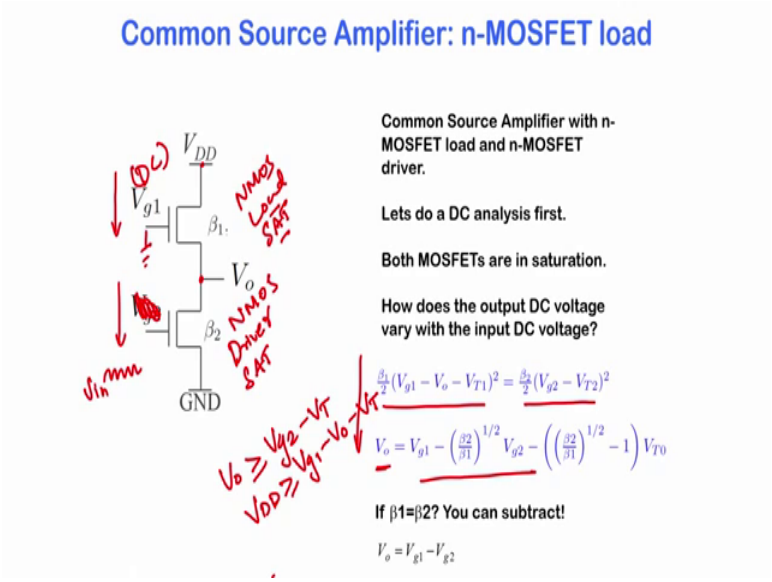

And I want to definitely improve R L what options do I have. So, in our attempt to try increase R L let us try to have a circuit which has 2 n-MOSFETs ok. We have an n-MOSFET driver, which is biased and saturation and an n-MOSFET load which is biased in saturation. And in order to make sure that these two are biased and saturation, you can do a Dc analysis, which I will leave as a homework problem wherein you just equate the currents in these two devices.

So, you see that this is the current in one saturation device. And this is the current in the other saturated MOSFET and by equating these two currents we know we get obtain a relation for V out and all you have to do is ensure that V out is greater than v g 2 minus V T, and that V D D is greater than and equal to V g 1 minus V out minus V T for both these MOSFETs to be in saturation.

So, we have a situation, where the DC conditions are set such that the driver MOSFET is in saturation, the load MOSFET is in saturation, and both are NMOS devices, both of them are NMOS devices. And since this is the driver we are going to replace v g 2 with a small signal input from the sensor. And v g 1 is a DC voltage which is used to just bias keep things under right bias conditions. So, there is no AC signal there ok.

And therefore, this will end up being coming AC ground when we do the AC analysis. So, let us take this case and why I have we chosen an NMOS device, the hope is that the NMOS device can be engineered through aspect ratio, through applying v g 1 in a suitable manner etcetera.

To make sure that V out is always kept finite. And it is always kept keeping you know MOSFET the driver MOSFET in saturation unlike the case of using a resistor, so that is the hope. And we hope that this is going to give us large gain, because now we can use many more parameters to tune the resistance or the MOSFET, but let us see whether that works out.

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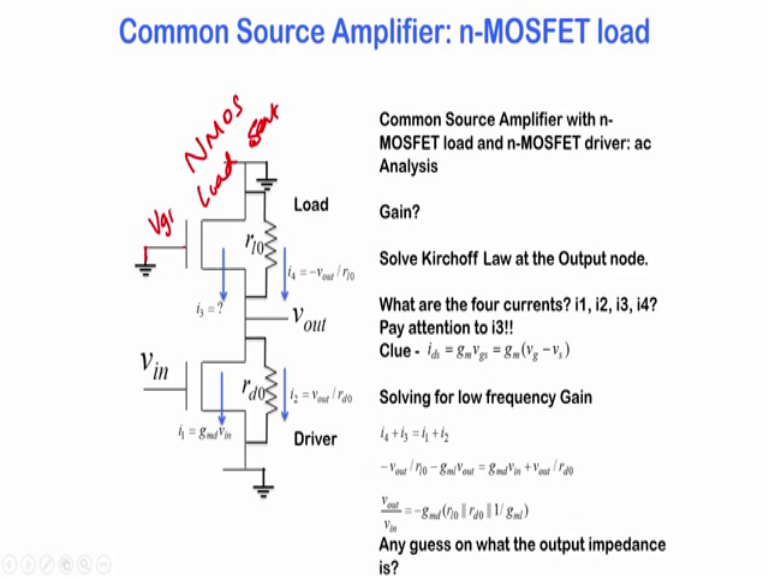

So, the small signal analysis is like this. So, you have that was the load MOSFET that is the load NMOS transistor, which is sitting in saturation. This is the channel length modulation resistor of that load. And this is like an ideal NMOS transistor, and in combination they give you the non ideality effect. And the gate is grounded, because this was a DC bias signal that we had applied, so that is grounded it is ac ground.

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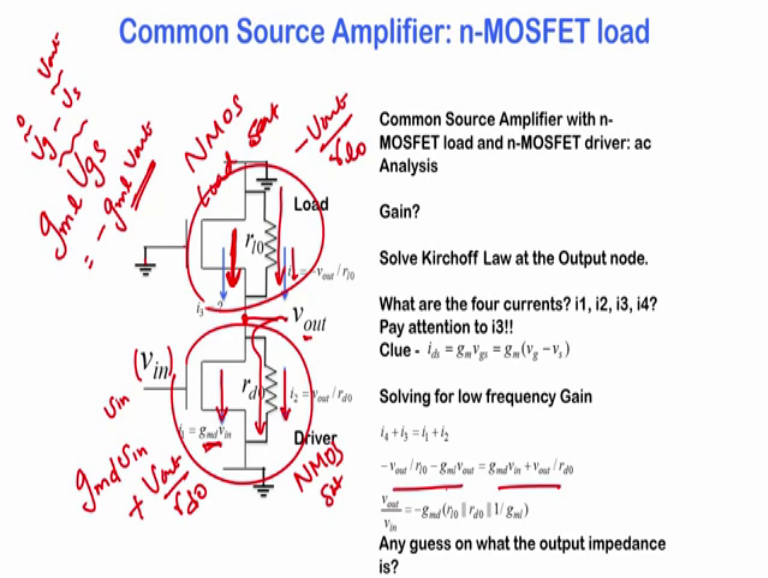

And now we have a small signal a c v in into the driver of the circuit the driver MOSFET, which is also an NMOS, which is in saturation; so, now, again writing Kirchhoff's law here. What are the currents in these four nodes ok, so the current through this transistor here. This current is not influenced by V out, because this is representing the ideal moss.

And therefore, this current is simply g m of the driver into v in that is this. What is the current here, the current here is V out by r o ok, so that current is V out divided by r d o. What is the current through this channel length modulation parameter, so that current is minus V out by r l o. And this current here is there a current here firstly so this current here is not going to be present, because of a v d s difference, because this is in saturation, but let us look at the v g s, if there is a v g s fluctuation, there will be a current of g m l into v g s.

And what is v g s it is a v g minus v s the v g is grounded, but what about the v s the v s is basically v out. So, therefore, there is a current and that current is minus gm l into v out. And this is the key to this forms the bottleneck of using the circuit in order to address gain. So, let us use Kirchhoff 's law. So, the total current through this branch here is this. And the total current through that node there is that and by equating these two you end up with a gain that looks like this.

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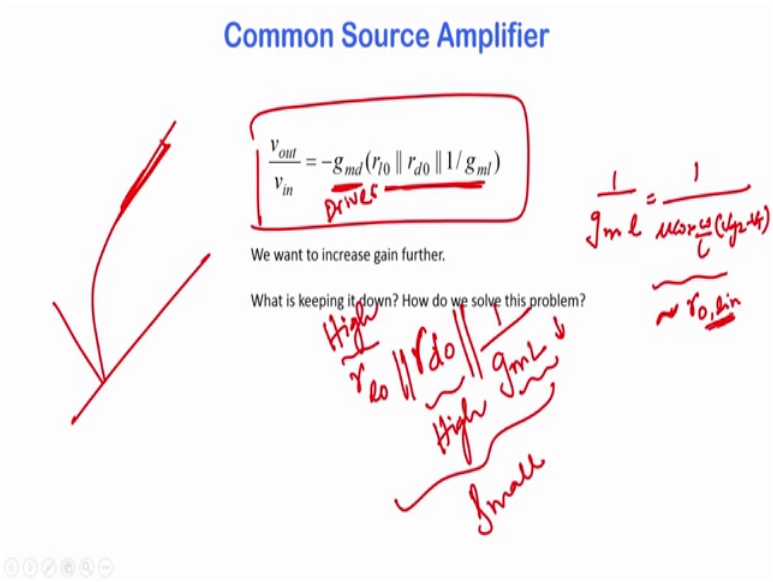

So, the gain has got g m d which is the driver multiplied by a parallel combination of these three resistors. You have RLO, which is high, because it is the output impedance. It is the output impedance of the MOSFET in saturation is very large in parallel with r d o, which is also the output impedance of the driver MOSFET in saturation it is large, but the parallel combination with g m l is going to reduce this entire term.

It is going to make this entire term small, because g m l 1 by g m l is a very small number, why is that 1 by g m l is nothing but 1 by mu C ox w over l into v g 2 minus VT ok. And this if you think of it is numerically, it has got the same numerical value as the output resistance the MOSFET in linear mode. When we looked at the analysis of a switch, and we already know that this is going to be designed to keep it very low.

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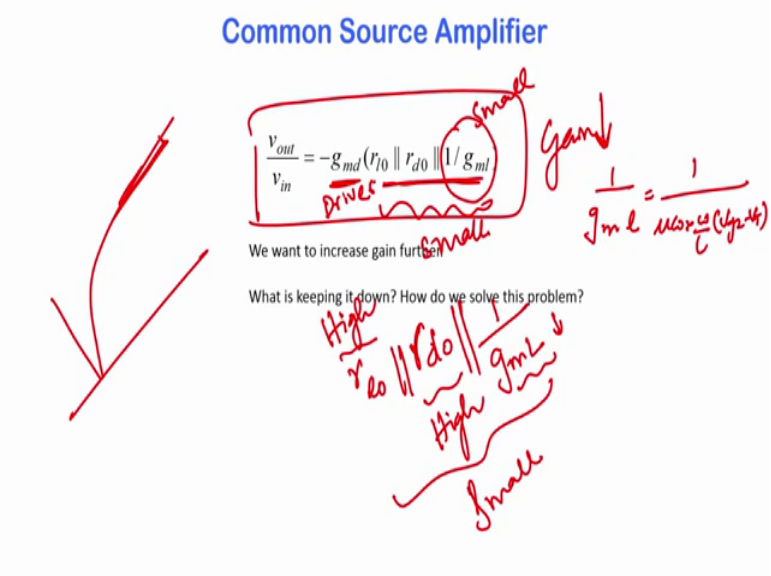

So, 1 by g m l is very small, this is a small term. And therefore this entire parallel combination is going to become small, and therefore the gain is going to become small. If this if only if this g m l, if this term are not present, the gain would be very large. And what is that g m l due to, it is due to the gate to source voltage of this MOSFET of this load fluctuating, because it was an n-MOSFET.

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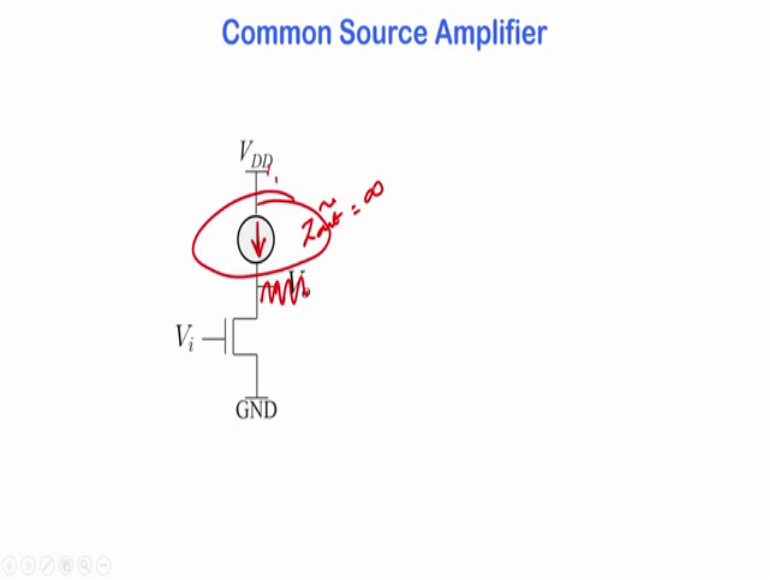

So, how do I get my high gain it looks like adding another n-MOSFET does not work. So, the answer to high gain is to find a device that will give us a current source, so that

no matter what the fluctuation across this device, the current is always a constant, and which means the small signal output impedance is close to infinite so that is the device we want.

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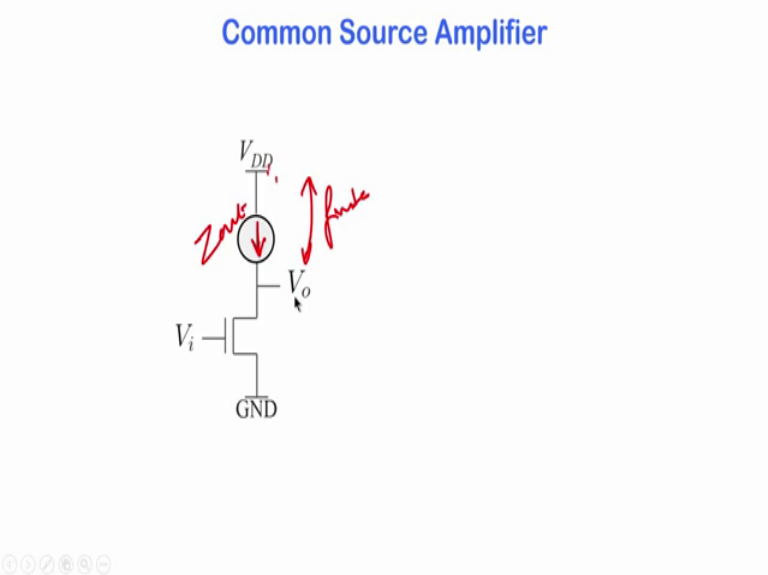

It will give you a finite voltage drop finite voltage drop, but infinite output impedance, so that is the magical device where looking for.

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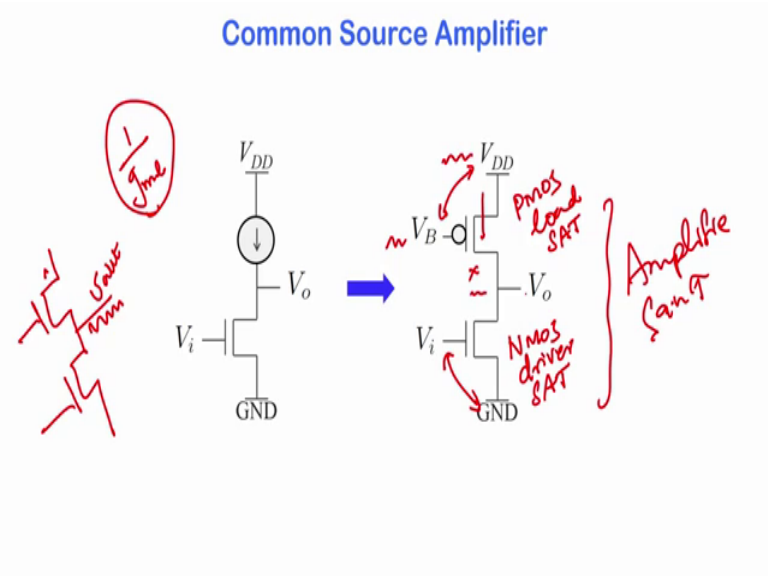

So, from our knowledge of device physics is there a device of that kind, the answer is yes. And the device is a complementary NMOS device. So, you have an you use an

NMOS driver, which is biased and saturation. And we use a PMOS load, which is also biased and saturation ok. And this structure is supposed to be an amplifier that has got very high gain, why is that in the previous case in the case of an NMOS, if we when we looked at the NMOS load, we found that the gain was being killed, because of the 1 by g m l term that is the g m term of the n-MOSFET.

The n-MOSFET was permitting a current through this path in response to the fluctuation in V out. So, we want a device that irrespective of the fluctuation V out the current will the will have no fluctuation or no response, and current through it we want such a device. And we are saying that the PMOS is such a device why is that what is the gate to source voltage of the PMOS, the gate to source voltage of the P MOS is this, the gate to source voltage to the NMOS is this. So, it is only if either this or that nodes fluctuate, well an ideal P MOS have any current through it. So, a fluctuation in V out will not cause a current through the P MOS device ok.

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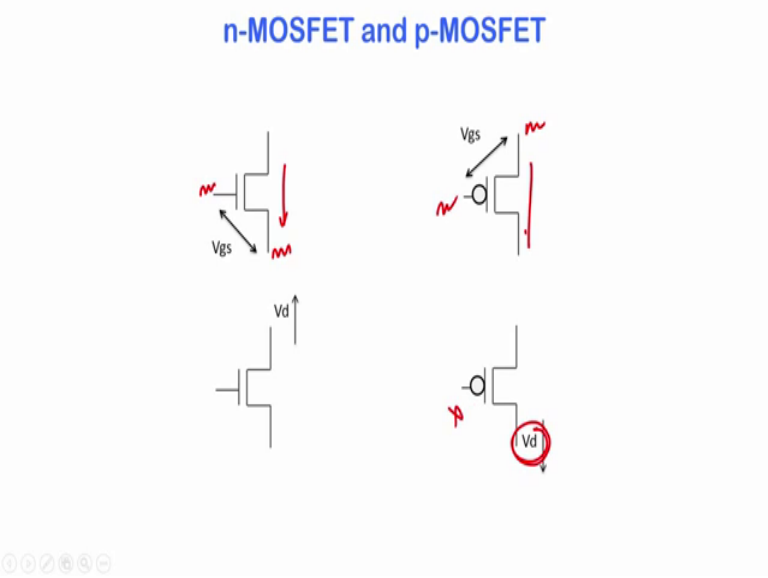

So, in an case of an NMOS device, if either this node or this node where to fluctuate, you will have a current through the device, but in the case of PMOS device it is only when these two nodes fluctuate that you will have a current through it. And therefore, fluctuation in the output node will not cause a current.

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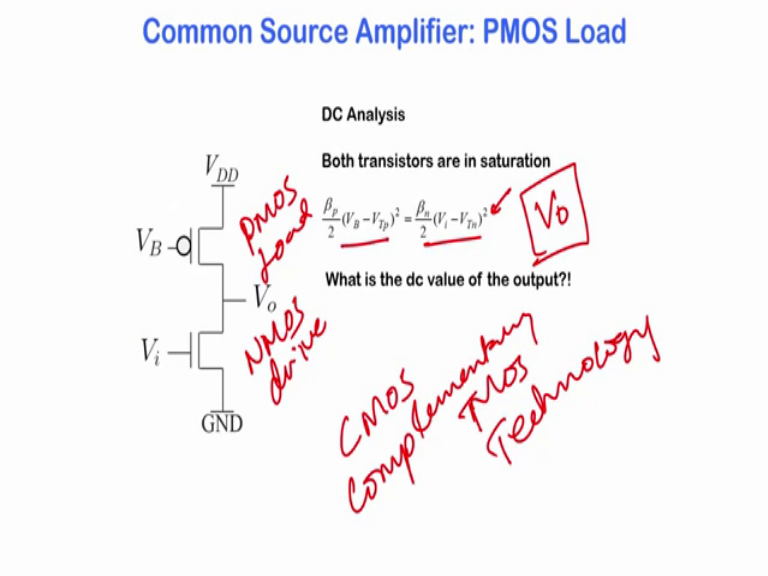

And therefore, it is going to be a device that is going to give you the resistors resistance that you desire. So, once again now, let us analyze a final circuit, which is the amplifier with P MOS load. So, we have a PMOS load and an NMOS driver. It could be the other way around as well.

So, it is basically CMOS technology or complementary MOS technology ok, which is basically the cornerstone of all our digital analog circuits now. So, if we look at this, we have the currents through both the devices being equal. And therefore firstly you will identify that there is no definition for the output voltage. And therefore it becomes quite difficult to bias the circuit, but that being put aside.

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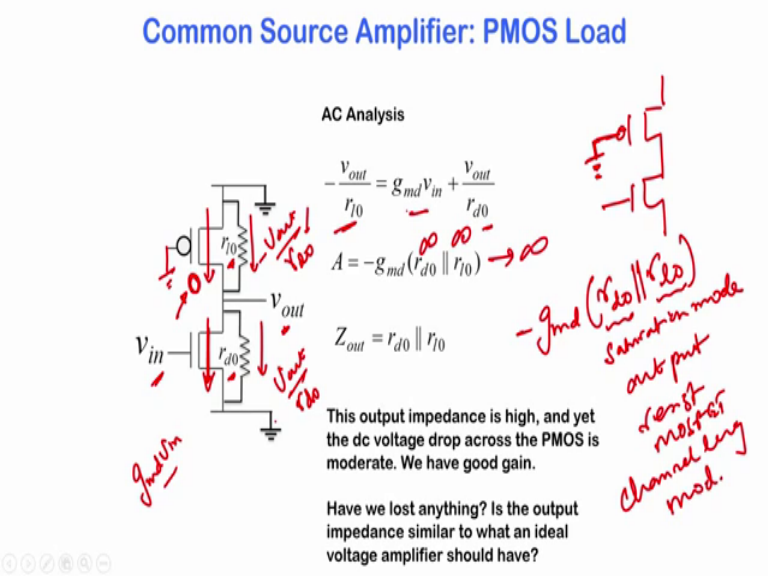

Let us take let us take let us consider the small signal analysis of your new amplifier, which has got a P MOS load and a NMOS driver. So, the P MOS load has got a bias voltage a dc bias voltage no ac fluctuation there, so we just ground it. So, you do not worry about that the power supply is grounded the ground is ground. This is v in that is v out, that is the channel length modulation of the P MOS that the channel length modulation of the NMOS.

And now we see the primary difference, the current through this is the same. It is g m d Vin, the current through this is V out by r d o, the current through this is V out minus V out by r l o, and the current through this is now 0, because neither is this node fluctuating, nor is that node fluctuating. So, the current is now so 0, and that is the fundamental difference between having an NMOS and a PMOS.

And therefore, using Kirchoff's law this current here is equal to gm, this current in this node that is g m d into Vin plus v d v out by r d o. And it turns out the gain is this it is minus g m d into r d o parallel r l o. This is very high and that is also very high, because these are the saturation mode output resistances of the MOSFET. And this is existing only, because of channel length modulation So, if you say that there is no channel length modulation, then this becomes infinite and that becomes infinite, and the gain is theoretically infinite.

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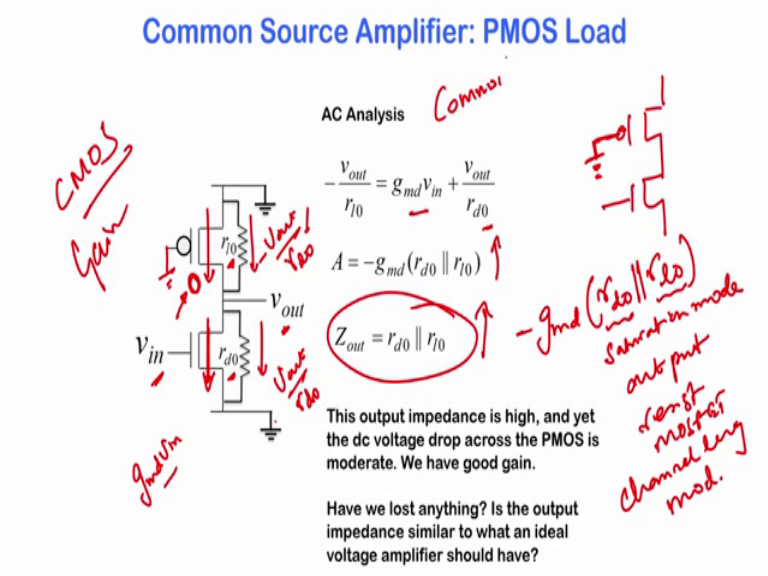

So, CMOS technology can give you very high gain ok, so that is why it is desirable to have CMOS technology. It can give you high gain ok, but does it follow the property of low output impedance the answer is no. The high gain comes with the cost of high output impedance. And therefore, you need to have this circuit give you high gain, and you need to have another circuit to give you low output impedance, which is not going to be covered in these set of lectures.

But if you are interested, then you can look up any book and analog circuits, and you can look up common drain amplifiers, and you know other amplifier topology such as common gate etcetera, etcetera. So, this gives you a brief understanding of amplifier design ok. And to summarize everything you have learned and connect everything to the device physics.

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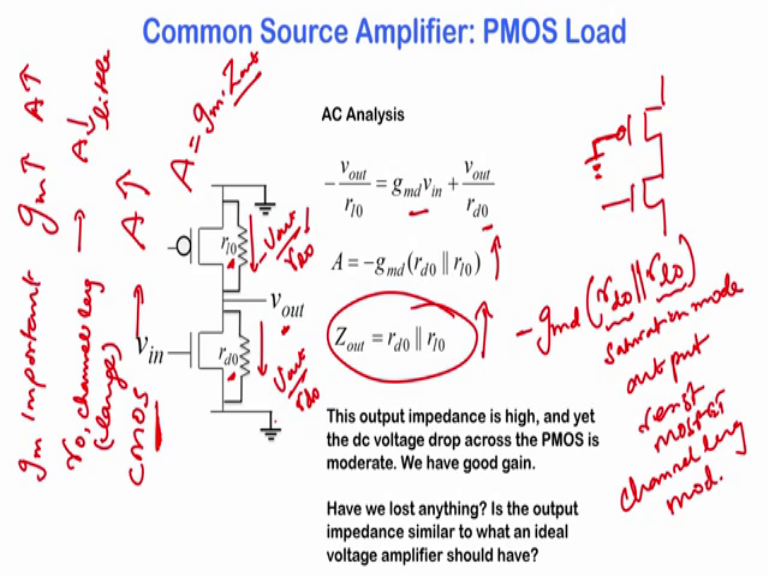

What is the key message? You all know what gm is and how gm is connected, so gm is important. High gm generally implies high gain. The next message is the channel length modulation r o in due to channel length modulation brings down gain a little ok. So, channel and modulation resistance is still large it is large, but it brings down it contributes to lowering the gain a little small.

And CMOS technology can give you very high gain. And the gain for most voltage amplifiers is a combination of the effective trans conductance of the driver, and the effective output impedance of the circuit ok. So, this is the take home message from everything that you have learned. So, CMOS the combination of PMOS and NMOS transistors is a very powerful tool.

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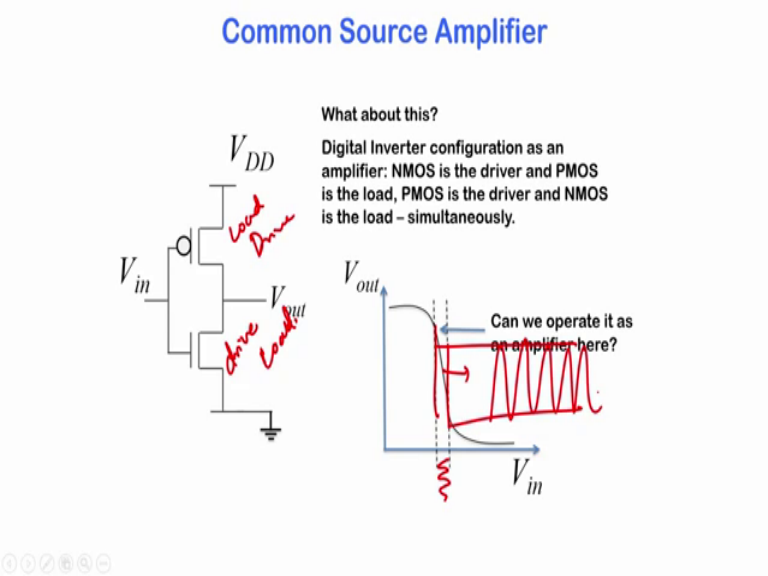

So, here is the summary of you know using the CMOS technology in an inverter configuration. So, if you are all familiar digital circuits, you will find that this is a circuit, which is called as an inverter. And from the point of view of analog amplifiers what we are doing here is we are using the NMOS as a driver, and the PMOS as a load and, also the PMOS as a driver, and the NMOS as a load. So, it is a very powerful very strong amplifier. And you will find that the output and input characteristics look like this. And you can see a region of very high gain. Any small fluctuation in the input will lead to a very large fluctuation in the output.