Semiconductor Devices and Circuits
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Lecture – 47
MOSFET as a switch – Continued

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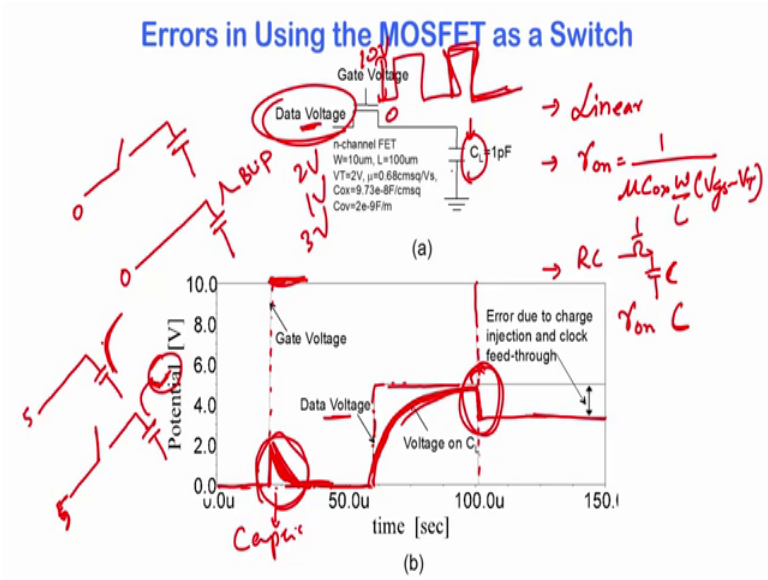

So, we have looked at using the MOSFET as a switch. We are going to operate the MOSFET in linear mode operation, we are we know that the on resistance of the MOSFET small signal on resistance of the MOSFET is 1 by mu C ox W over L into V gs minus V t. And we know that a good estimate of the RC time constant in a MOSFET capacitor circuit is r on into the capacitance of the capacitor. Now finally, what errors could creep? So, here is a simulation or for MOSFET trying to write some data onto the capacitor.

So, take a look at this. So, this curve which I show you here in a red line is the voltage on the capacitor, so that is the voltage on the capacitor. And what do we have here, so here we have the gate voltage. So, the MOSFET turns on at this point. And you see that without anything happening the data voltage is 0, so that is the data voltage ok; so that is the data voltage line. So, the data voltage line is all 0, but the moment the gate voltage turns on, you see this little blip on the capacitor, so why did this blip occur.

And then the moment the data voltage turns on, the capacitor starts acquiring this charge, it starts acquiring charge; it gets starts charging up till the data voltage. You have already seen the RC time constant for this. And then the gate voltage turns off here, the data voltage is still the same. And the gate voltage turns off which means what is happening, the switch was open initially; and when the switch closed, this was 0, and this still 0, when the switch closed, we saw this little blip.

And then some data was provided, we provided 5 volts of data here and this capacitor now started charging to 5 volts. And then suddenly the gate is now open, which means the switch is open; and here you can see the sudden drop in the voltage that was being stored, this is still 5 volts, but the moment the switch opens you see that there is a blip. In fact, the voltage is no longer 5 volts on the capacitor. So, capacitor loses some charge.

So, why does the gate influence the voltage on the capacitor plates? The answer is it is got to do with two different phenomena, which causes parasitic errors in the MOSFET, in a MOS in the capacitor for MOSFET capacitor circuit.

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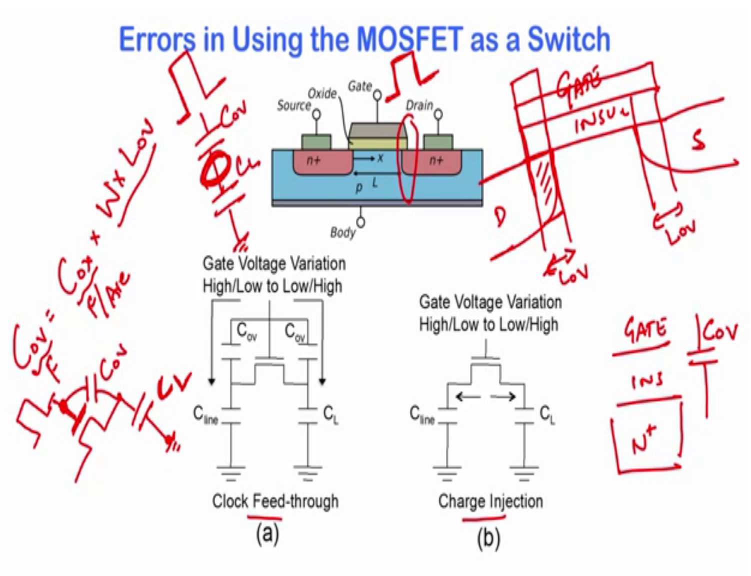

So, the errors are because of two different phenomena which are called clock feed-through and charge injection. And both of them have got to do with the operation of the MOSFET, when the gate turns on and both these both these mechanisms, they create this error and the capacitance during the operation of the MOSFET that is the gate turns on and turns off.

So, in order understand clock feed-through, we need to understand this gate drain overlap region. So, let me just exaggerate the MOSFET structure little. So, we have the gate, we have the insulator and we and if you remember, the region near the source drain so this was the let us say the drain and the source regions. The gate had a little overlap with the drain and source electrodes.

And when we discuss the geometry of the MOSFET, we had marked this overlap region with L overlap; and this overlap is important for the operation of the MOSFET, because it provides complete get field control through the entire channel. And it is all right to have an overlap equal to 0, but the moment you start having overlaps less than 0, then you have regions in the MOSFET that are not controlled by the gate. Therefore, this overlap is necessary, but it is also responsible for all this some of this behavior that you see here.

So, let us look at this cross section here under this overlap. So, what do we have? We have the gate metal, we have an insulator and we have a heavily doped drain electrode, which is essentially a parallel plate capacitor. So, essentially you have a capacitor which is we which we call as the overlap capacitor, and what is the capacitance of this overlap capacitor; it is basically your C ox, so if you measure this in farads, C ox is the capacitance per unit area, and area which we need is W into L overlap, so that is the area we are talking about.

So, this overlap capacitor appears across the gate, it couples the gate signal to the source and drain electrodes. So, if this were to be your circuit, if this is the switch capacitor circuit that we are looking at. So, let us say that is the capacitor and we are observing all the voltages on this capacitor, and we saw that there were some blips coming in and going out.

So, what the circuit that should actually be drawn, is the circuit with having this overlap capacitance between the gate to the drain. And now from this circuit you see that when you have a gate voltage that is fluctuating. So, we saw the gate; when the gate voltage went up, we saw this blip and the gate voltage came down, we saw another blip. So, when the gate voltage goes ups up and down you have a transient or time varying voltage across these series capacitors, which is C overlap and your load capacitance, so that is your C L that is the load capacitance.

So, we have these two capacitors and series and you have a gate voltage that is going up and coming down. And it is this voltage that is creating a fluctuation on your load capacitance. So, when the voltage when the gate voltage climbs up you see that there is a transient and the C overlap is coupling the gate charge to the C to the load capacitor. So, you have this quick transient and the moment the voltage stabilizes, there is no more current through the capacitance series, capacitor circuit and the current quickly dies out to 0, so that is one mechanism. What is the other mechanism, the other mechanism is charge injection. So, let us imagine there is a puddle of water.

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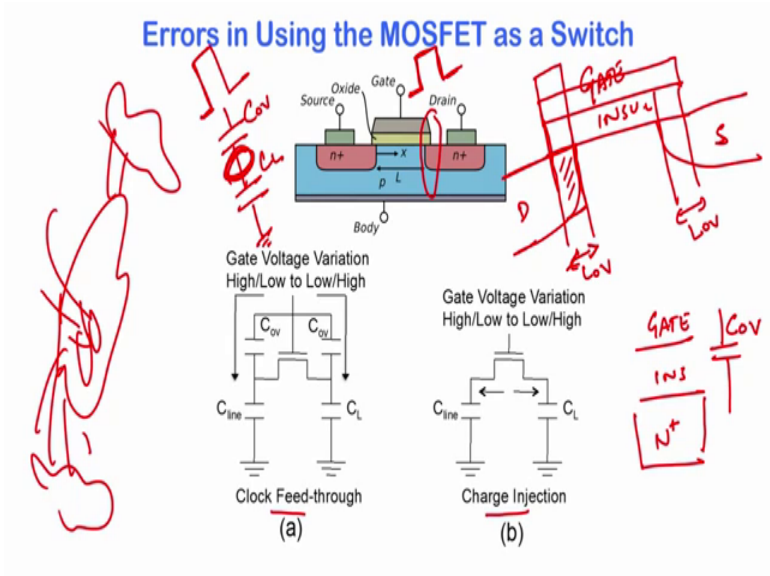

And so let us have a little puddle of water. And let us say a child were to jump into this puddle, you will automatically see that the water will also splash out and it will all head to the sides. So, the charge injection mechanism is a bit like that.

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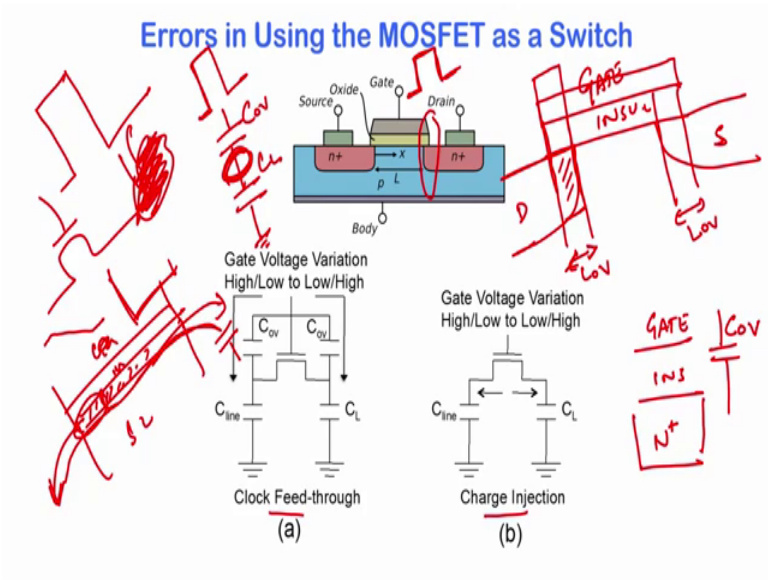

When the gate goes high so we have a MOSFET when the gate voltage goes high, inversely layer charge is formed, where did this inversion layer come from, where did the charge in the inversion layer come from; the inversion layer charge came in from the source. And the moment the gate voltage goes off, the inversion layer has to disappear. So, you have a lot of charge sitting here you have the gate, insulator, semiconductor you have a lot of inversion layer charge sitting here.

And the moment the gate switches off, this is the inversion layer charge has to leave this place. Now, where does the inversion layer charge go back, it goes back to the source and drain electrodes, there is nowhere else for this charge to go, so this charge here is you like a little puddle of water. And the gate turning off is the child jumping in and trying to get the puddle of water out of that place, and the puddle and this little puddle of charge they just moves to the source and drain electrodes.

Now, if you were to gently turn off the gate, and give this charge enough time. So, you turn off the gate very slowly, you turn off the gate very slowly. And you give all this charge enough time to realize which is the low impedance path, which means with the line the part which is got a larger capacitor then you will find that most of the charge goes to that part and very little charge goes to the low impedance or the higher impedance path.

The basically the charge distributes itself, you have a current that distributes itself depending on the external impedances, but on the other hand if you were to turn off this gate very rapidly, you do not give enough time for the charge and you will find that an equal amount of charge exits the source and drain electrons.

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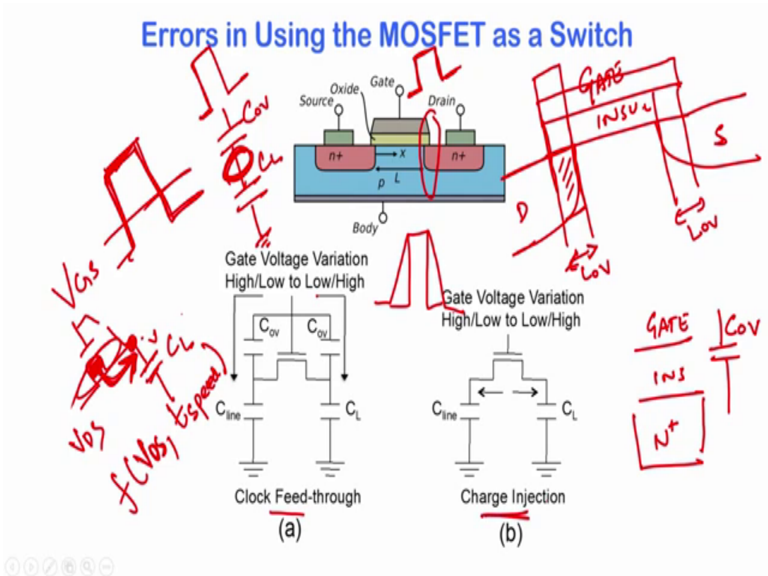

So, you now have another mechanism which corrupts the charge on the charge store on the capacitor. So, we had this capacitor load capacitor, we already saw that by turning off the gate, whatever charge this gate transient caused a current through this path and it created an error on the stored charge in the capacitor; but there is another error and that is the charge in the channel will also exit the MOSFET, and will also jump into this capacitor here, and it will also corrupt the data on the capacitor.

Now, which of this is a bigger problem? The bigger problem in some sense is the charge injection, why is it bigger; the clock feed-through mechanism, the amount of error it creates is fixed if you have fixed your gate voltage, or your select line voltage. If the V GS is fixed, it does not matter how rapidly the gate transits, it does not matter what your V DS is, if this is fixed, your error here is fixed.

And therefore, this error can be corrected off as an offset if you know what the gate voltage levels are, and you know what your overlap capacitance is, and you know what your load capacitance is, in some sense you can correct this error of as an as an offset, it is an offset error; and you can just overcompensate for this offset, but on the other hand the charge injection depends is a function of the drain to source voltage.

There is the data that you are applying, that is the data. And this data could vary from one operation to the other; it could be 2 volts, now it could be 1 volt; the next second, it could be 3 volts etcetera, etcetera. Whereas the turning on and turning off is generally constant, you know the MOSFET will always turn on at a fixed voltage, let us say 10 volts to 0 volts, this turn on voltage the MOSFET does not change. You would not keep the MOSFET in linear mode of operation and so that really does not change too much.

So, this charge injection error, the amount of charge stored in the channel depends on the drain to source voltage. And the amount of charge exists exiting the channel, also depends on the speed; the turning on and turning off speed of the gate signal. The gate signal would turn on slowly, and turn off slowly; you will have a different error. And if it turns on quickly, you will have half the channel charge entering the capacitor. So, because of these two reasons its quite hard to predict the amount of charge in the amount of charge injection, its quite hard to predict it.

So, therefore it is a problem in itself, but if you just look at the quantity so, here you have the overlap capacitance that is the charge that is coupling through, but here you have the entire channel region, entire channel charge its coupling through. So, for these reasons both these, I mean the charge injection is a little bit slight slightly more complicated than the clock feed-through phenomena, but nevertheless these two are very well studied.

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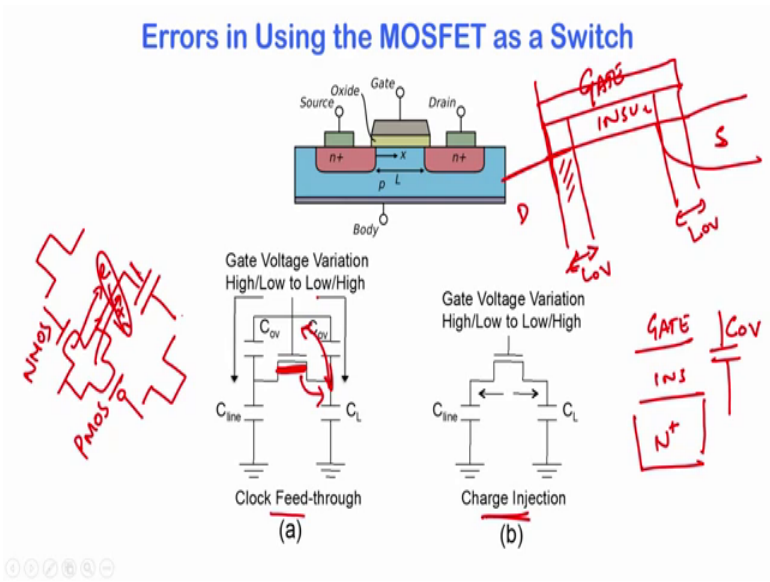

And there are several techniques to compensate for both. In fact, for charge injection it is very useful technique is to have a complementary device so, for example and you provide this complementary device with the opposing signal. So, let us say the gate goes on and off here, you know the clock drives the opposing gate. So, which means that when electrons come out of this holes also, an equal number of holes also come out of the complementary device which is basically your P-MOSFET, and that is your N-MOSFET.

And you have electrons and holes and therefore, you do not have any charge injection. So, there are techniques to overcome these, but nevertheless it is a problem that you should be aware of.

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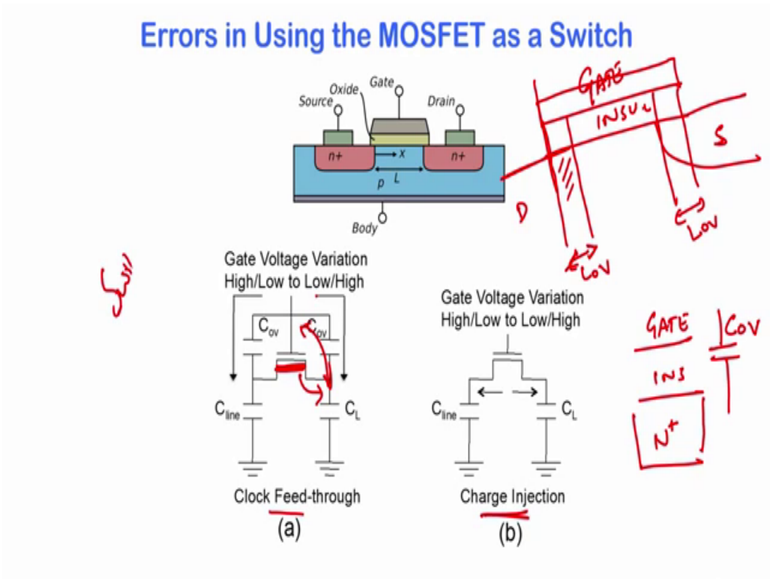

So, with that we will conclude our discussion on the use of the MOSFET as a switch.

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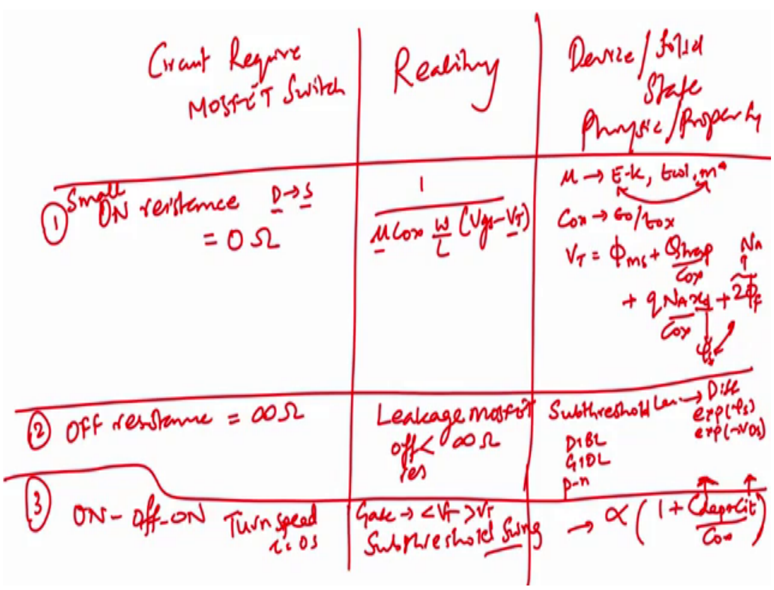

So, to summarize let us see what connections we can make with the circuit application. The circuit requirements of the MOSFET as a switch, the reality of what can be expected, and the device or solid state, physics or the property that governs this, that governs this connection. So, here is the connection between circuit requirement and the device physics.

So, the first thing what is the ideal property of a switch, when the switch is closed? So, let us say what is the on resistance of the switch that is from drain to source; since, we are using MOSFET we will just say drain to source. Now, what we would really like is that this be 0 ohms. So, we are talking about small signal resistance, let us say small signal resistance, we would like it to be 0 ohms; but in reality it is 1 by mu C ox W over L into V gs minus V T. And the connection to each of these terms you know, I already elaborated upon each of these terms.

So, mobility comes from the E-K diagram, and it is dependent on your tcol and effective mass, so that is that is the connection to the E-K diagram. And C ox is basically your epsilon ox by t ox, and V T is basically your flat band voltage which is phi m s plus the trapped charge in the insulator plus the depletion charge q N a x d by C ox plus phi F which is connected to which depends on N a; and x d also depends on 2 phi F on the surface potential which is again connected to 2 phi F during turn on; so that was the connection there.

The second point is what is the off resistance of the switch? So, when the switch is turned off, what resistance would be ideally like, we would like infinite ohms, but is that the case it is not, because we have leakage mechanisms in the MOSFET. And we already did an exhaustive study, not an exhaustive study at least we did a introductory study on all the different leakage mechanisms.

We had leakage through the gate let us keep the gate aside for now. We had sub threshold leakage, which we found was due to diffusion of carriers and had an exponential dependence on the surface potential, and exponential dependence on V DS etcetera. And we had other mechanisms like you know, we had mechanisms like drain induced barrier lowering, and gate induced drain leakage, and leakage through the p-n junctions at the source drain contacts, it is the contributing to the leakage currents. And therefore, definitely the off resistance of the MOSFET is much less than infinite.

Third, what about the turn on speed we want that switch to go from on to off, and to on very rapidly right, we want what is the turn on speed of the switch. We would like it to be ideally we would like it to be 0 seconds, but is that truly the case it is not. So, if we take the MOSFET alone. So, when the gate goes from you know below V T to above V T, what is the turn on speed dependent on; it depends on the subthreshold swing of the MOSFET.

And what is the subthreshold swing depend on, subthreshold swing is proportional to 1 plus C depletion plus C, interfacial trap by C ox. So, if your depletion capacitance is large, and if and which can which can happen if your x t is small, which can happen due to high doping. And if your interfacial trap capacitance is large, then your sub threshold swing becomes very large ok; which means that you need a larger gate voltage to make the current climb up by 1 decade. And then what else did we see? So, let me just find some space here. So, let us since we have understood what V T is, let me just erase that.

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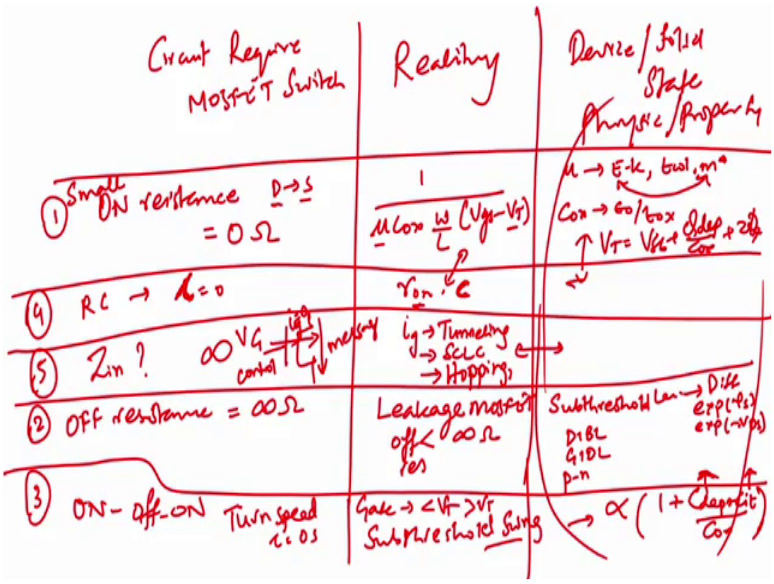

So, what about the turn on speed in a circuit? So, you have a MOSFET RC circuit, the turn on speed is typically your r on into the capacitance. We would ideally like it to be 0, but it is not going to be 0; it is going to be r on into capacitance, and we have already defined what r on is, so that it is the same answers that and is there anything else. So, we would so these are the key parameters.

So, you would also like other things like for example, we would like know parasitics, and we would like we would like that the MOSFET be able to take infinite amount of current, when it is on; and have an infinite voltage drop, when it is off etcetera, but these are all related to these basic device properties. And you see that the reality is quite different from what one would desire as a circuit designer, but nevertheless these are important.

And just one more thing though, one more important property which is, what is the input impedance of the MOSFET so, let me call it impedance, input impedance of the MOSFET. We would ideally like it to be infinite, so what do you mean by input impedance we mean that the gate current is 0. We do not want the gate to be the control signal to be influencing any message that is going in from source to drain. We would like this current to ideally be 0.

But is it truly the case? It is not, because you have leakage mechanism such as tunneling, you have space charge limited currents to the dielectric, you have you know other mechanisms like hopping, and mobile ions, and trap charge and the dielectric etcetera, etcetera. So, therefore, this two is not close to ideal. And that the key is that you understand what the values are, and you understand the demise physics and the material and these solid state properties that control these different aspects.