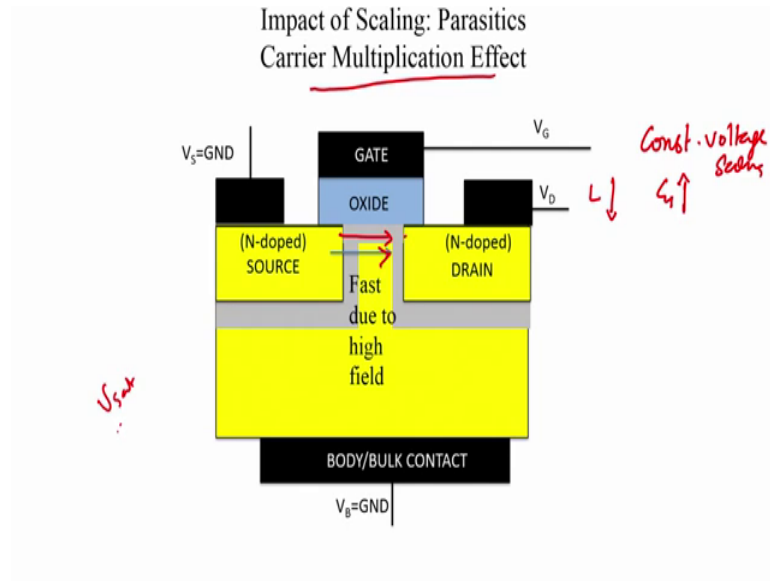


Semiconductor Devices and Circuits
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Lecture – 43
Scaling of MOSFETs - Continued, Leakage currents in MOSFETs

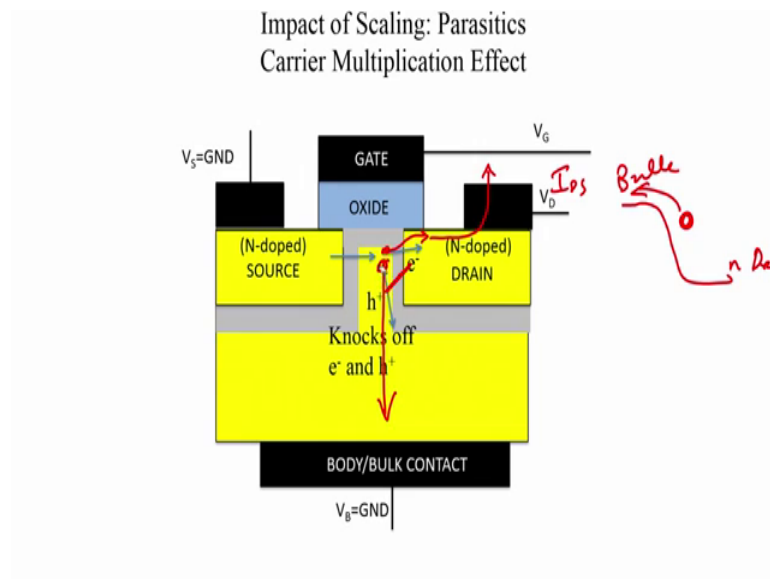
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So now, what are the impact of scaling hap? So, now, let us look at some parasitics carry a multiplication effect ok. Now what happens? So, this is a very interesting phenomena, which is a there is a possibility for positive feedback here, which can actually destroy your device. So, if you make the channel length of the device, very small the electric field between the source and the drain starts increasing ok. So, this electric field becomes larger and larger.

So, let us say we have used constant voltage scaling and we have reduced the channel length of the device ok so, V is a constant voltage scale. Now this high electric field makes these electrons travel at a very high velocity. So, in fact, the electrons will now be traveling at the saturation velocity.

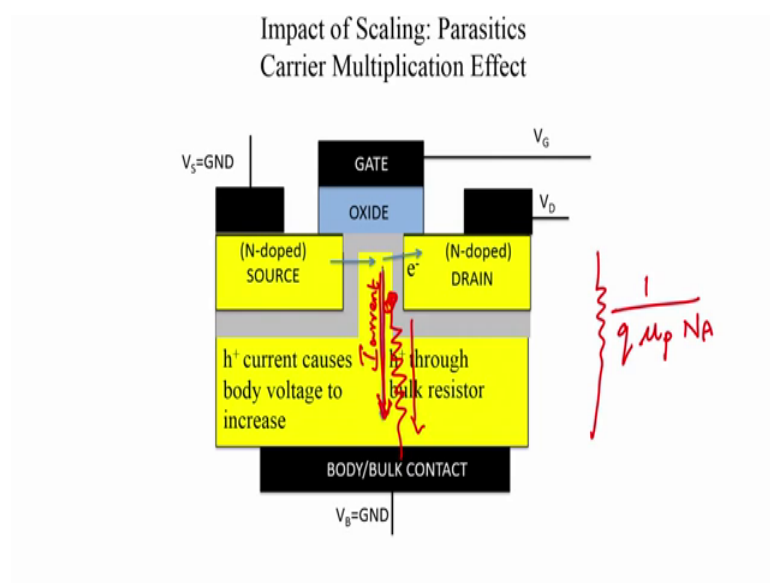
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And due to this very high velocity there is a possibility that these electrons can impact other silicon atoms and can free electrons and holes ok. So, you can have impact ionization they can knock off electrons and holes from silicon atoms ok. So, now if an electron and hole pair is created if an electron hole pair is created here, the electron would quickly run away migrate through this and enter the drain ok, it will just simply contribute to the IDS.

But, what does a hole do? The hole sees a pn junction here ok, it sees sorry sees a p type bulk and an n type drain that is bulk and let us say the hole was created here is going to run upward and into the bulk ok. So, the hole is going to migrate away into the bulk. So, if the hole migrates into the bulk ok, if let us say, there are several holes and electron pairs created and a lot of these holes start migrating into the bulk.

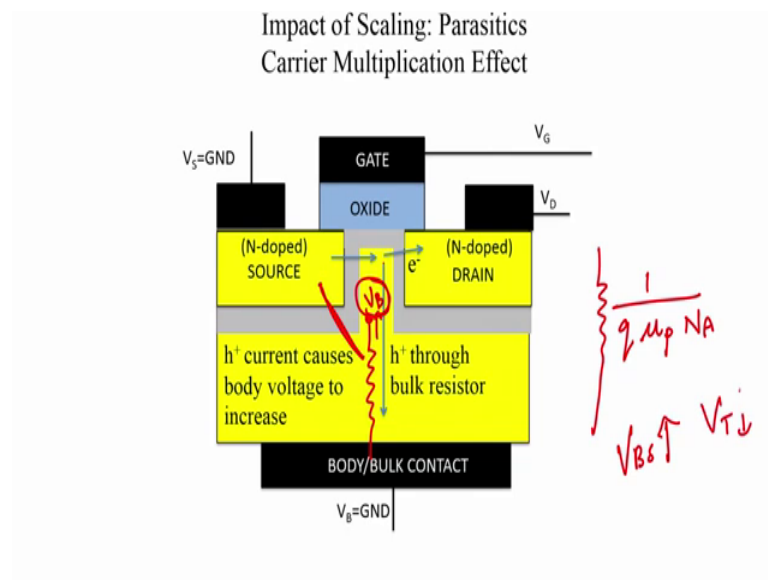
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They are essentially going to create a hole current here. So, essentially you are going to have a current, flowing inside the bulk and this current is because of the holes. And the bulk has a certain resistance ok, because it is doped n type it is doped p type. So, it is going to have a resistance of resistivity of $1/q\mu_p N_A$ and depending on the geometries is going to have a certain resistance.

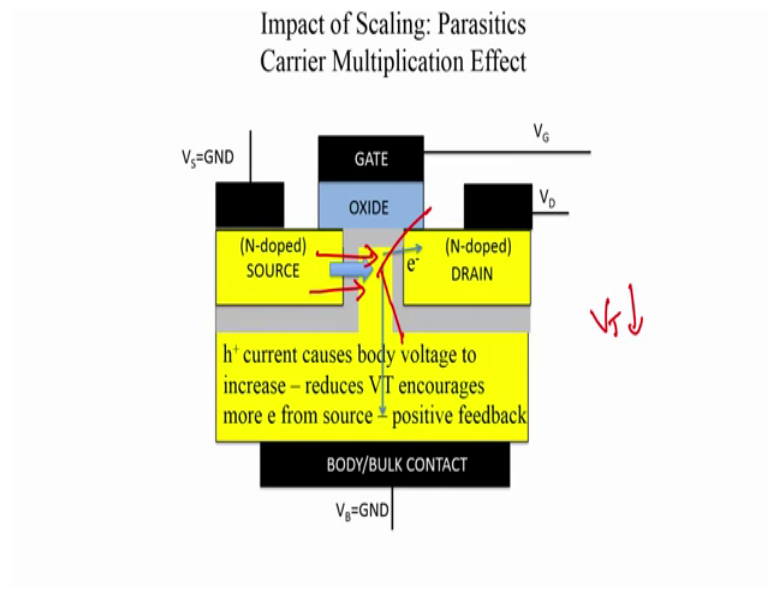
So, there is a certain resistor here and you are going to have a current flowing through, this resistor and what does this current do? It is going to increase this potential here so, the larger the current the larger the potential ok.

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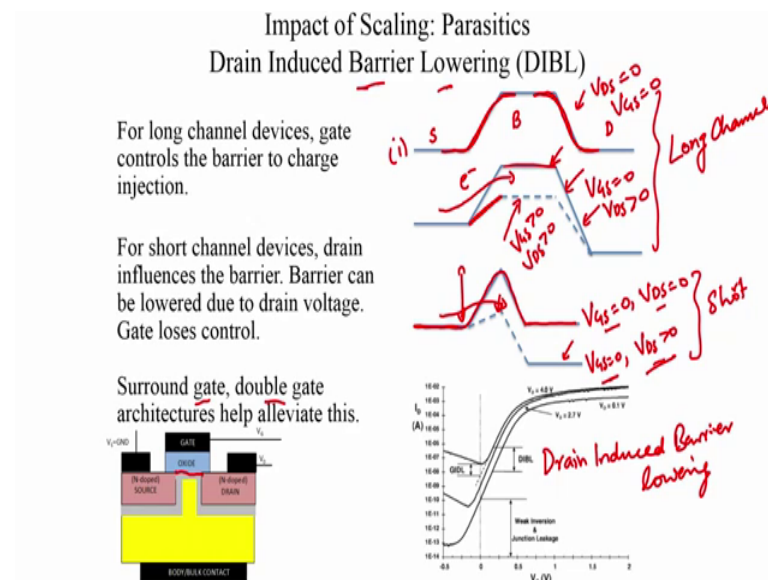
So, essentially we have a whole current flowing through the bulk. The bulk has some resistance and therefore, this potential of the bulk begins to increase if this whole current increases. So, if V_B , which is the potential the bulk starts to increase the V_{BS} starts to increase and what happens V_{BS} starts to increase? V_B starts to increase, this junction gets forward biased and it is going to reduce the threshold voltage.

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If VBS starts to increase is going to reduce the threshold voltage and if you reduce the threshold voltage, you are going to encourage more carriers, more electrons to get in from the source. And this is going to further create more electron hole pairs and this positive feedback mechanism can simply lead to an instability, which will eventually destroy the device.

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So, there is a possibility of this happening, if the device is not very carefully engineered by using correct scaling principles. So, the next parasitic due to scaling is something called as drain induced barrier lowering and the idea here, is you know, if you have a say long channel MOSFET. So, here were looking at band diagrams for long channel MOSFETs ok. So, the drain and source are far apart and the case you are looking here, the case 1, we are looking at is here, you have a source electrode, there is the body and here is the drain electrode.

And if you think of this pn junction, you have a pn junction here and you have another pn junction here and in order to inject carriers, this is at equilibrium, this is when there is no VDS applied. And there is no VGS applied and when we have to, when we increase the drain to source voltage, all that happens is that all these barrier heights remain the same, but the drain to source voltage increases and therefore, you see that, this pn junction is now strongly reverse biased and when we apply a gate voltage.

So, this is the case, when VGS is still 0, but when VDS is greater than 0 and now when we apply a gate voltage. So, when we bring in the gate voltage, when we make VGS greater than 0 and VDS greater than 0, we lower the gate voltage helps to lower this barrier and therefore, encourages electrons to come in from the source. So, that is the normal operation of a MOSFET. Now when we head towards short channel MOSFETs ok, the drain starts getting very close to the source. So in fact, if this is the depletion layer of the source, then you can see that drain depletion starts immediately and that is the band bending ok.

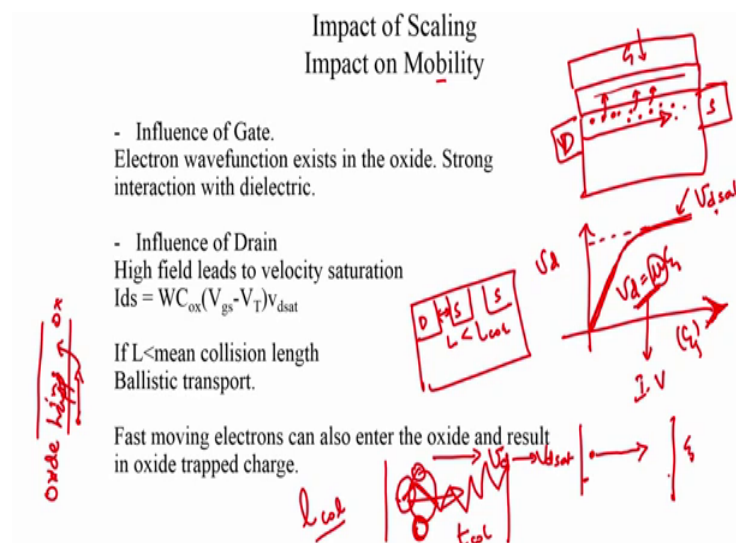
So, the band bending at the condition when VGS is equal to 0 and VDS equal to 0 for a short channel device would look, somewhat like this of course, I have used straight lines simply because, it is easy to draw, but you could imagine a very strong interaction between the depletion region at the drain side and the depletion region at the source side. And without the application of VGS so, this is all at VGS equal to 0 and VDS equal to 0, if VGS is still kept at 0 and VDS is made greater than 0, then what we would expect? Is a band bending of this kind.

Now, as we see in long channel devices, we do not want VDS to actually influences barrier height near the source side. But since these 2 depletion regions are so, strongly coupled because of the short channel, you see that when VDS is greater than 0, the VDS itself, the VDS field itself influences, this barrier height. And this barrier height is lowered because of VDS, without VGS being applied and that is a problem because, now what we are doing is? We are taking control away from the gate, the VDS itself controls the barrier height. And this is something called as drain induced barrier lowering, where the drain to source voltage lowers the barrier for carrier injection and you start seeing electrons get in even, when VGS is 0.

So, this is a very significant you know in some sense, it is a leakage mechanism, it can lead to leakage because, if you look at the IV characteristics. So, here is an IV characteristics for a very low VDS and the moment VDS is increased to something that is quite significant. So, let us say here, the VDS is increased to a larger value, you find that there is significant change in the currents, the device turns on at a different point and it also produces a larger amount of current.

So, this is something called as drain induced barrier lowering and in order to alleviate this problem, what happens is you know the how do we you know get the gate to have more control? So, you want to not only have the gate having an interface with just one surface layer, but you know you come up with architecture such as surround gate or double gate MOSFETs etcetera, to sort of reduce this impact of the drain and allow the gauge to have a significantly larger control on the carrier injection.

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So, with that we you know cover these topics on the impact of scaling on different parasitics and we will now look at our studies on the impact of scaling on mobility and then head towards the other topics on MOSFETs. Now, with regards to mobility there are 2 influences right. So, you have two fields in a MOSFET that control the carrier movement, you have the gate and then you have the source and drain voltages.

Now, if the gate voltage is increased, you increase the interaction of these carriers of these electrons with the insulator. And this becomes particularly strong, when the insulator thickness is reduced during scaling and the drain to source voltage also; obviously, impacts the I know the movement of the charge transport of the carriers and at low fields the velocity, the drift velocity of the carriers is defined by the mobility. So, if you remember the plot of drift velocity versus electric field at low electric fields, you have this almost linear relation with the electric field with the drift velocity being mu times the electric field and this was the relation that, we used to derive the current voltage characteristics of the MOSFET.

But, in short channel MOSFETs it is very likely particularly, if say constant field scaling is not deployed and if you say, if you use constant voltage scaling it is very likely that the velocity saturates as because, the field is very large. So, the current voltage characteristics is, then determined by the saturated drift velocity, that is $V_{d sat}$ and not. So, much by the mobility and. In fact, the current voltage relation here, this is drain to source colored is given by basically, the total charge present in the channel into $V_{d sat}$ ok. So, this is the charge per unit area into W into length per unit time will determine the current through the drain and source.

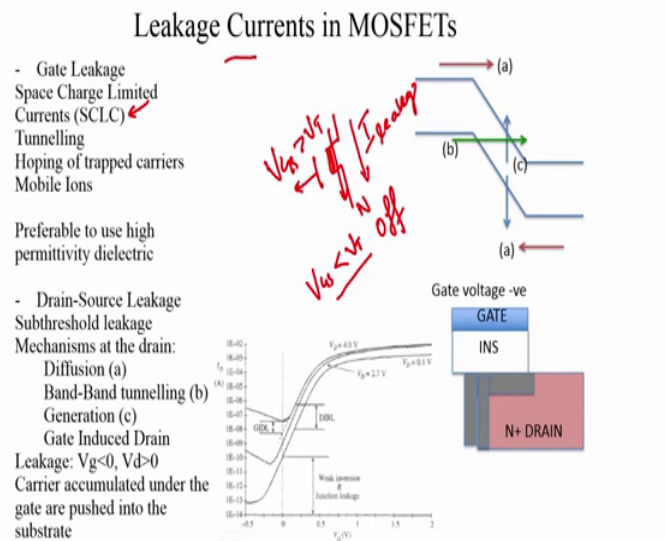
Now, if the channel is reduced to such an extent. So, if you take your drain and source terminals and you start bringing them closer and closer ok. So, you reduce L to such an extent that L becomes smaller than the mean collision time, mean collision length of the carriers, then we enter into a very different physics of operation. So, what we are saying is that normally, these electrons would when you when you keep an electron in vacuum, it experiences a force and therefore, it accelerates. But in a semiconductor lattice the electron undergoes all these scattering events, it call as it scatters with the lattice defects,

it scatters with the lattice atoms, it scatters with the I mean you have a electron scattering etcetera.

And therefore, because of all these scattering events, we saw that the electron experiences a effective drift velocity and as the electric field is increased this drift velocity saturates, because the electron is still undergoing these scattering events. But, if you reduce the channel length and these scattering events, you could say that they have a mean collision time of t_{col} and a mean collision length of $l_{collision}$. If the channel length of the MOSFET, that is if this distance between drain and source is reduced to less than, the mean collision length then, it is very likely that a large number of electrons, do not on average experience any scattering and these electrons would simply shoot past without experiencing any scattering.

So, we have brought in the channel lens to within you know these mean scattering lengths. And therefore, in these regions the electrons could accelerate and in this case, the transport is called as ballistic transport. So, under very high fields electrons could move so, quickly that they can also enter the oxide. So, you have very high velocity electrons, they have got very high energy and one consequence of that is you have an insulator here and you have your semi conductor and these high velocity electrons are got enough energy to get into the oxide and they essentially become your oxide trapped charges.

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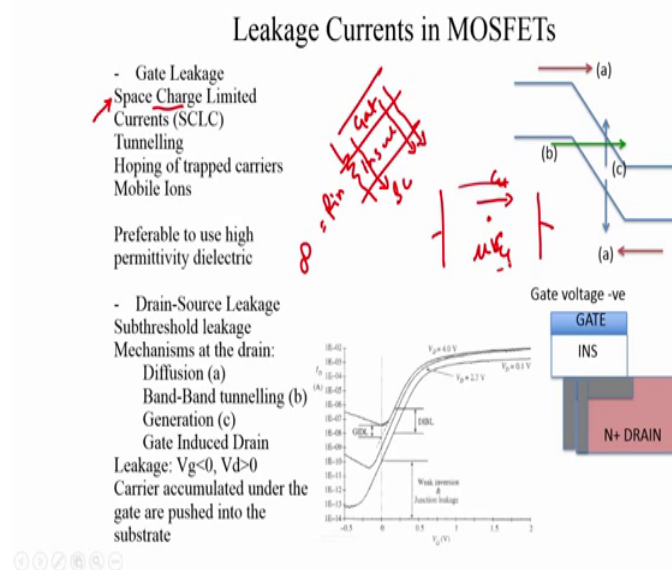


So, these are all the consequences of having a having a combination of short channel effect as well as having high fields and their impacts on the mobility of carriers. So, as a final topic with regards to the physics of MOSFETs, let us just look, you know just sort of let us very quickly look at the different mechanisms of leakage currents in MOSFETs ok. So, leakage currents in MOSFETs is an exhaustive lecture by in itself and because, we constrained with regards to time we cannot talk about this so, exhaustively but although, we will touch upon certain topics particularly things, like space charge limited current, we will have a special lecture on that. But as such we will only spend this one slide on understanding the different mechanisms of leakage currents in MOSFET.

Now firstly, why are leakage currents, why the study of leakage current so important? It is important because, when you have MOSFET and when the MOSFET, when let us say, you have a N channel MOSFET, when V_{GS} is greater than V_T , the MOSFET is said to be on and you are supposed to have a current through the MOSFET. And when V_{GS} is less than V_T , we technically want the MOSFET to be turned off, we want all the currents in the MOSFET to be as low as possible.

But in reality that is not the case ok, we do have leakage mechanisms, we do have leakage of charge through between the drain to source even, when V_{GS} is less than V_T and these mechanisms contribute to leakage currents. So, what are the different leakage mechanisms? So, first let us look at leakage through the gate ok.

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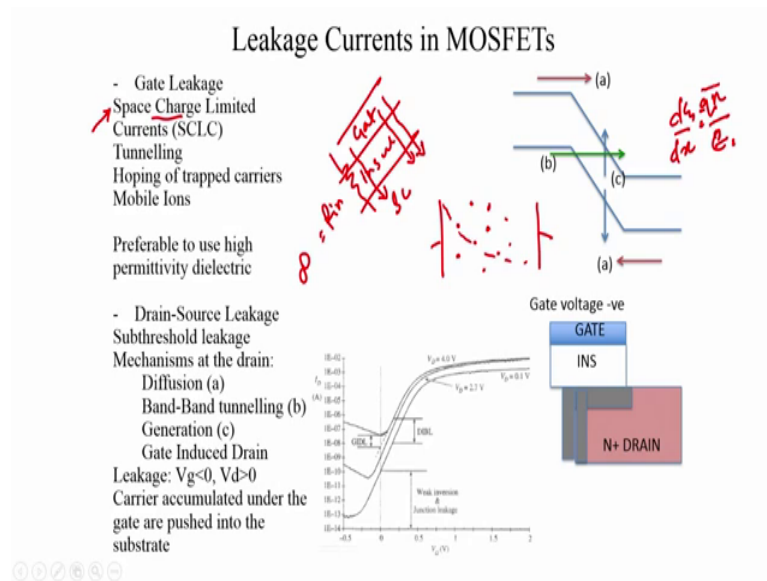


Now if you look at gates if you look at the insulator, the insulator was in place to make sure that the input resistance to the MOSFET was theoretically infinite at least at low frequencies ok. But in reality you do have the insulator leaking charge; you do have a small amount of current from the gate to the semiconductor.

So, what are the mechanisms by which a current can exist through this insulate? The first mechanism is something called as space charge limited currents. It is a drift driven charge transport, but it is called space charge limited, because depending on your structure ok. So, depending on the trap state density inside the inside the insulator or you know depending on the quality of the insulator, you could have different mechanisms of transport, where the transport is limited by space charge which is in this case, the electrons themselves ok.

So, the idea is this, you have an electric field across say 2 plates and you inject a lot of electrons inside ok. Now, what is the electric field felt by an electron here, and what is the electric field felt by an electron here? Now if there was only 1 electron present in this region, we would say that the electron experience, a certain field and therefore, it is got a certain drift velocity. So, if this is a semiconductor, it is got a certain drift velocity which is μ times the electric field and this contributes to the current.

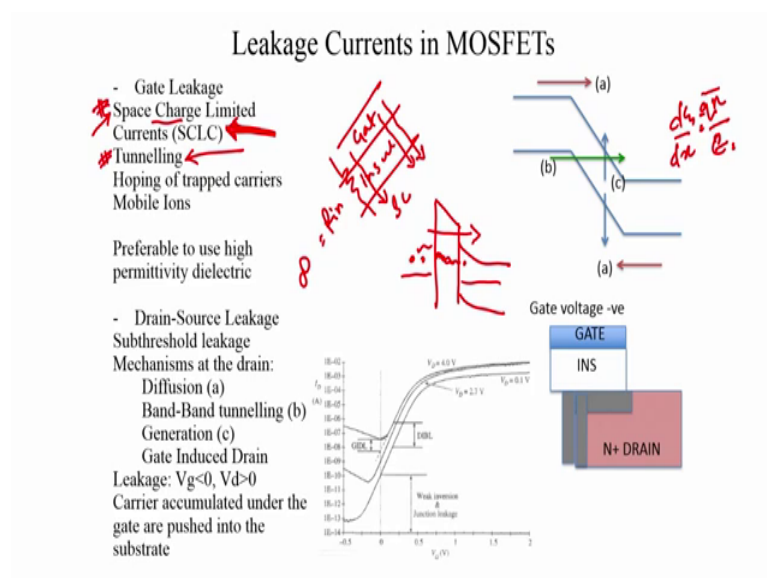
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But, on the other hand, if there are several electrons present and this electron these electrons from a very sparse pathway between these two terminals, then you need to solve Poisson's equation here ok, we need to write Poisson's equation, in that region to say that, the electric field distribution in that region is defined by the charge distribution in that region. And therefore, note all electrons will see the same field and therefore, this current is determined by the space charge, which is basically this charge distribution in this region and therefore, it is something called as space charge limited current.

Now, we will have a special lecture that identifies different means or mechanisms and models for space charge limited currents, but this is one of the methods of charge transport through the insulator. The other method that you are familiar with is tunneling.

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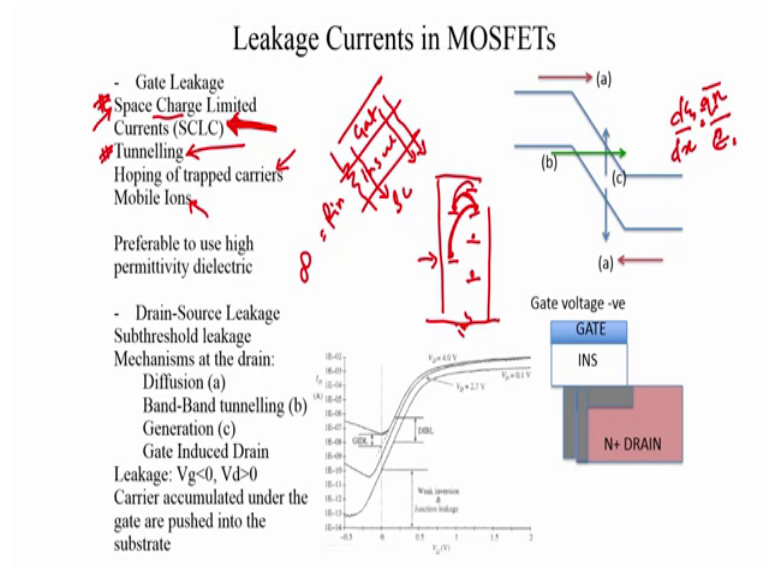


So as we saw since the insulator is a barrier ok. So, let us say you have your metal semiconductor let us say, we have turned off the MOSFET so, the gate voltage is 0 or

less than 0. And the MOSFET is supposed to be technically off ok, but you still have electrons, these electron wave functions can exist inside through can penetrate this barrier and can these electrons can appear on the other side and therefore, this leads to a current through the insulator and that is due to tunneling.

So, this is another mechanism of charge transport, through the insulator the next something called as hopping and this is again something a topic that, we will briefly talk about when we when we have a lecture on disordered semiconductors.

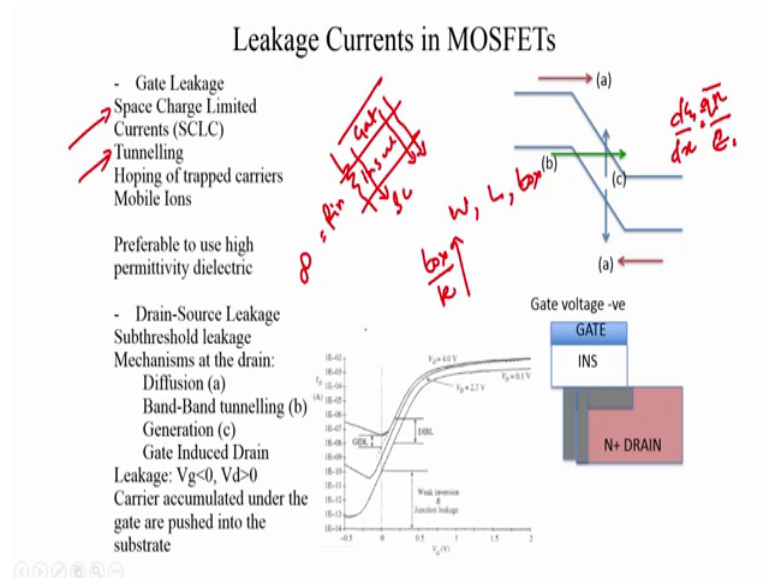
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So, the idea is you have an insulator and let us say the insulators defective. So, you actually have energy states inside the band gap of the insulator and these energy states can act as little homes for electrons of any carriers and the carriers can hop between these energy states. And this hopping can be encouraged by the field and it is determined by the energy level differences between these states as well as the spatial distances between these states.

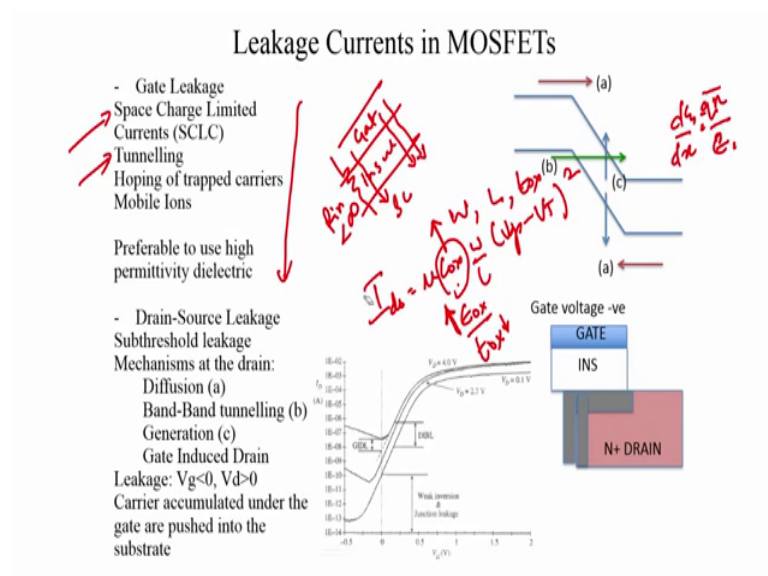
So, there are many mechanisms that determine hopping ok. So, that is another mechanism of charge transport through the insulator and finally, you have mobile ions which can also contribute to gate currents. So, these are the different mechanisms by which through which you have currents through the insulator.

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Now when we scale down the MOSFET the idea is to scale down. W , L as well as t_{ox} and when the thickness of the oxide is scaled down by a factor of k mechanism such as tunneling and space charge limited currents are all supposed to increase and they will increase quite significantly ok.

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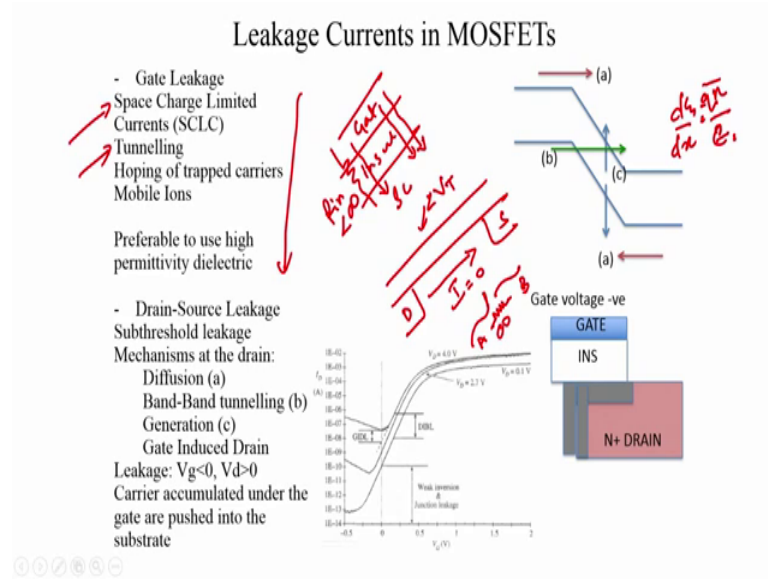


So, what is the option? So, we want to improve field effect, which means if you look at your current voltage relation, where you have $\mu C_{ox} \frac{W}{L} (V_{gs} - V_t)^2$, we would like to improve this parameter here, this C_{ox} . And we are attempting to do that by performing scaling so, we have C_{ox} is ϵ_{ox} / t_{ox} and you scale down t_{ox} and therefore, scale up C_{ox} , but scaling down t_{ox} will result in these leakages and how do we overcome that we say that we do not scale down t_{ox} , all the way we instead pick a dielectric, which is got pick an insulator, which is got a high permittivity and we improve ϵ_{ox} and therefore, improve C_{ox} . While trying to keep t_{ox} same, the

same or while trying to scale down t_{ox} , just a little bit and in this way we can still improve, your field effect and at the same time not given to all these gate leakage mechanisms. .

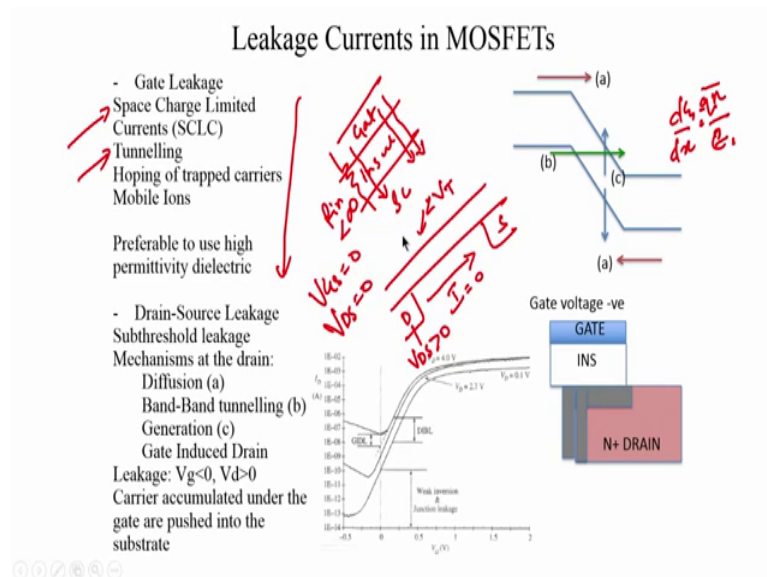
Now, the gate leakage mechanisms effectively reduce the input impedance, they do not keep the input impedance infinite and they make it quite finite and this is got implications, when we design circuits.

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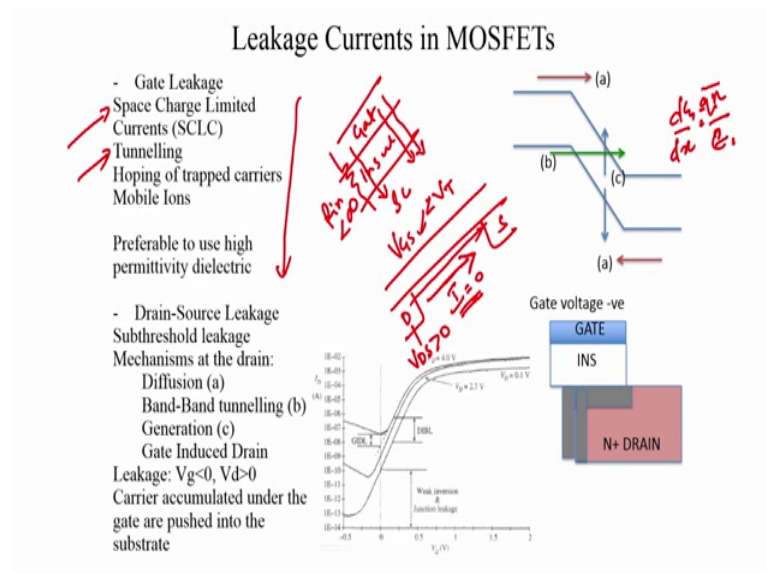


Now what about leakage mechanisms between the drain and source? So, you have the drain and source electrodes in a MOSFET and when the MOSFET is off ok, when the gate voltage is supposed to be less than V_T the idea is you do not have inversion layer formed. So, there is no inversion layer, when the MOSFET is off and theoretically, we would like that the current be 0 or in other words, if you remember the the switch or sending a signal from A to B, when the switch is open, we would like the resistance of this MOSFET of the switch to be ideally infinite ok.

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So, which means that you do have a drain to source voltage, there is a V_{DS} that is greater than 0, if V_{DS} is 0 and a V_{GS} is 0, there should be no current in the MOSFET, that is nothing driving any current mechanism. But a V_{DS} is greater than 0 and V_{GS} is less than V_T or you know if you keep the V_{GS} at a point, where the MOSFET is supposed to be turned off then we do hope that the current is 0, but that is definitely not the case and that is because of many leakage mechanisms through the transistor between drain and source.

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Leakage Currents in MOSFETs

- Gate Leakage
- Space Charge Limited Currents (SCLC)
- Tunnelling
- Hopping of trapped carriers
- Mobile Ions

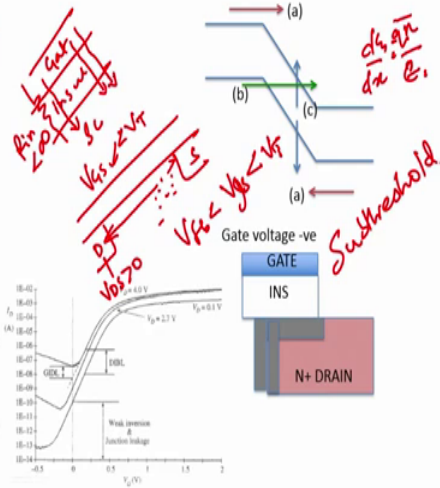
Preferable to use high permittivity dielectric

- Drain-Source Leakage
- Subthreshold leakage

Mechanisms at the drain:

- Diffusion (a)
- Band-Band tunnelling (b)
- Generation (c)
- Gate Induced Drain

Leakage: $V_g < 0, V_d > 0$
Carrier accumulated under the gate are pushed into the substrate



So, what are the different leakage mechanisms? The very first and in fact, the most significant is sub threshold leakage. So, we have already seen that, when V_{GS} lies in this region V_{fb} less than V_{GS} less than V_T , we have a few carriers injected in the near the source side and these carriers diffuse over to the drain side. And we have something called as the sub threshold conduction and we looked at this in some detail and we defined the sub threshold slope etcetera.

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Leakage Currents in MOSFETs

- Gate Leakage
- Space Charge Limited Currents (SCLC)
- Tunnelling
- Hopping of trapped carriers
- Mobile Ions

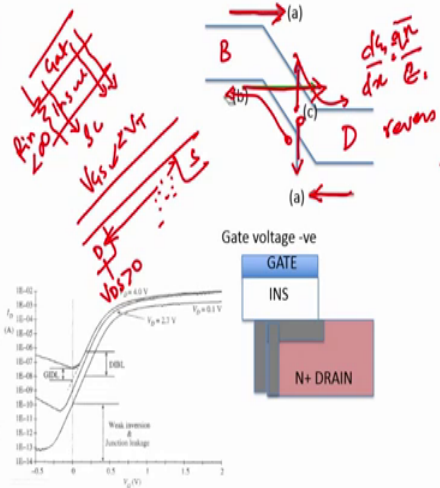
Preferable to use high permittivity dielectric

- Drain-Source Leakage
Subthreshold leakage

Mechanisms at the drain:

- Diffusion (a)
Band-Band tunnelling (b)
Generation (c)
Gate Induced Drain

Leakage: $V_g < 0$, $V_d > 0$
Carrier accumulated under the gate are pushed into the substrate



So, that becomes one of the leakage mechanisms ok, you do have sub threshold currents. Now apart from that, let us take a look at the drain bulk interface ok. So, you have the drain, you have the body of the semiconductor and you have this pn junction, which has got a band bending of this one. So, all leakage mechanisms can this pn junction is reverse biased and near the source side, it is not depending on the body to source potential.

So, these are that is another mechanism and finally, you have something called as gate induced drained leakage ok. Now this is something that, you are probably hearing for the first time ok. So, what is gate induced drain leakage? So, let us take the condition when V_g is less than 0 and V_d is greater than 0 and let us now focus on the gate drain overlap region.

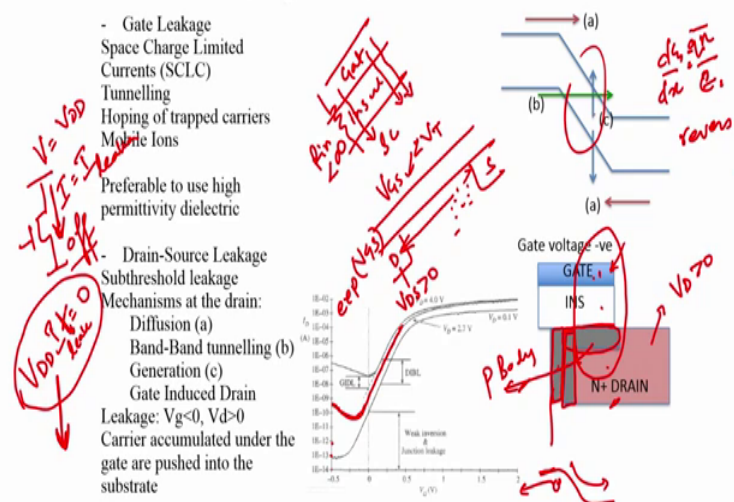
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So firstly, you have the depletion region on the p side and the N side here, because of this pN junction diode between the body and the N doped drain and then you will now also have a depletion region that exists in below this gate. And any carriers generated or any carriers present here, will drift through all these electric fields ok. So, you will have all the electrons ok. So, if you look at this depletion region it looks like that. So, all the electrons will now start running away to the drain side and all the holes will now start running away to the body and this causes an another leakage mechanisms.

So, normally without gate induced drain leakage your currents should be somewhere else and with gate induced drain leakage, your currents are a little higher so, you are basically having leakage. Now why are all these why I am so worried about leakage? So firstly, it completes our MOSFET models right. So, we looked at let us draw the IDS VGS characteristics of a MOSFET. So, we now have a characteristic is actually very well drawn here.

So, you have leakage through the gate at gate and insulator and you also have leakage from source to drain and all these leakage mechanisms are important, because they contribute to power you know the loss of battery life.

Leakage Currents in MOSFETs



So for example, if you are using these MOSFETs and circuits and let us say, you have a circuit and this MOSFET is supposed to be turned off ok. So, we think the MOSFET is turned off and there is supposed to be 0 current or we hope that there is 0 current despite, there being despite the MOSFET being connected to a power supply. And therefore, we expect that the power consumption of the MOSFET, when it is turned off is the VDD into the current through the MOSFET, which is 0.

But because, you now have a leakage current since I is not 0 and you have all these leakage mechanisms; you have static power consumption in a MOSFET circuit. And this power consumption exists even, when all the MOSFETs are turned off and this is going to drain the battery charge because, it is going to continuously drain this much of power from the battery, it is going to drain this much of charge from the this much of energy from the battery at this power. So, therefore, leakage is important and as I said this is all, we will talk about with regards to leakage because this itself could form an entire chapter or you know detailed set of lectures by itself but, we are short of short on time.