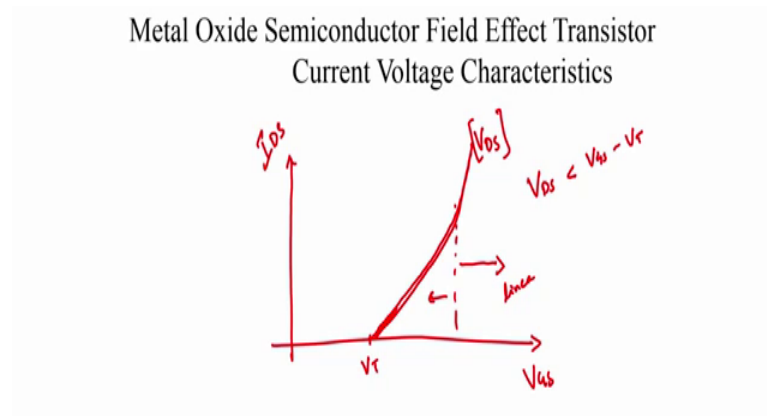


**Semiconductor Devices and Circuits**  
**Prof. Sanjiv Sambandan**  
**Department of Instrumentation and Applied Physics**  
**Indian Institute of Science, Bangalore**

**Lecture - 39**  
**MOSFET: I-V characteristics - Cont..**

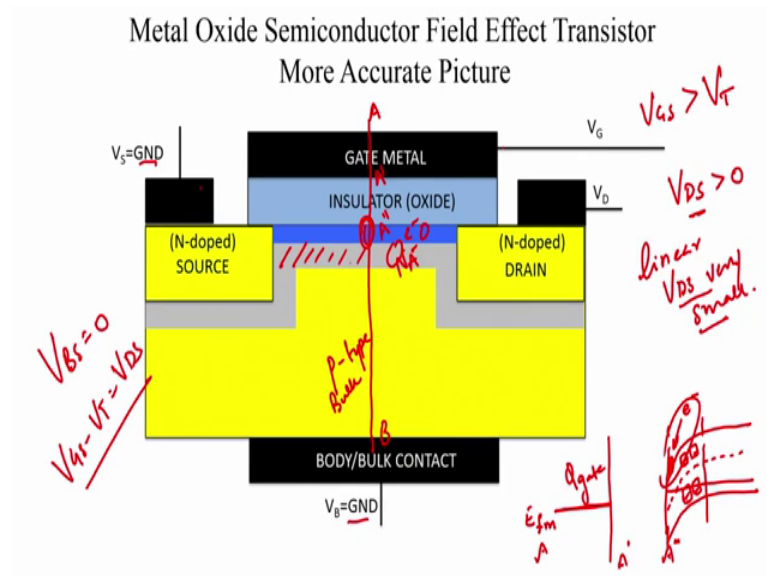
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So, to just to summarize everything we have looked at the MOSFET operates in 2 regions ok. So, we have so far we have only considered 2 regions; which is if I were to plot the  $I_{DS}$  versus  $V_{GS}$ . We have till the threshold voltage we do not know what is going on, but after the threshold voltage depending on the value of the  $V_{DS}$  chosen, the MOSFET (Refer Time: 00:41), linear mode of operation or it can enter saturation mode of operation ok.

So, if I once you once you pick a certain  $V_{DS}$  ok. So, let us say  $V_{DS}$  is now fixed for values of  $V_{DS}$  less than  $V_{GS}$  minus  $V_T$  ok. So, let us say that which implies that in this region ok. So, these this is the region where let us say  $V_{DS}$  got the possibility of being less than  $V_{GS}$  minus  $V_T$ , the MOSFET will be in linear mode of operation, and in this region the MOSFET will be in saturation mode of operation. But so far we have not discussed what happens to the MOSFET below threshold voltage.

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So, while discussing the current voltage characteristics, we used a very simple figure ok. It was just done so that the current voltage characteristic, you could sort of imagine what is going on while deriving the first order model for the current voltage characteristics of the MOSFET.

But here is a more accurate in a picture of the situation. So, you have a gate metal, you have your source have grounded the source, you have the body in this case the body is grounded. So, the body to source voltage is 0, and you have a  $V_D$  a drain voltage which is being applied. So, you have a certain drain to source voltages it is greater than 0.

And you have a gate voltage that is  $V_{GS}$  is greater than the flat band voltage. Now in this case since the channel is already formed we will say it is greater than the threshold voltage. Now when you say when we said when we make this initial approximation that is inner in the case of linear operation, we said that  $V_{DS}$  is very small. It does exist, but it is very, very small ok. And as a consequence of that we found that you do have an inversion layer, but the inversion layer is got in almost the same concentration per unit area throughout the region from source to drain. But what we did not show in the previous picture was also the depletion region.

So, if you remember the most capacitor, you first deplete the; you first deplete the semiconductor and it is only after the semiconductor is depleted that you form the inversion layer. So, you have 2 regions here, which is the inversion and the depletion

layer. And in the previous pictures this is not made very obvious. I am trying to make this quite clear here and if you remember the band bending. So, you have it if I were to take a cross section like this ok.

So, this is through the mass capacitor. So, you have your gate metal. So, let us say we start from point A and you head to point B, and we are drawing we are going to draw the band bending along this cut line. So, at a you have a gate metal which has got a certain work function ok. So, that is the work function of the gate metal, and we have applied positive voltage to this device by this time, since you have a P type body, although it shown in the same colour you have a P type bulk.

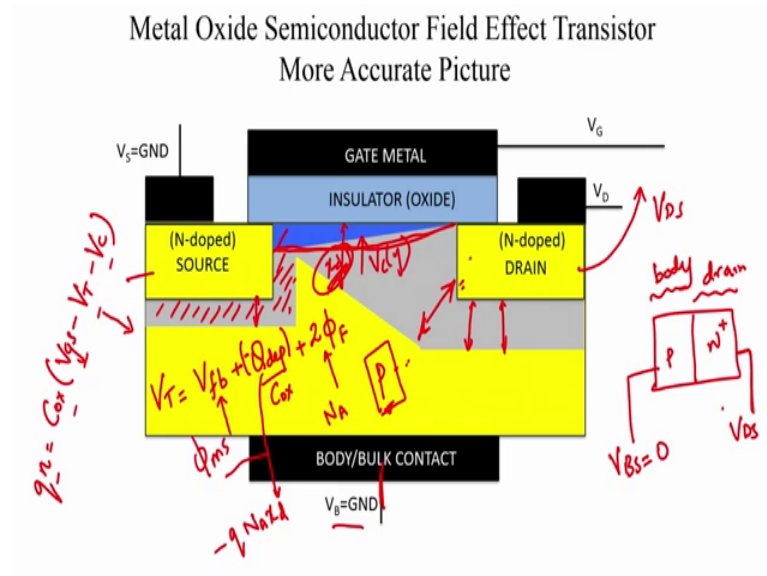
So, you have applied a positive voltage to this which means that you have suppress the, you suppress the fermi level of the metal. And then you have the insulator so, from this point. So, let us say A dash to A double dash let us say. So, this is your A, that is your A dash and from A dash to A double dash we have the region of the insulator ok. So, that is the insulator, and it is only after the insulator that you have your semiconductor.

And right now your semiconductor is in has got significant band bending, has got significant band bending with the fermi level located here which is above  $E_{fm}$ , and you have the intrinsic fermi level bending this way.

And this region here, the channel region is essentially the electrons that have accumulated here. So, that is the channel region; which is shown in blue in the figure, and this gray shaded region is the depletion region. So, it is basically all the acceptor ions that were all exposed and are compensating for the charge applied on the gate metal along with the free electrons.

So, you have free electrons and the depletion layer exposed ions compensating for the charge. So, this is the picture of what is their along this cut line. Now if we aware to increase the  $V_{DS}$  so, we do not have a  $V_{DS}$  that is very small; that means, you cannot ignore the  $V_{DS}$  anymore, but you increase the  $V_{DS}$ .

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So, we increase the  $V_{DS}$  significantly; as  $V_{DS}$  goes up significantly, you see this P N junction here, this P N junction becomes more reverse biased. Because your bulk this P can be said to be at ground. So, you have a P N junction diode where that is the N side that is the P side, that is the N plus that is contributing here drain region, and that is the body or the bulk of the semiconductor. When my  $V_{DS}$  goes very large, so, this is my  $V_{DS}$ , and that is my  $V_{BS}$  which is now connected to 0.

So, my  $V_{BS}$  is 0 because my body is at ground. So, if this gate if the drain voltage goes to be goes up, you increases the reverse bias on the P N junction and therefore, this depletion layer around the drain region should increase significantly, ok. I probably exaggerated it here, but you know you want have such nice sharp lines will have a region that is much more gentle and gradual like that. An a near the source sides since my since the P N junction has got 0 voltage across it, it will have the same depletion layer of all practical purposes it will have the same depletion with as one would expect in equilibrium. With the exception that you have a active gate field right now.

So, you will find that the depletion layer in this region is going to be much a smaller as compared to the depletion layer thickness near the drain side. And also we also solve the channel potential you know. So, the channel potential varies as you go from drain to source, and this channel potential also affects the also affects the free carrier concentration; which is the inversion layer charge. And therefore, one would find that the

inversion layer charge actually decreases as one heads towards the drain site, and this leads to the pinch off and therefore, your saturation mode characteristics.

So, in our model so far we never you know used we never took into count this variation in the depletion layer thickness. And why is that important? So, if you recollect our models ok, we always said that  $q_n$  which is the number of electrons or let us say the number of number of electrons at the interface per unit volume was equal to your  $C_{ox}$  into  $V_{GS}$  minus  $V_T$  minus the channel potential.

And we made this we used this picture to accomplish that equation right because here the depletion layer is not varying too much because our  $V_{DS}$  is very small. But then while talking about saturation mode operation, we just continued using the same equation and substituted  $V_{GS}$  minus  $V_T$  for  $V_{DS}$  after giving some qualitative analysis ok. So, can we quantify these bits a little better? So, that is that is that is the point of the next few slides.

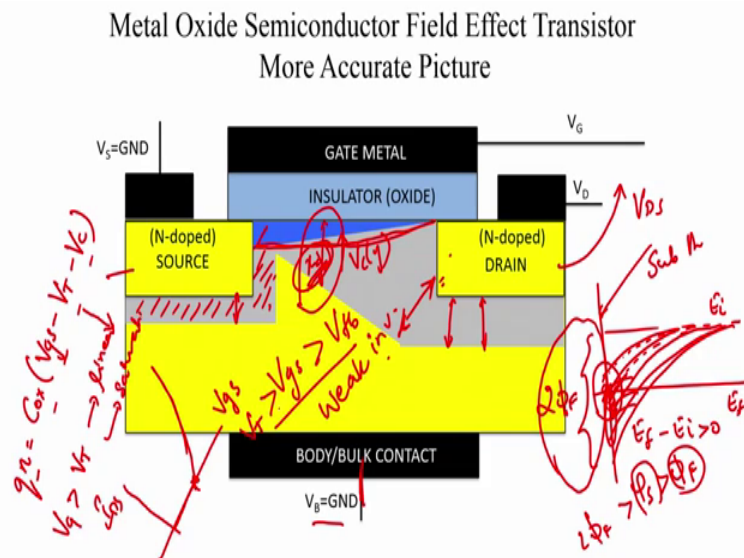
So, we said that  $q_n$  is equal to  $C_{ox}$  into  $V_{GS}$  minus  $V_T$  minus  $V_c$  ok, but the problem in assuming that  $x_d$  is constant everywhere is related to the threshold voltage ok. Why is it related to the threshold voltage? What is the threshold voltage? Threshold voltage has got 3 milestones ok, the threshold voltage for accomplishing the threshold voltage you need to first you know get to flat band condition, you need to put enough charge in the gate so that you are at flat band, then you need to deplete the semiconductor ok.

So, in our case the depletion charge is negative. So, I will just use a negative sign, and after that we need to increase a surface potential till the surface potential matches 2 times  $\phi_f$ ; where  $\phi_f$  depends upon the doping concentration of the P type bulk. So,  $v_{fb}$  so far is only related to the metal semiconductor work function difference. That really does not mat it really does not care as to whether the depletion with this increasing as we approach the drain side or not.

Similarly,  $\phi_f$  only depends upon the dopant concentration any right. That too is not dependent on the thickness of the depletion region. But  $q_{depletion}$  obviously, should depend upon the thickness of the depletion region. And what does  $q_{depletion}$ ? It is a depletion charge per unit area and that is going to be minus  $q N_A$  into  $x_d$ .

So, in all our assumptions so far we have ignored this fact. And this is something that we will address in these lectures. Now that is one fine tuning to the model. The second the second problem the second deficit in the models that we have developed is as to what happens when  $V_{GS}$  is less than  $V_T$  ok.

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We said ok, when  $V_{GS}$  is greater than  $V_T$  you have the linear mode of operation, and then you have the pinch off and therefore, the saturation mode of operation.

And so far for  $V_{GS}$  below  $V_T$  the current was said to be 0 ok, and it was it was here somewhere that the characteristic started off. So, if you plot  $V_{GS}$  versus  $I_{DS}$ , the current is 0 till a certain point and then the characteristics start off beyond that point ok. Now that is rarely the case, you do not have electrons sitting there as a traffic stop and waiting for  $V_{GS}$  tube become greater than  $V_T$ . The physics is much more smoother and it is much more natural much more gradual I should say.

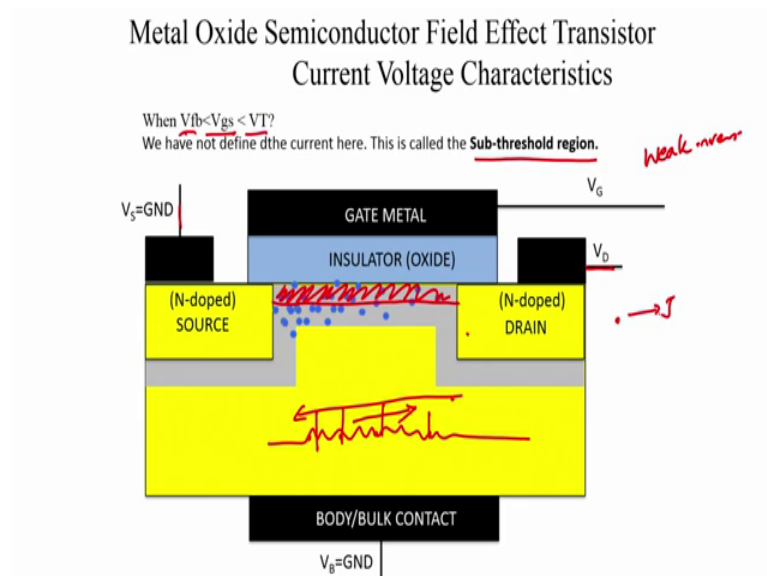
And when  $V_{GS}$  is greater than the flat band voltage, but less than the threshold voltage, you do have something called as weak inversion. And what does weak inversion? Weak inversion means that, the band bending at the semi conductor insulator interface looks like this. You have you have let us say this is the fermi level of the semiconductor. And the intrinsic fermi level does start bending a little, and that is your depletion region.

And as it bends a little more your  $E_i$  minus  $E_f$ , or  $E_f$  minus  $E_i$  near the interface becomes greater than 0; which means at the  $E_i$  has gone below  $E_f$ . And as keep increasing the gate voltage continues going below  $E_f$  till the point where it the bending is so much that  $E_i$  minus  $E_f$  which is becomes equal to  $\phi_f$  or the surface potential becomes equal to  $2\phi_f$ , which is when we say that we have hit threshold; but all these regions wherein  $\phi_s$  is greater than  $\phi_f$ , but less than  $2\phi_f$  ok.

All these regions are said to be weak inversion; which means that electrons are encouraged to appear at the surface ok, starting from you know well before even when  $\phi_s$  is less than  $\phi_f$ , electrons do start appearing at the surface ok. But this is to the concentration is still not large enough for us to say that the device is completely turned on.

So, that is the region which we have completely blanked out on in our model. So, we are also going to correct for that aspect. That region is something called as a sub threshold region. So, we will address 2 topics now. One is the correction to what happens at  $V_{GS}$  less than  $V_T$ , and the second is taking into account this variation in  $x_d$  to correct for the threshold voltage.

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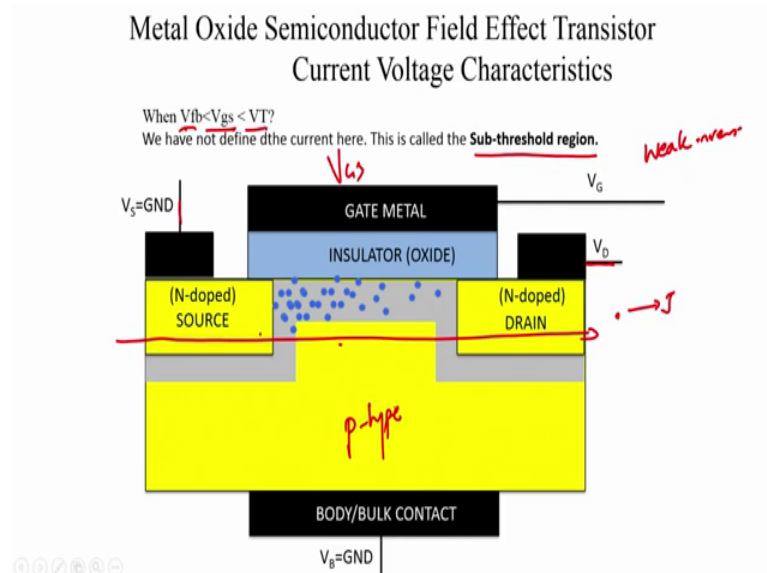


So, when the  $V_{GS}$  is less than  $V_T$ , but greater than the flat band voltage we are in weak inversion ok, or it is called as a sub threshold region of operation. Now as long as you have a  $V_{DS}$  you do have a current ok. But we need to be careful about how we model

this current. Now in the case of inversion, we had a complete electron channel connecting the source to the drain, right. It was like one long resistor that was connecting source to the drain. And therefore, the drain to source voltage was sort of divided it was spread across this resistor.

So, as you moved from the drain to source, every electron felt the field of the drain voltage field of  $V_{DS}$ . And therefore, we could model the current as a drift current ok. But in the case of weak inversion what is expected is you have a certain  $V_{GS}$  and if you look at this P N junction ok.

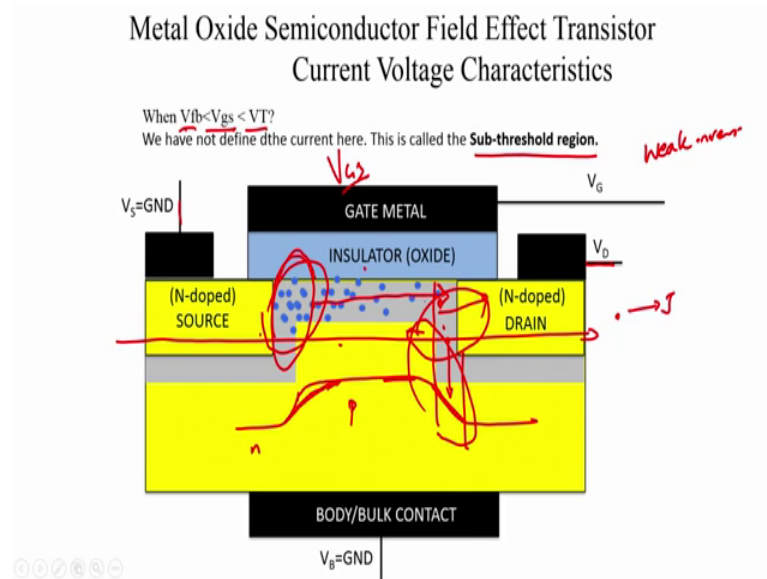
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So, these are if you let us let us draw a cut line this way ok. So, what do we have? We have an N type you have a P type those shown in the same colour. So, this is a mistake, yeah, it should have been shown with a different colour. So, you have your N doped source and N doped drain.



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And you have a P N junction that looks like that right.

So, that is the P region that is the N region and this is the, you know depletion with there that is the depletion with there and this is a P N junction.

So, the moment we apply a  $V_{GS}$  what happens is we trying to suppress this barrier. And therefore, the electrons are encouraged try an occupy the region between the gate at the insulate and semiconductor from the source. Now while performing the analysis under full or strong inversion, we assume that many electrons had already come in, and they are all they have already formed a channel. But in the weak inversion, you can say that the  $V_{GS}$  is so small that we cannot make that assumption anymore.

So, you do have some suppression near the source side. You have more suppression of the barrier near the source side and less or near that drain side so, let us say that. And therefore, you do have a lot of carriers injected near the source ok. But they are still not large enough for them to form a continuous channel which means that if you look at this depletion region, this P N junction diode, the field here you did this P N junction diode is completely dropped across this depletion region ok. And therefore, these electrons really cannot feel the drain source field till they have reached this depletion boundary ok.

So, the electrons need to migrate from here to here into this depletion boundary before they actually start drifting towards the drain. So, therefore, what do you think would be the mechanism by which the electrons injected here could move to the other side?

(Refer Slide Time: 18:10)

**Metal Oxide Semiconductor Field Effect Transistor  
Current Voltage Characteristics**

Carrier count varies as  $\exp(q\phi_s/kT)$ .  
 Carriers from the source do not 'feel' the VDS field till they reach the PN depletion edge.

Current controlled by diffusion.

$$I_{ds} = qAD_n \frac{dn}{dy} \approx qD_n(W) \frac{n(0) - n(L)}{L}$$

The answer has to be diffusion right. So, you have, you have electrons being injected near the source and not so many being injected near the drain ok. So, you have you have a concentration gradient in the electrons.

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**Metal Oxide Semiconductor Field Effect Transistor  
Current Voltage Characteristics**

When  $V_{fb} < V_{gs} < V_T$ ?  
 We have not define dthe current here. This is called the **Sub-threshold region**.

*weak inversion*

*Diffusion*

*Subth → Diffusion*

And these electrons do not feel the drain to source field till they reach this depletion edge. And therefore, these electrons are now the, their movement of their flux is governed completely by the concentration gradient therefore, the mechanism of transport is diffusion.

So, in sub threshold region, we cannot use a drift equation to model electrons, but rather we must use the diffuse diffusion component ok. So, this is how we go about. It just a very quick estimate is as follows right. So, the carrier count will vary exponentially with the surface potential ok. And as we as we move from as we move from the source to the drain, as we move from the source to the drain, we find that the carrier count increases ok. So, I am sorry it decreases.

So, let us say  $N$  is a number of electrons per unit volume near the source is  $N_0$  ok. So, we have been defined we have defined the source and the drain like this. And we say that this is  $y$  equal to 0, and that is  $y$  equal to  $L$ . And at  $y$  equal to 0, we have defining the carrier concentrations  $N_0$ , and at  $y$  equal to  $L$  we define the carrier concentration as  $N$  equal to  $N$  of  $L$ .

So, the diffusion current is  $q$  times whatever the area of cross section is into  $dn$  which is the diffusion coefficient. So, which is approximately  $kT \mu$  by  $q$ , it is a diffusion coefficient and the concentration the derivative of  $N$  with respect to  $y$ ; which you know brings out the concentration gradient. So, this is our diffusion current. And what is  $A$  here,  $A$  is whatever you know thickness you want to associate. So, the last time while performing the analysis on inversion, we said that let us treat all the electrons like a particle and this sheet of electron charge had a thickness of  $h$ .

Now we never defined  $h$ , I can it because  $h$  cancelled off. But a here let us retain it and we will try to get an approximate estimate of what  $h$  is. So, this will constitute the area of cross section, which is the channel width into this thickness edge ok. And instead of  $dn$  by  $dy$  instead of me getting estimate a perfect estimate which relates to the channel potential of what  $N$  is with respect to  $y$ , what we will do is will make a big approximation here, and say that  $dn$  by  $d$   $dn$  by  $dy$  is simply  $N$  of 0 minus  $N$  of  $L$  divided by  $L$ .

So, which means is the carrier concentration near the source minus the carrier concentration near the drain divided by  $L$  ok. Big estimate  $I$  means a big approximation,

but a never the less it is very useful to get our quickens. So, we say that this is our dn by dy ok. And therefore, we will now go ahead and compute what dn by dy.

(Refer Slide Time: 22:06)

Metal Oxide Semiconductor Field Effect Transistor  
Current Voltage Characteristics

$n(0) = n_{p0} \exp(q\phi_s / kT)$   
 $n(L) = n_{p0} \exp(q(\phi_s - V_{ds}) / kT)$

$h \sim \text{Debye Length} \sim \frac{kT}{q^2 \epsilon_s} = \frac{kT}{q \sqrt{2qN_A \phi_s / \epsilon_s}}$

$I_{ds} \cong qD_n W \frac{kT}{q \sqrt{2qN_A \phi_s / \epsilon_s}} \frac{n_{p0} \exp(q\phi_s / kT)(1 - \exp(-qV_{ds} / kT))}{L}$   
 $\cong \mu \frac{n_i^2}{N_A} \left( \frac{kT}{q} \right)^2 \frac{W}{L} \sqrt{\frac{q\epsilon_s}{2N_A \phi_s}} \exp(q\phi_s / kT)(1 - \exp(-qV_{ds} / kT))$

*Handwritten notes:*  
 $n_{p0} e^{q\phi_s / kT}$   
 $n(L) = n_{p0} e^{q(\phi_s - V_{ds}) / kT}$

So, near the source side this is the expected carrier concentration. You have  $n_{p0}$ ; which is the number of electrons in the P type bulk at equilibrium into  $e$  to the power  $q\phi_s$  by  $kT$ , which is like the forward bias voltage applied to your diode, the source and bulk diode. And near the drain side or at any other region, you would have  $N$  of say  $y$  equal to  $n_{p0} e$  to the power  $q\phi_s$  minus  $V_c$  of  $kt$  ok. There is no channel here, but it is the potential gradient as you go from source to drain, and near the drain side this would simply be  $V_{DS}$  ok.

So, at  $N$  equal to  $L$  at  $y$  equal to  $L$   $N$  of  $L$  is simply  $n_{p0}$  into exponential of  $q\phi_s$  minus  $V_{DS}$  by  $kt$  ok. And what is this  $h$  the channel thickness right. So, a good estimate for  $h$  ok; so, you should remember the electrons form a very very thin channels, basically just a sheet of charge ok. It is not it is not very thick. In fact, if you although this is all we are not doing this as part of this course, if you look at the profile of the conduction band here. You have all the electrons sitting here, and these electrons all have their own wave function. And essentially, these electrons are sitting inside a triangular box of some set of some sorts right.

So, it is if I just approximate everything like this we say, if I draw my conduction band diagram like this. And if I say that this is the insulator, you have electrons that have a

certain wave function that are sitting inside this box. And what is the potential profile, the potential profile on the left side you could say is a finite potential barrier because of the insulator. And on the right side is a triangular potential barrier, and the electrons also experienced significant electrostatic interaction between each other.

And therefore, that also gets involved into the potential term. So, it is a it is a complex situation right here. But it is you could expect the electron wave function to be to have a non you could expect the electron wave function to penetrate these barriers. And therefore, the electrons have a non-0 probability of occupying the regions in the insulator etcetera, etcetera. But what we are doing here is we just want to understand, what this thickness is ok, we want to understand get an estimate for the thickness because we want an approximate answer to what our sub threshold current is.

So, what is an estimate of this thickness, the estimate of this thickness is the estimate of the penetration depth of the electric field right. So, you have you have your band bending in the semiconductor because of the applied gate.

(Refer Slide Time: 25:34)

Metal Oxide Semiconductor Field Effect Transistor  
Current Voltage Characteristics

$n(0) = n_{p0} \exp(q\phi_s / kT)$   
 $n(L) = n_{p0} \exp(q(\phi_s - V_{ds}) / kT)$

Debye Length  $\sim \frac{kT}{q\epsilon_s} = \frac{kT}{q\sqrt{2qN_A\phi_s / \epsilon_s}}$

$I_{ds} \cong qD_n W \frac{kT}{q\sqrt{2qN_A\phi_s / \epsilon_s}} \frac{n_{p0} \exp(q\phi_s / kT)(1 - \exp(-qV_{ds} / kT))}{L}$   
 $\cong \mu \frac{n_i^2}{N_A} \left(\frac{kT}{q}\right)^2 \frac{W}{L} \sqrt{\frac{q\epsilon_s}{2N_A\phi_s}} \exp(q\phi_s / kT)(1 - \exp(-qV_{ds} / kT))$

Handwritten notes:  $n_{p0} e^{q\phi_s / kT}$ ,  $n(L) = n_{p0} e^{q(\phi_s - V_{ds}) / kT}$

In case you have the insulator there and you have due to the applied gate voltage you have band bending in the semiconductor. And beyond a certain point  $x_d$  our bands become flat, but once the electrons appear at the interface what is Poisson's equation?

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**Metal Oxide Semiconductor Field Effect Transistor  
Current Voltage Characteristics**

$n(0) = n_{p0} \exp(q\phi_s / kT)$   
 $n(L) = n_{p0} \exp(q(\phi_s - V_{ds}) / kT)$

$\sim$  Debye Length  $\sim \frac{kT}{q\sqrt{2qN_A\phi_s/\epsilon_s}}$

$I_{ds} \cong qD_n W \frac{kT}{q\sqrt{2qN_A\phi_s/\epsilon_s}} \frac{n_{p0} \exp(q\phi_s / kT)(1 - \exp(-qV_{ds} / kT))}{L}$

$\cong \mu \frac{n_i^2}{N_A} \left(\frac{kT}{q}\right)^2 \frac{W}{L} \sqrt{\frac{q\epsilon_s}{2N_A\phi_s}} \exp(q\phi_s / kT)(1 - \exp(-qV_{ds} / kT))$

Poisson's equation now becomes  $d^2\phi/dx^2$  is equal to the electron charge right. So, it is the electron charge by epsilon plus the acceptor ion.

So, you also have the acceptor ion charge. So, this is the Poisson's equation that we need to solve and this is a function of the potential. So, we have already looked at this case when we looked at the ohmic metal semiconductor contacts ok. If you remember the ohmic metal semiconductor junction; of course, there probably we do not have we used N type semiconductor in any analysis, but nevertheless the idea is the same. And you do have an electron charge which is dependent on the potential. And therefore, you need to use those techniques to solve Poisson's equation ok.

So, it is a similar case here, and a good estimate of the penetration depth of the electric field is something called as a Debye length, right. It is it provides a rough estimate as to you know how to what extent the band bending occurs.

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Metal Oxide Semiconductor Field Effect Transistor  
Current Voltage Characteristics

$$n(0) = n_{p0} \exp(q\phi_s / kT)$$

$$n(L) = n_{p0} \exp(q(\phi_s - V_{ds}) / kT)$$

$$h \sim \text{Debye Length} \sim \frac{kT}{q\sqrt{2qN_A\phi_s/\epsilon_s}}$$

$$I_{ds} \cong qD_n W \frac{kT}{q\sqrt{2qN_A\phi_s/\epsilon_s}} \frac{n_{p0} \exp(q\phi_s / kT) (1 - \exp(-qV_{ds} / kT))}{L}$$

$$\cong \mu \frac{n_i^2}{N_A} \left( \frac{kT}{q} \right)^2 \frac{W}{L} \sqrt{\frac{q\epsilon_s}{2N_A\phi_s}} \exp(q\phi_s / kT) (1 - \exp(-qV_{ds} / kT))$$

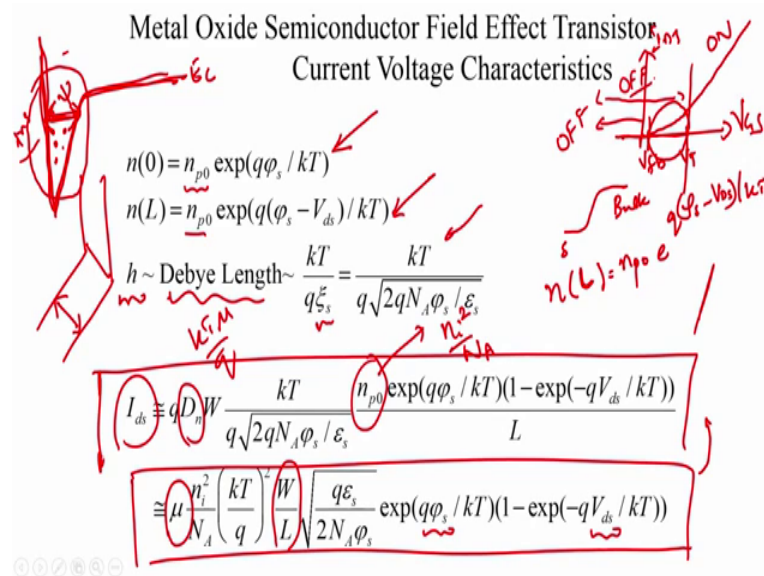
And we define this  $h$  or this thickness of the electron sheet still not yet a sheet, but that thickness of this cross section of conduction to be  $h$  which is approximately the Debye length, and the Debye length is approximately the thermal voltage divided by the electric field at the semiconductor in select a interface. But the electric field in the semiconductor at the semi conductor insulator interface. So, this is our definition the Debye length and that turns out to be this. So, we assign 3 parameters here right.

So, this is our equation this is our equation for the current. We know what the diffusion coefficient because it is  $kT \mu N$  by  $q$ , we will not define that any further  $q$  is a constant,  $w$  is a channel width,  $h$  was undefined. So, we have defined that  $N$  of  $0$  was undefined. So, we have defined that  $N$  of  $L$  is undefined. So, we have defined that and  $L$  is the channel length so, that is defined.

So now we have all the parameters needed to identified the current in the sub threshold region. And the current is simply the combination of all these and it turns out to be this equation here. Very rough approximation, many things approximated here right. Now if you take  $n_{p0}$  and say it is nothing but  $n_i^2$  by  $N_A$  ok, and if you say that  $n_{p0} = kT \mu$  by  $q$ . You can rewrite this expression as this particular in this particular form. Now what is important to note is that, the drain to source current does exist below threshold, and the drain to source current is dependent on the aspect ratio is proportional to the mobility ok.

And it is exponentially dependent on the surface potential which in turn is dependent on the gate voltage. And it is exponentially dependent on the drain to source voltage. So, it is a very characteristic nature of the current in the sub threshold region. You have an exponential dependence on the gate voltage ok. Now the sub threshold current is basically the current that is the sub threshold region right. So, if you if you were to draw the  $I_{DS}$  versus  $V_{GS}$  characteristics.

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So, let me now exaggerate this ok. So, let us say below flat band the currents all ignored, and between flat band to sub threshold, we will now no longer say that the current is 0, because we now have an equation here.

We know the current is exponentially increasing ok, it increases and then beyond  $V_T$  the current enters the square law dependence on the voltages, ok. So, that is the that is the current voltage characteristics of the MOSFET. Now in this region ok, this region is quite significant, because beyond this region beyond  $V_T$  the MOSFET is said to be on, and below  $V_{fb}$  the MOSFET is said to be off ok. Or in fact, extending all the way till  $V_T$  the MOSFET is technically off it does not conduct as much current as the on state.

Therefore, this region between  $V_{fb}$  and  $V_T$  is the intermediate region from the off to the on state. Therefore, the speed at which or you know the current density in this region strongly determines the speed at which the MOSFET turns from off to on and on to off.



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Metal Oxide Semiconductor Field Effect Transistor  
Current Voltage Characteristics

$$n(0) = n_{p0} \exp(q\phi_s / kT)$$

$$n(L) = n_{p0} \exp(q(\phi_s - V_{ds}) / kT)$$

$$h \sim \text{Debye Length} \sim \frac{kT}{q \sqrt{2qN_A \phi_s / \epsilon_s}}$$

$$I_{ds} = q D_n W \frac{kT}{q \sqrt{2qN_A \phi_s / \epsilon_s}} \frac{n_{p0} \exp(q\phi_s / kT) (1 - \exp(-qV_{ds} / kT))}{L}$$

$$\cong \mu \frac{n_i^2}{N_A} \left( \frac{kT}{q} \right) \left( \frac{W}{L} \right) \left[ \frac{q \epsilon_s}{2 N_A \phi_s} \exp(q\phi_s / kT) (1 - \exp(-qV_{ds} / kT)) \right]$$

And it is a very key parameter you know the slopes or the time constants or your  $dI_D$  by  $dV_g$  if you like ; is a very important parameter to estimate how quickly the MOSFET turns on.

So, we need to give a better definition for this region, particularly the slopes associated to this region ok. And what is done, but since the current is only dependent on the surface, the exponential of the surface potential we need to do some work to define this correctly.