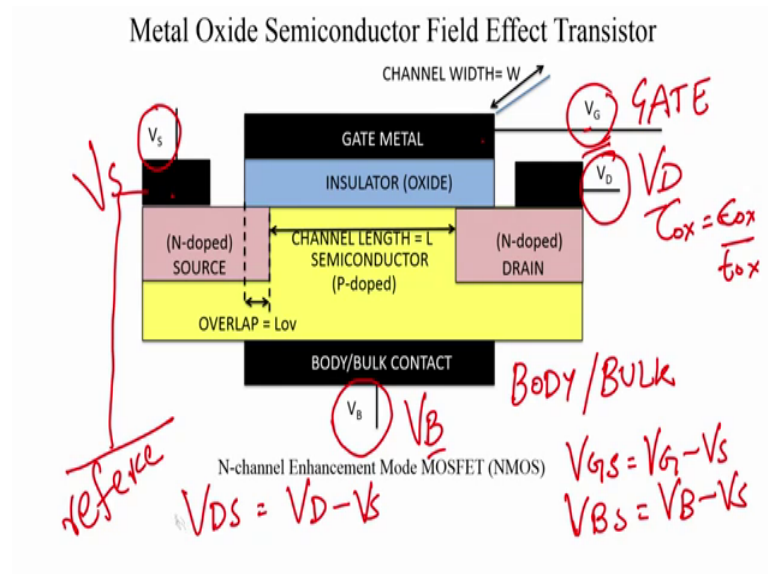


Semiconductor Devices and Circuits
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Lecture -36
MOSFET: Introduction

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The enhancement mode MOSFET looks like this. So, you are already familiar with this bit which is the MOS capacitor ok. So, if we look at this cross section if you forget everything else that is present beyond this, we forget all that what you have here is the gate, insulator, semiconductor and the back contact and this was your MOS capacitor. But, what the MOSFET does is it makes use of this device, but it adds some more terminals ok.

So, now you have the gate which is provided a gate voltage V_G . And then you have the back contact which is got a voltage V_B and this back contact is now called in the context of the MOSFET it is now called the body or the bulk contact because, it connects to the body of the semiconductor ok. So, it is the body or the bulk contact and then that is your familiar gate contact that is connecting to the gate metal. You have your insulator and the insulator could be an oxide and it is got some thickness t_{ox} and it is got the permittivity ϵ_{ox} and therefore, the insulator capacitance per unit area is ϵ_{ox} by t_{ox} .

And then you have your semiconductor and let us stay with the example of a P doped semiconductor. Now, in order to create your A and B that is the two terminals through which the signal has to transfer, the signal has to transfer from A to B and in order to have those two terminals you have your source and you have a drain ok.

So, these are two additional terminals in your, that are added to your MOS capacitor to create your MOSFET. Now what does the source in drain have, now the first thing is that the source and drain let us look at the way it is created ok. So, it is not just metal placed on the semiconductor and we will see why it should not be. Essentially what we need is a electrical contact and the current will actually transfer from source to drain or the carriers will move from the source to drain or vice versa depending on the type of carriers and depending on the potential.

And the first thing about the source and drain is normally they are absolutely symmetrical. There is nothing to say as to there is nothing in the design or in the fabrication to say that one of them is the source and the other is the drain. The source and drain are purely defined based on the voltages that you apply, the bias voltages that you apply ok. So, this is this structure is absolutely symmetry.

So, give it a MOSFET like this it is equally possible to you treat this terminal as your source and that terminal as your drain it does not matter, but it all depends on the voltages that you apply. So, we will just label that as your source and it is given a source voltage V_S and this is the drain and this is given a drain voltage V_D . Now all these potentials that is V_B V_D the gate are all taken with respect to the source. So, this is the reference potential for your MOSFET structure. So, what is important in the MOSFET is the gate to source voltage ok.

So, it is not just V_G with respect to some arbitrary ground or some universal ground that really you need to really extract out what is the potential seen or what are the fields seen within the device and therefore, all the voltages are measured with respect to the source. So, you have the gate to source voltage which is basically V_G minus V_S , you have the body to source voltage which is basically your V_B minus V_S and you have the drain to source voltage which is V_D minus V_S ok, but for now let us just say that the source is at V_S and the gate is at V_G the body is at V_B and that drain is at V_D . So, how are the source and drain terminals created.

So, essentially you have created a diode here, you create a diode here, and you create a diode here and then you have your metal contact ok. Now what is the purpose of this source and drain? So, the idea of the MOSFET is to operate an inversion. So, the MOSFET if you think of the MOSFET as an on and off device ok; so, when it is off let us say the flat band voltage is 0. So, we are familiar with the MOS capacitor and the flat band voltage. So, let us say the flat band voltage is 0 ok.

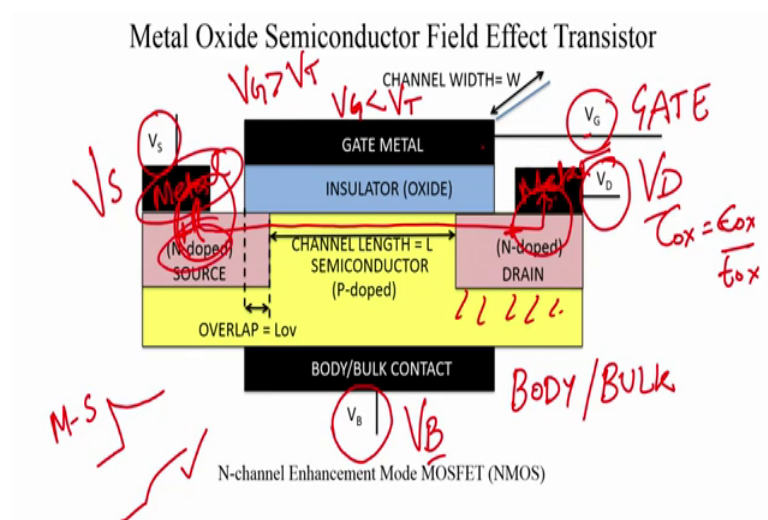
The diagram illustrates the structure of an N-channel Enhancement Mode MOSFET (NMOS). The layers from top to bottom are: GATE METAL, INSULATOR (OXIDE), (N-doped) SOURCE, (P-doped) SEMICONDUCTOR, (N-doped) DRAIN, and BODY/BULK CONTACT. The channel width is labeled as W and the channel length as L . The overlap between the gate and the source/drain is labeled as $OVERLAP = Lov$. Handwritten red annotations include: $V_G > V_T$ and $V_G < V_T$ near the gate; V_S and V_D near the source and drain; V_G and V_D near the gate and drain; V_B and V_B near the body/bulk contact; $C_{ox} = \frac{\epsilon_{ox}}{t_{ox}}$ near the oxide layer; and V_S and V_D near the source and drain. The text "CHANNEL WIDTH = W" is written above the gate metal. The text "CHANNEL LENGTH = L" is written inside the semiconductor layer. The text "OVERLAP = Lov" is written below the source/drain region. The text "BODY/BULK CONTACT" is written below the semiconductor layer. The text "GATE METAL" is written inside the gate metal layer. The text "INSULATOR (OXIDE)" is written inside the oxide layer. The text "(N-doped) SOURCE" is written inside the source region. The text "(P-doped) SEMICONDUCTOR" is written inside the semiconductor layer. The text "(N-doped) DRAIN" is written inside the drain region.

And theoretically when my VG is at the flat band voltage or generally we will speaking when VG is less than VT there should be no electrons here and therefore, you are in depletion mode operation or your in you are switched off ok. So, there is nothing there is no way carriers from the source can actually move to that drain because this region is completely depleted. But, when VG becomes greater than VT the MOSFET enters the inversion region which means that the, which means that minority carriers start appearing at the interface.

So, we have already looked at this in the discussion on the MOS capacitor. And the idea is that if you have an N doped region not these minority carriers which are electrons, not only appear from the thermally generated carriers from the P doped bulk, but are also drawn in from the source side; provided that there is a drain the source voltage. So, the source also contributes to these.

So, the essential idea so, this is the first role of the N plus doped source and drain which is to act as a carrier source or the minority carrier source in their device. And, essentially create this is N plus electron N plus pathway or this conduit because everything around this is doped is all depleted sorry it is a PN junction device therefore, these all depleted you have a depletion region throughout here ok. So, all this is depleted, but when inversion happens you have this entire region being depleted and you have an electrically conductive path from this N doped region through these electrons and through that N doped region into the drain. So, that is the way the MOSFET intends to operate ok. So, that is one point of having a N plus region.

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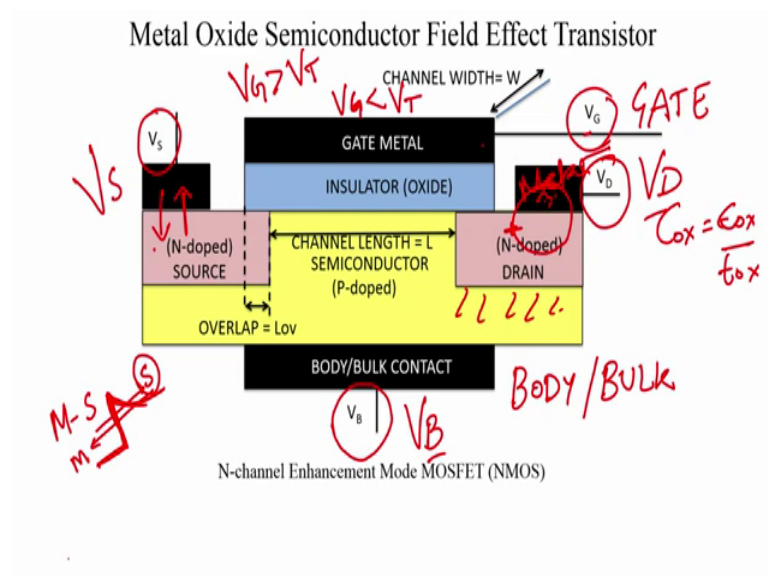


The other key purpose of these N plus dope, wide are we insisting on a heavily doped drain and source contact ok. So, this is your drain source contact, the idea is we want to inject the current right from this metal and into that metal which means that we want this metal semiconductor junction to be ohmic ok. So, if you remember your metal semiconductor junctions we could had two kinds of junctions; one is where we had a

short key barrier and the other is where we had a ohmic contact ok. So, which contact would you like if you want to have current flowing through both ways, we would ideally I like an ohmic contact.

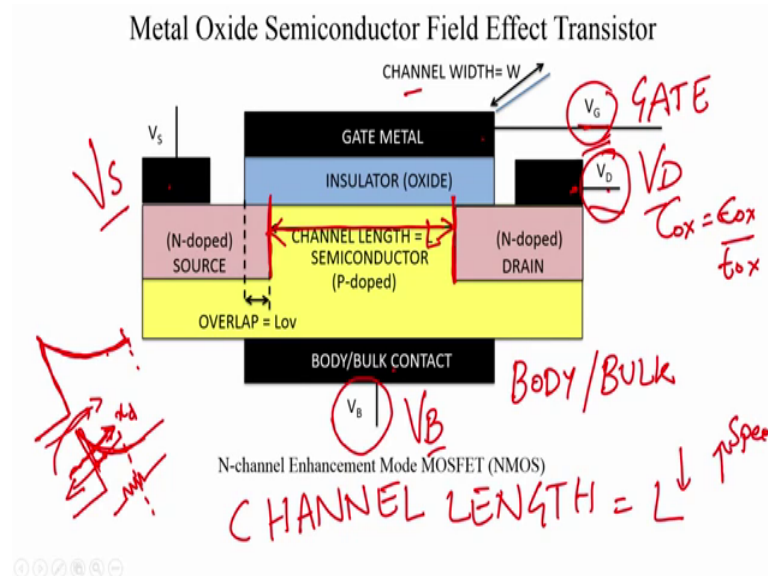
So, by simply choosing a metal and by doping the semiconductor correctly we should have an ohmic contact, but unfortunately that is not it is not that trivial. And, it is not that trivial because of a lot of issues particularly because of the Fermi level gets pinned, because of interfacial states etcetera etcetera which means there are trap states here; electrons get trapped and electrons cannot move about very easily. So, it is very likely that we will end up creating a short key barrier or a short key contact and this is not what you need. So, how given the fact that you can do nothing other than create a short key contact.

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So, let us say we have this problem we can only create a short key contact and we want to get electrons in and out of this from the metal to the end to the doped semiconductor which is the source we want to get electrons in and out of this; how do we go about doing that ok. So, let us look at the band bending of a metal semiconductor junction short key junction.

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So, let us say that is your band bending ok. Now what happens if I increase my dope and concentration in the semiconductor? If you increase the dope and concentration in the semiconductor the band bending will become a lot sharper, will be the bending will be much more narrower right. All the bending will finish quite early the x_d becomes small, the bending becomes the bending is very the electric fields are quite large etcetera etcetera.

On the other hand if you reduce the doped and concentration the bending is more relaxed the x_t is much larger the electric fields of weaker and so on. But, the advantage of having a bending that is very sharp is that if you remember the different mechanisms of charge transport through a metal semiconductor junction we had thermionic emission, we had diffusion, but we also had tunneling through the barrier through this triangular barrier we had this WKB approximation etcetera etcetera. So, the point of having this heavily N plus doped region is to create a sharp triangular barrier through which electrons can easily tunnel in and out ok.

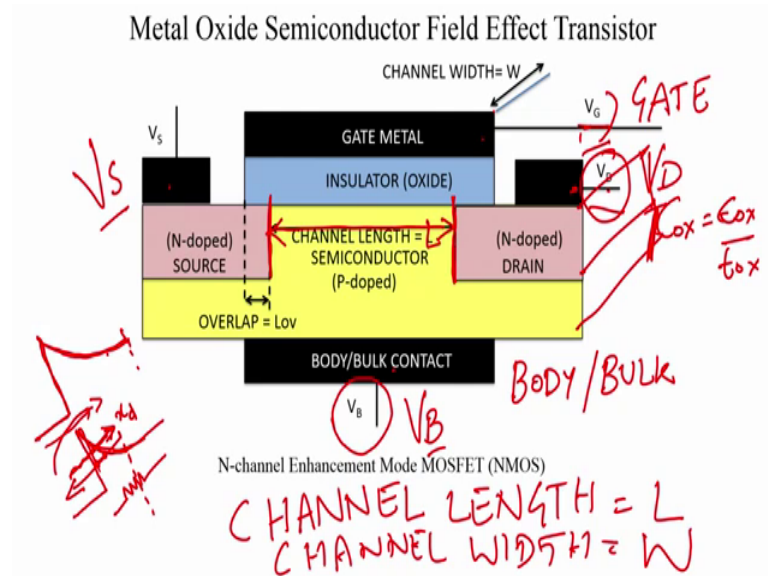
And therefore, give you a very low resistance contact between the metal and the semiconductor. So, that is the reason for having this N plus doped region apart from very obvious reasons it is good to have a strongly doped strongly doped source and drain contact. So, these two together that is this metal and this doped region together make your source. So, essentially the potential here is the potential here. So, all this is short

circuit ok. And these two together make your drain ok. So, now let us look at some of the geometrical aspects of the MOSFET architecture.

So, we have. So, this is the MOS structure. So, you have the back contact which is that VB the source which is at VS the drain which is at VD the gate which is at VG they have an insulator between the gate and the semiconductor and all potentials are taken with respect to the source. So, what is important is VD's VG's and VB's. So, what is the geometrical aspects now this region between from where the source ends to where the drain begins ok. So, in that sense; so, this region the length of this region is quite important and it is called the channel length it is a technical term ok. So, when we said channel length we are talking about this distance from the drain to the source that is the length the electrons the carriers must travel if they want to go from the source to the drain.

Now, the channel length is quite an important parameters when you hear about Moore's law and when you hear about scaling when you hear about the technology the MOSFETs and the transistors becoming smaller and smaller it is the channel length that they are trying to reduce. Because, if you reduce channel length the speed of the MOSFET is expected to increase of course, they are reducing all the other parameters also which we will look at when we when we talk about scaling. But, it is a channel length that if you reduce the channel length you generally tend to improve the speed of the MOSFET. The other parameter is as to how wide this devices right. So, you have the same cross section through the page.

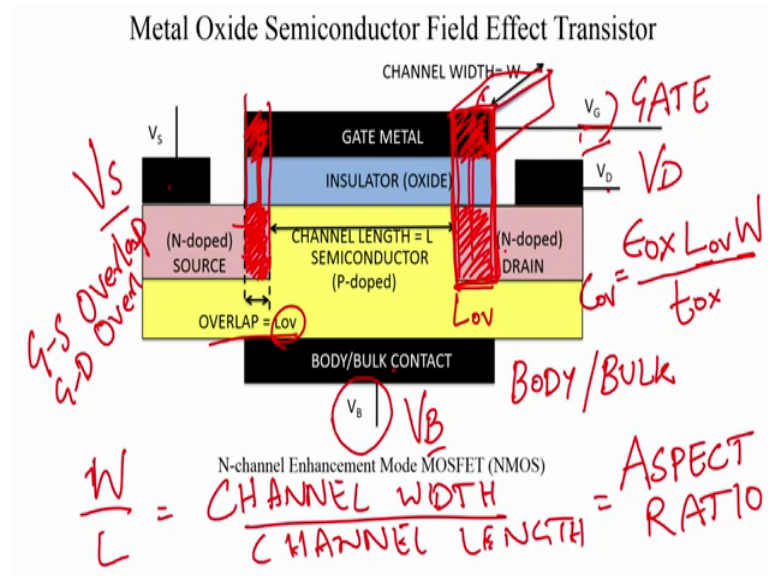
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So, as you look inside the page you have a certain width if you look at the perspective view the devices has got a certain width ok. So, that will be gate and so on. And so for so, that will be your contact and that is your semiconductor etcetera. So, I am not drawn it in perspective. So, you are looking at a cross section to the device has got a certain width and that width is called as a channel width ok.

So, that is the width of the channel and that is given a symbol W. So, when we say W and L we mean the channel width and the channel length and a special ratio which is particularly useful when we talk about currents etcetera in the MOSFET is the ratio of the channel width to the channel length ok.

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So, this ratio so the ratio which is basically W over L right; W by L is the channel width of the MOSFET divided by the channel length. And this ratio is particularly important in terms in the context of device design or circuit design and it is given a special name it is called as the aspect ratio of the device. So, when we say aspect ratio when we say the aspect ratio is 1, it implies the channel width is equal to the channel length and we say aspect ratios 2 it implies the width is twice that of the length and. So, on now that is the channel length and channel width now apart from that another important parameter with regards to frequency response in particular is the overlap length.

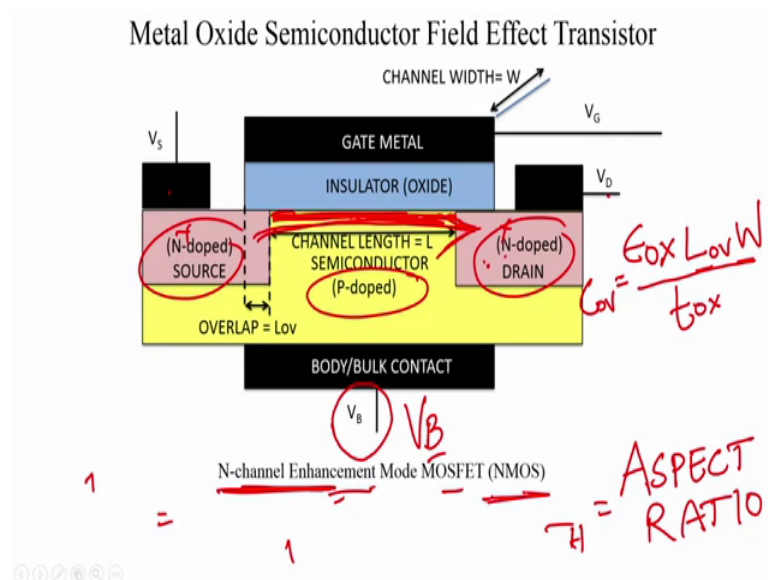
So, the source and the drain they extend below the gate. So, the gate can impact a certain region of the source and the drain. So, if you look at this cross section you can see that the gate metal is overlapping the source and the drain of course; there is an insulator in between. So, there is there is no direct current unless there are leakage currents there is no direct current from the gate to the source and drain or vice versa, but there will be a field impact the any voltage in the gate we will try to influence are these regions at this source and drain. And, this length of this overlap is something called as the overlap length or the gate to source overlap length and the gate to drain overlap length if these two are symmetrical will just say both of them are L overlap ok.

So, this essentially becomes a little capacitor right. So, what is the capacitance of this capacitor. So, it is epsilon A by D, but what is epsilon it is epsilon ox what is the area of

cross section or what is the overlap cross section. It is L into W . So, L overlap into W is that is overlap length into the width of the device it is the area of cross section divided by the thickness of the oxide t_{ox} .

So, that is the overlap capacitance which is the capacitance between the drain and the source other a many other capacitances because we have to PN junction diodes. So, therefore, there is a diffusion capacitance or a depletion capacitance etcetera etcetera, but we are into we are talking about the capacitance of this device this structure here. So, that is to do with the general architecture the design of the MOSFET there are many other small features, but mean these are the basic points alright.

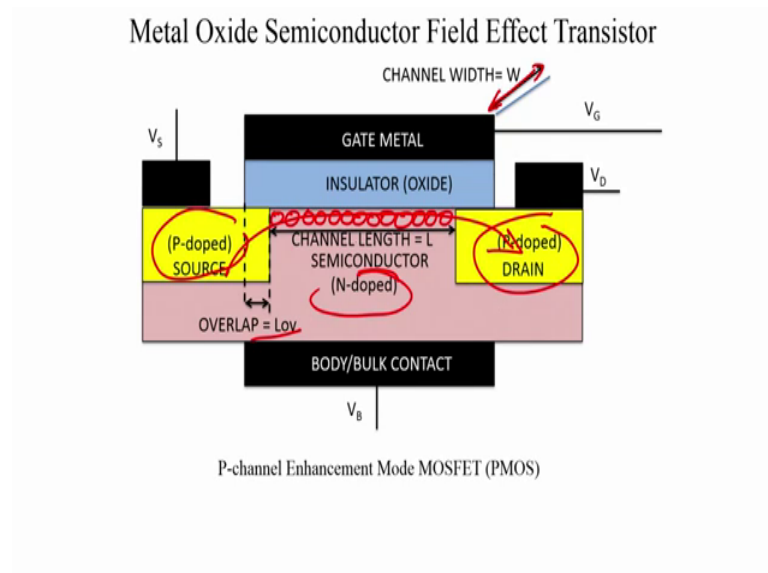
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So, this structure is got what it is a going to P doped semiconductor and it is got N doped contacts right strongly N doped contacts and the idea is when you have inversion you will have electrons which are the minority carriers between the source and drain. And you will have an electron channel going in from electron you will have a electrons being the current carrying current carriers between source and drain. So, this device is called an N channel enhancement mode MOSFET N channel means it is the electrons that are going to form the channel. So, this regional is called as the channel ok. So, that is the channel which is the conduit of charge transport. So, it is an N channel enhancement mode MOSFET we will simply call it as NMOS device or N type MOSFET or N channel MOSFET.

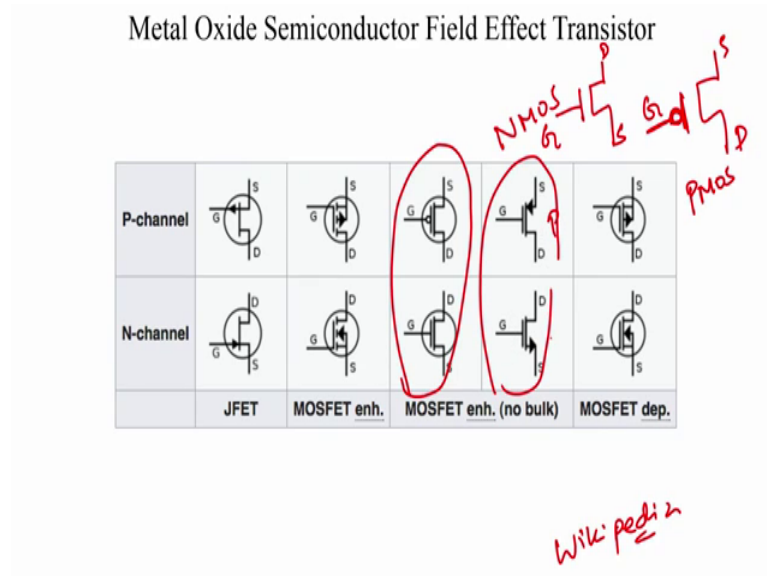
Similarly you could have the counterpart the complementary device which is the P channel MOSFET and for the P channel MOSFET you have to have a MOS capacitor with N doped semi conductor and you have P doped source and drain contacts.

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And, the idea is any inversion you will have holes at the interface which are the minority carriers and you will have holes being the carrier of the current we will have a hole current going from the source to the drain or from the high potential to the low potential. And, everything else remains the same you have an you have a channel width you have a overlapped length and you have a channel length.

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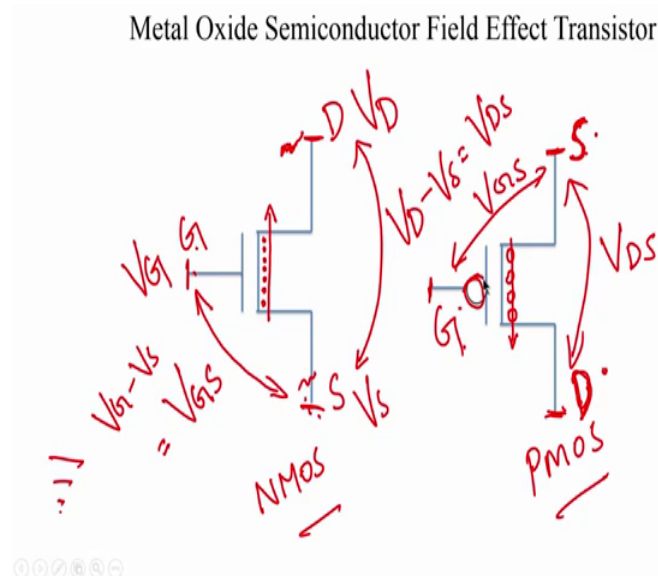
Now, there are different kinds of field effect transistors. So, I have taken this from an online source and these are the circuit equivalents. So, if you want to represent them as a circuit. So, these are the ways you would represent these transistors, but we are interested in the enhancement mode MOSFET right. So, we are interested in these 6 you have any of these options ok. So, you can use the any symbol you like, but if you are using let us say you want to represent the body contact or the bulk contact and you want to set the body a bulk contact it a different potential from that of the source.

So, normally we connect the body and the bulk to the source, but it can be may it can be used in a more clever manner by creating a potential difference between the body and the source. So, if you want to really use it that way you want probably using this symbol it shows the gate, it shows the drain, it shows the source and it shows the body here ok. So, that is the body terminal and here what it is telling you is that the body is connected to the source, but what I will be using is typically this.

So, this is just as a force of by the force of habit I tend to represent end channel devices like this and P channel MOSFETs with a circle there and that circle is probably comes from the use of the knot logic or the inverse logic. So, that becomes a P MOS device that is your N MOS device you cannot see the bulk contact in this ok. So, that could be your drain source and gate and these are your two devices ok. And, this is yet another

representation for the PMOS and the NMOS; but let us just stick to one we will just stick to this particular representation.

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So, here we have the NMOS and here you have the PMOS ok. So, in the NMOS we have the drain terminal, you have the source terminal and you have the gate terminal the body contact is not shown here. Now, the gate is at potential V_G with respect to some let us say universal ground, the source is at a potential V_S with respect to the same ground and this is at a potential V_D . Now, what is important with regards to the MOSFET are these potentials because that is what determines the electric fields inside the device.

So, it is the gate to source potential which is V_G minus V_S ok. So, when we say V_G it means it is V_G minus V_S or automatically the gate with respect to the source. And when we say V_{DS} it means it is the drain minus the source potential so, that is V_{DS} . Similarly for a PMOS you have the source the drain and the gate and the reason I am relocating the source, here is if you think of it from the point of view of a circuit ok. So, I am trying to sort of establish that thread right now, which is typically for an NMOS you will find that if this is the construct you will find that this is at a higher potential everything is with the respect to the source.

So, this is at a potential that is greater than the source the gate is at a potential is greater than the source. And, in the case of a PMOS you will find that if you want to continue using the same equations without changing the variables from gate to source to source to

gate etcetera etcetera. You want to be so, I am sorry gate to source to gate to drain etcetera etcetera. You want to sort of relocate these variables and in the manner where the source is at a higher potential, the drain is at a lower potential and the gate is at a potential that is greater than the drain ok. So, you will probably gather this intuition as we move along, but nevertheless that is the reason why I am just relocating the source here, it is basically the opposite kind of carriers ok.

So, it is the holes, it is the holes which are carrying current and the hole current is moving from the higher potential to the lower potential. In this case it is the electrons that are carrying current. And, the electron current is moving from the lower potential to the higher potential. So, in both cases the source is sourcing the carriers and the drain is accepting the carriers. So, if you want to think of it that way then that is the another way to look at this ok.

So, that is the source this is a drain and that is the gate and what we are interested in is in the gate to source voltage and the drain to source voltage. So, if you recollect if I tell you that the source is at a higher potential than the gate and drain, you will know that the V_{GS} and V_{DS} are negative in value ok. But, these are the important voltages and these are the circuit symbols we will be using for the NMOS and PMOS; the big difference in the PMOS is this is little circle and you see at the input ok. So, that is the difference.