Integrated Circuits, MOSFETs, OP-Amps and their Applications
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Lecture - 14
MOSFETs Characteristics and Applications (Current Mirrors)

So, we have seen in the last lecture actually, that was last module right of the same lecture, that how can we derive the relation between depletion type MOSFET in terms of drain characteristics transfer characteristics, and we have seen an examples also right?.

So, in this particular lecture a part of the same lecture in this particular module, let us see, how we can derive the MOSFET current voltage characteristics? And then let us see, how we can use this MOSFET as a very important application which is your current mirror? All right current mirror we will see it is interesting application.

So, if you see the screen what you see here is.

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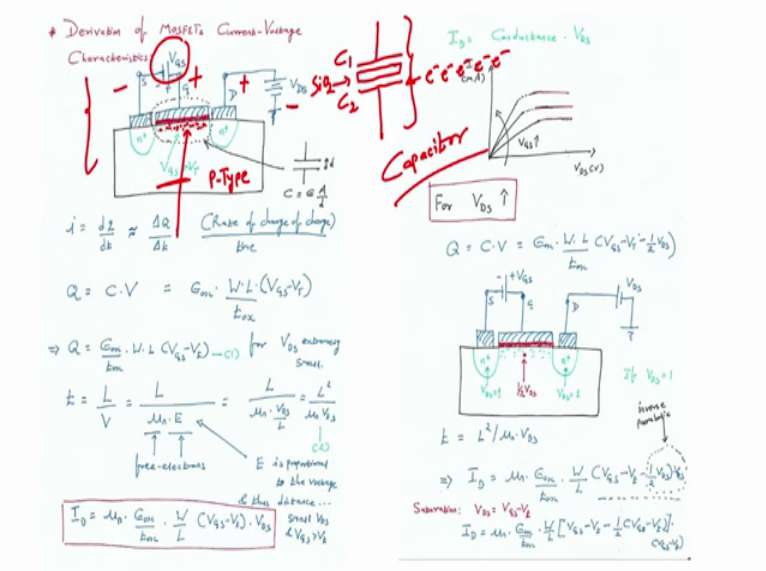

We have a MOSFET here, now you can see here this is nothing but N channel. So, we have P type substrate, we have P type substrate now there is no channel formation initially, but when my VGS is greater than V T, then there will be formation of channel right.

So, if I apply voltage if this manner; that means, my gate is positive compared to source, my drain is positive compared to source, right? Then what will happen? That means, why electrons will come in this particular region, and the channel formation will happen when VGS is greater than V T, the channel will form; that means, in this particular case how it looks like? It looks like I have a gate which is connect to a metal, then there is a oxide layer, and then there is a another metal why because this is made up of this is your channel, made up of electrons right this one..

So, it looks like there are 2 conducting plates, conducting plate 1 conducting plate 2, separated by insulating layer Sio2. So, what does this reminds us of? This reminds us that this looks similar to a capacitor right, capacitor is what? 2 conducting plates separated by dielectric material or air, right this why how we define the capacitor..

So, here we can see that there is a formation of capacitor, when you apply a positive gate voltage, and the due to which the electrons from the substrate gets attracted towards the gate and forms the channel, this channel forms 1 plate, the metal through which the conducts is taken is from is from another plate, while there is a insulator between the 2 conducting plates. So, this is nothing but your capacitor..

Now, if I have the capacitor, then I also know my capacitance is nothing but C equals to k A epsilon naught upon d right.

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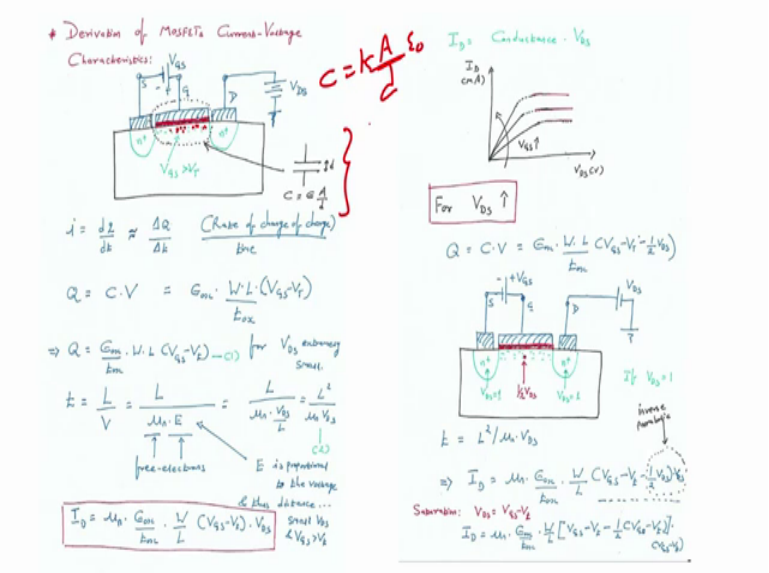

There is a formula that is fine that we all know..

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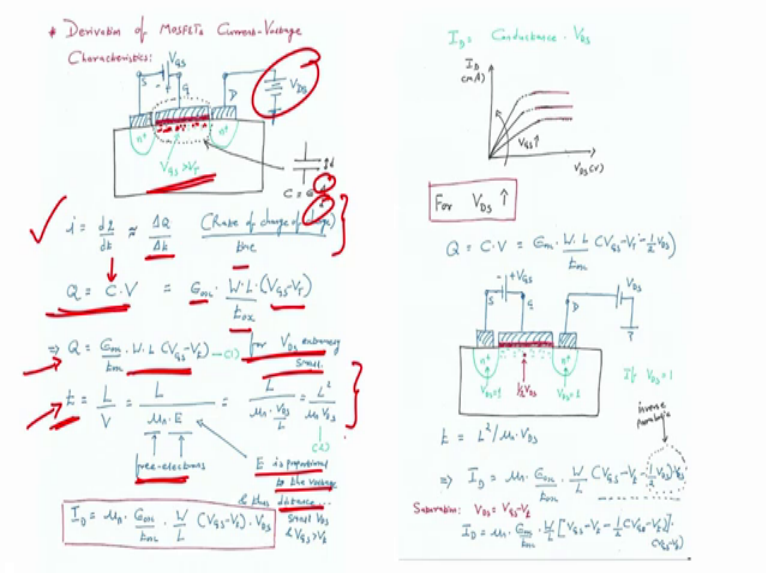

So, what, but we also know that current, what is current? Current is nothing but dq by dt, rate of change of charge divided by time right, current is rate of change of charge divided by time.

Now, what is charge, charge is nothing but C into V right, now we know this is nothing but epsilon naught the this is formula for C, epsilon naught W L t, V is VGS minus V T, why VGS minus V T? Because VGS is greater than V T, then only formation of channel will occur, that is why we are writing VGS minus V T right, that is our minimum voltage or the voltage, that is responsible for forming the channels for forming the channel between source and drain right.

So, again what we see, I equals to dq by dt or is delta Q by delta t, is nothing but rate of change of charge divided by time, now Q is nothing but C into V. So, C is nothing but capacitance. So, epsilon into W L by t right, epsilon naught A by d right; so, A by d is nothing but if you we can write width to length by t oxide, right into VGS minus V T.

So, let us consider this particular equation, Q equals to this value, for VDS extremely small, you see here VDS is extremely small all right VDS is extremely small, this is the condition guys, now what is my t? T is nothing but L by V right, what is v? V is mu into

E, what is mu into E? Mu is free electrons, and E is proportional to the voltage, and thus distance right E is proportional to the voltage and thus distance right.

So, time is nothing but length divided by velocity is nothing but mu into electric field, and this is nothing but free electrons, which is mu N; E is proportional to the voltage distance voltage and thus distance. So, if I substitute this value then my t would be L square upon L square, divided by mu N into VDS, this is my t value right. So, what I find is? My t equals to L square divided by mu N into VDS, L square divided by mu N into VDS right.

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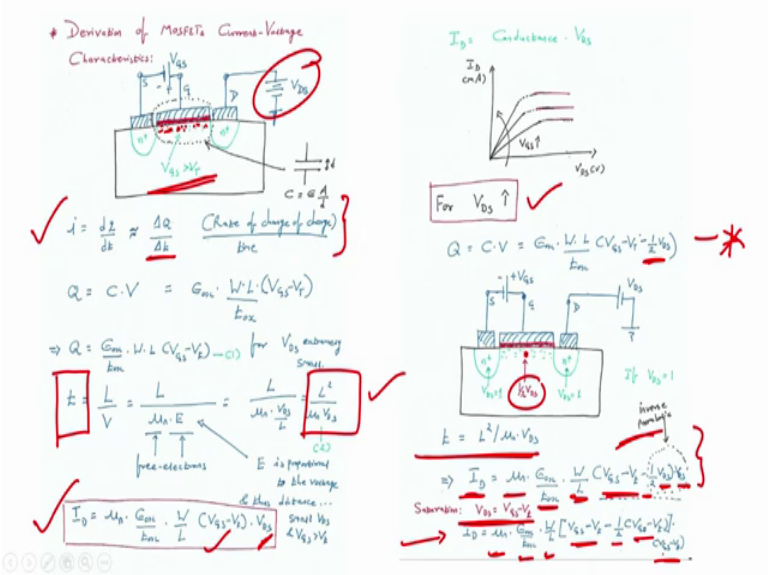

Now, if I substitute this value then what will I have? I will have ID equals to mu N right, epsilon naught x divided by t o x, into W by L into VGS minus V T into VDS, this equation right, I will get this equation, because now I know, what is the value of t? Right

So, if I substitute this value, then I will this particular equation, that is my ID right, because I know t I know Q. So, I can find ID, and I from ID; I know what is the relation between my drain current, and my voltage across drain and source right.

Now, if my VDS is high, in this case Q equals to C V we know, we know mu x W by L t o x, this is VGS minus V T, you see this equation remain same, but instead of VDS, we have minus half VDS because for higher V higher VDS, we have to consider the point

somewhere in middle of the channel which is nothing but, half times your voltage to voltage applied across source and drain half times voltage across the source and drain.

So, if I substitute this value now; so, I now have Q equals to this particular equation right, which is my equation let us say x right or equation star. So, t equals to I know this formula here L square by mu N VDS. So, if I substitute this value, what will happen ID equals to mu N this one, into W by L VGS minus V T minus half VDS, minus half VDS into VDS into VDS right.

So, what does this looks like, this looks where I nothing but, half VDS into VDS looks like a inverse parabola inverse parabola. So, if I substitute this value of VDS equals to VGS minus V T, what will I have? I have substitute VDS minus; VGS minus V T, here VGS minus V T here. So, I will substitute ID equals to mu N right, into this particular formula by W by L right, epsilon naught x upon t o x whereas, see this particular formula is epsilon x upon t o x, this one guys mu n, epsilon x, W by L, VGS minus V T, half instead of VDS, I will have right VGS minus V T. So, VGS minus V T into VGS minus V T.

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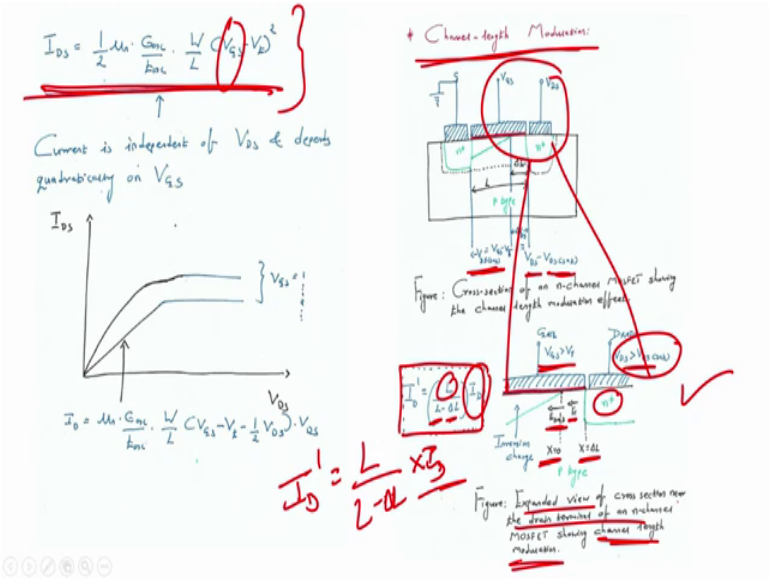

When I do this what I get is, I get the formula ID s equals to half times mu N into epsilon x upon t o x, this ox is because of oxide ox is because of oxide into W by L VGS minus V T whole square; that means, current is independent of VDS, you can see here in my

this region ids current is independent of VDS, but depends only on VGS, easy very easy right extremely easy.

So, if I now consider, let us see what is channel length modulation? So, I have the channel initially right, you can see here initially there is a channel like this, now if I keep on increasing VDS I told you right, if I keep on increasing VDS, then slowly even if I keep on increasing I changing the VGS slowly, the channel will start shrinking, towards the drain side.

So, if initial length is L, length between source and drain is L, then with amount of channel which has been shrunk is delta L right, then what will I have VDS saturation is VGS minus V T, where is I equal to VDS minus VD saturation, correct VDS minus VD saturation.

So, let us see here in this case if I have if I just mainly this particular portion, what will I see? I see there is a saturation, electric field x equals to 0 x equals to delta L this is my drain, my voltage across drain will be VDS is extremely high than VDS saturation, VGS is greater than V T, in this case the inverse charge will happen, and my ID formula would be nothing but ID dash equals to length minus original length minus change in the length is modulation right, which is my change in the channel modulation into my drain current ID.

So, in this particular case when we have to consider the channel length modulation, we have to consider the change in the channel into the current ID. So, this is the expanded view of cross section near the drain terminal, which is the this particular expanded we have this particular terminal like this, this is what it is here right in channel length modulation channel length modulation.

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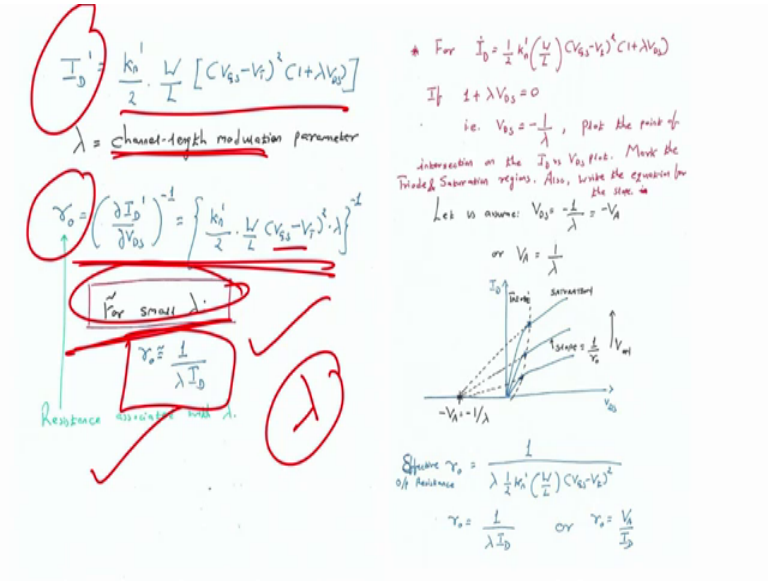

So, if I further substitute the value what will I have, ID that is equals to kn by 2, why kn by 2? Because I already have formula sorry. So, ID that is equals to nothing but kn by 2, W by L VGS minus V T into 1 plus lambda VDS, this is my formula when I consider the channel length modulation parameter, when I consider the channel length modulation parameter, then I have to and then I get this particular formula for the current for the drain current.

Now, if I want to see what is r o right that is this resistance associated with my lambda right, which is my channel length modulation parameter, then it is given by inverse of d ID dash by VD VDS right, equals to nothing but kn by 2 same thing, right VGS minus V T into lambda whole inverse or 1 by this particular formula.

Now, since lambda for small lambda I have nothing but, r o will be 1 by lambda I d. So, most of the time we consider the lambda is small, and that is why we can get the we can directly use the formula r o equals to 1 upon lambda ID, all right it is very easy, you can see that now here because of the channel length modulation parameters, we have the new value of ID dash right, which is this and now the r o which is resistance associated with lambda is given by this equation, where for small lambda we can write down r o equals to 1 by lambda ID.

So, if I am given a question; if I am given a problem right, that is more important you can solve a problem if you know this. So, you see this particular slide which is this one.

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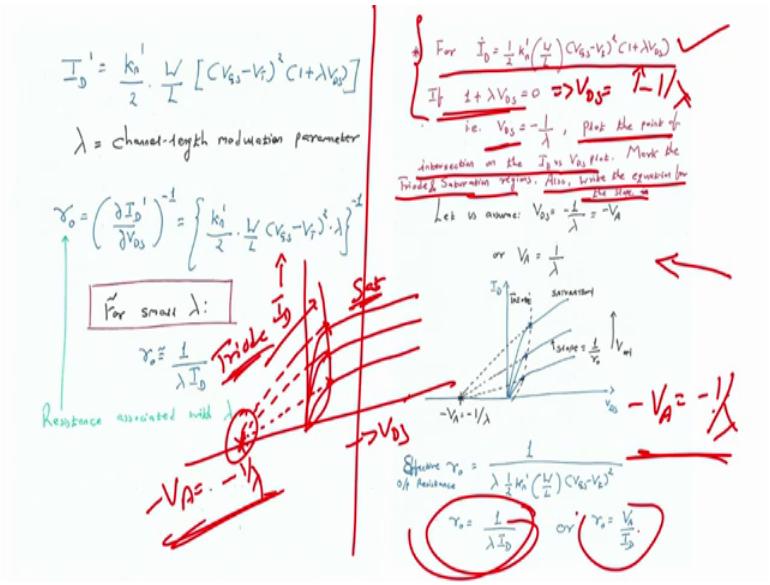

So, for ID equals to this value this equation, if 1 plus lambda VDS this particular value is 0, then VDS that is VDS equals to if this is 0; that means, that VDS equals to minus 1 by lambda right, if this is the case plot the point of intersection on ID versus VDS plot, marks the triode and saturation region also write the equation of slope.

So, what is the question if I am given this equation, and I am also given 1 plus lambda VDS equals to 0, and if I am asked to plot the point of intersection on ID versus VDS; that means, I am ask that you have ID you have VDS, why do not you point plot a point in for this given condition? Also tell us where is saturation region where is triode region. So, it is very easy right.

See my VDS equals to minus 1 by lambda, minus 1 by lambda will be nothing but in the in this region right, now what we have to do we have we have current right we have VDS. So, when I increase VDS I will have this kind of slopes is it, this kind of plot, when I have this my plot I just connect like this. So, this is my point of intersection, I can say minus V A equals to minus 1 by lambda right, my point of intersection.

Now, this region this region. So, I plot like this anything which is here is my triode, this is my saturation region, this is my triode region, right and my effective r o or output resistance is 1 by lambda ID, or I can also write equals to V A by ID, because V A lambda are related like this right.

So, if I substitute value of lambda, I can get r o equals to V A by ID, easy very easy right extremely easy, if you have any doubt ask me you can ask me through the forum, you can ask me I will help you out if you have any doubts. Otherwise the equation is so, easy that anyone can solve it the problem is so, easy that anyone can solve it right once you know the basics of your MOSFET right.

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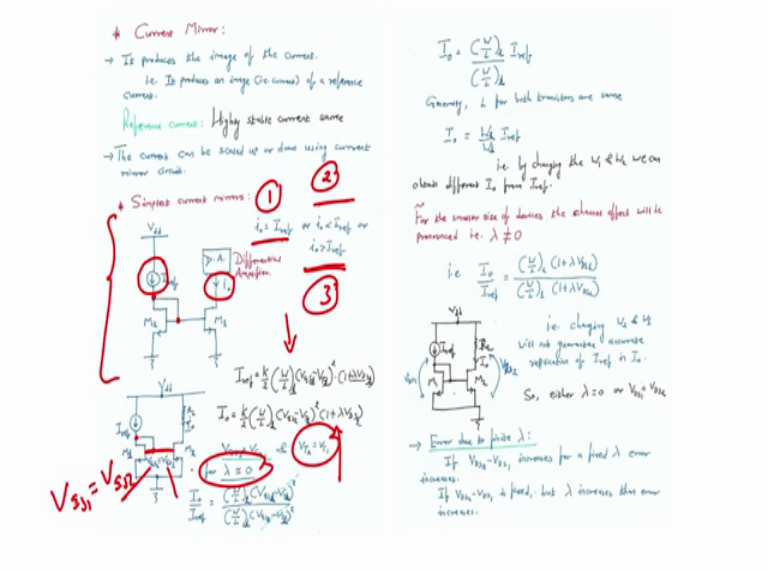

So, let us see a very important application of the MOSFET. So, that is the current mirror, now if you can come back to me, I can show you something yes. So, let us say you have a mirror right, in mirror when I place some mirror in front of my face, what can I see? I can see the image right if I put the mirror in front of my face I see my face right; that means, the image is replicated on the mirror, I can see the image of my face when I am looking at the mirror right.

Now, if you have gone through this phone walls, right they have different kind of mirrors where our body looks like fat, long, short, thin isn't it so; that means, that mirror cannot only show you your actual image, but it also shows you amplified version of your image, or a shrinked version of your image correct; that means, their mirror has a capacity to show you different images of course, of you only right..

So, it is not a movie hurry potter where you see in the in the mirror, whatever you are afraid of and you can see in the mirror right it is not similar to that, but in general when I talk about mirror what you see is your image, and you can change the magnification of

the images using that mirror. So, is there a mirror in electronics and can we change your magnify the current right, is there a mirror in electronics and can we change first of all can we replicate, second is if we can replicate, can we change the current if yes, can we magnify the current yes or no. So, we had to see that particular application in the current mirror all right.

So, come back to the screen, the screen it produces the image of the current right, current mirror is nothing but it produces the image of the current, it produces the image that is current of a reference current right, we require a reference current otherwise, how can it produce image? Reference current highly stable current source, because you has to replicate the current. So, the source should be also stable, and stable source is your highly stable current source.

Now, as I said currents can be scaled up or it can be scaled down, using the current mirror circuit all right using the current mirror circuit. So, for this if you see this particular circuit what is it? It is a simplest current mirror this is called simplest current mirror. So, you can see here the gate is connected to the drain right, this is MOSFET, there are 2 MOSFETs M 1 and M 2, there is a high reference here right and this is I o. So, I o is the mirror of I reference, and in this particular case, we can have I o equals to I reference, that is same we can have I o less than I reference, or we can have I o greater than I reference, we can have 3 conditions 1, 2 and 3 right. So, if I draw the circuit I can also draw like this.

Now, what I see is, I reference this I reference, what is I reference? I reference this equation we already know right, I reference is nothing but k by 2 W by L because it is one M 1. So, I am saying VGS 1 minus V T one whole square into 1 plus lambda VDS, we have seen this equation just before the slide right.

So, I o would be I o would be same thing just number 2 would be there, because M 2 MOSFET 2 is there right. So, in this particular case you can see here, when I am shorting this one and this gates are shorted; that means, the VGS and VGS is equal; that means, VGS1 is equals to VGS 2 right, and; that means, that my threshold voltage V T 2 should be equals to V T 1, if I V T 2 equals to V T one; that means, my lambda would be equals to 0, or in another term.

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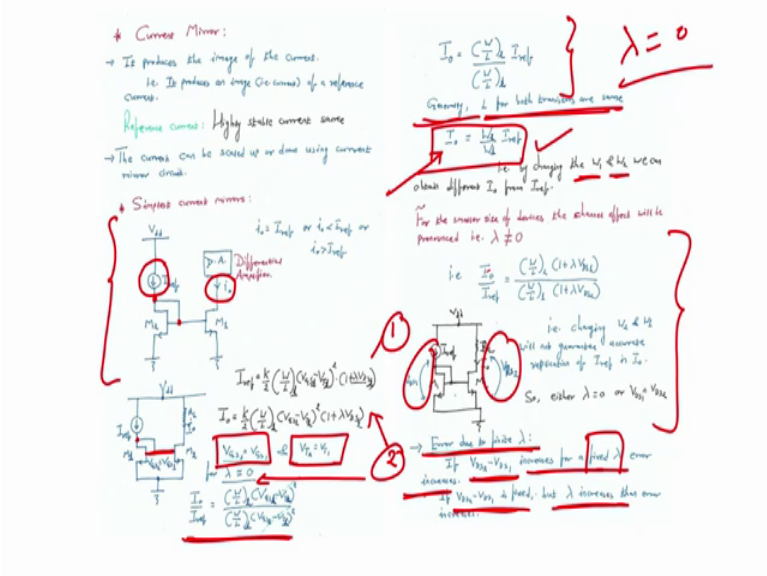

If I have VGS 2 equals to VGS 1, because this I have shorted and V T 2 equals to V T 1. So, let us consider first condition lambda equals to 0, for lambda equals to 0 if I divide the equation number 1 and equation number 2, such that 2 by 1; that means, I o by I reference I will have, I o equals to W by L of 2, divided by W by L of 1, into I reference right, I o equals to d by L of 2 divide by W by L of 1 into I reference.

Generally what you will see is, L for both transistors are same, generally we will find that the length for both the transistors are same, and that is why we can write I o equals to W 2 by W 1 into I reference, that is if I change w1 or if I change W 2, then I can see change in current right the mirror current, if I keep w1 equals to W 2, I will have same current if I if w1 greater than W 2, I will have higher current if I have w1 less than W 2, I will have lower current; that means, I have a circuit in which I can change the current, I can have same current, or I can increase or decrease the current right; that means, this circuit is nothing but a mirror circuit, it is a mirror and that mirror is of a current, and that is why it is a current mirror all right..

But what if the. So, this condition is true when we are considering lambda equals to 0, but what if lambda is not equal to 0,when lambda is not equal to 0, we have this formula 1 right, we have this formula, that is by changing W 2 and w1, we cannot guarantee that we can have replication of I ref in I o, because now this is the condition that we have to

consider, because here lambda is not equals to 0. So, in this particular case, what will happen? Then there is a error due to this lambda error due to this lambda all right..

So, let us see the first error, let us see the in the simplest mirror circuit, if I want to have I o by I reference equals to W by W 2 by w1 into I reference, either I can have lambda equals to 0 or I can have VD VDS1 equals to VDS 2, then only I can have this one gone, and I have this formula which is I o by I reference equals to W by L by W by L, if L is constant I o by I reference equals to W 2 by w1 into I reference.

But here if my lambda is not equals to 0, and my VDS1 is not equals to VDS 2, then there will be a problem, and problems are let us see first one is error due to finite lambda, there is a finite lambda then what kind of error is there if VDS 2 minus VDS 1, increases for lambda for fixed lambda error increases correct if my VDS 1, this VDS 2 and VDS 1 increases and lambda is fixed then my error would increase then my error would increase.

If I keep VDS minus V d VDS 2 minus VDS1 fixed, if I keep VDS 2 minus V d N VDS1 fixed, then for lambda increases then error again increases, then if my lambda increases error again increases. So, let us see the another one..

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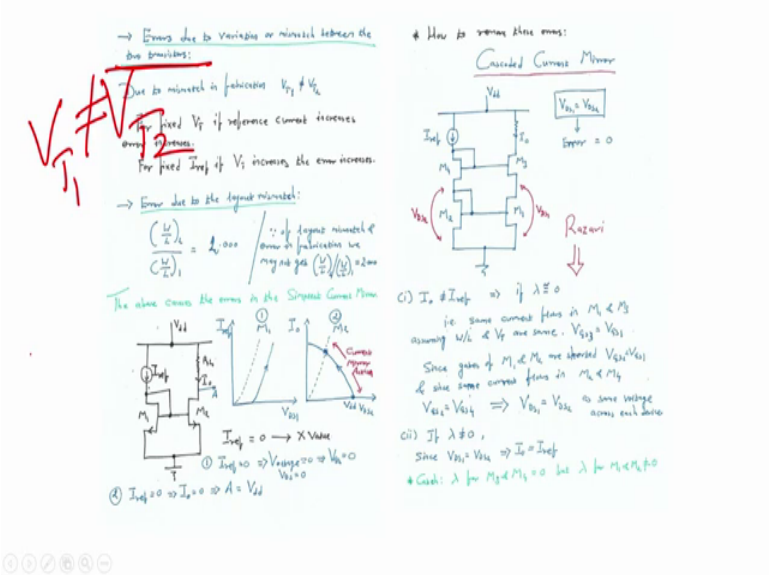

Error due to variation or mismatch between 2 transistors right, if there is a mismatch between 2 transistors that we have selected for designing the current mirror, what we will

see? The threshold voltage of first transistor will not be equal to the threshold voltage of second transistor, V T 1 will not be equal to V T 2 right, if threshold voltage is are not equal, then there is a mismatch between the threshold voltages..

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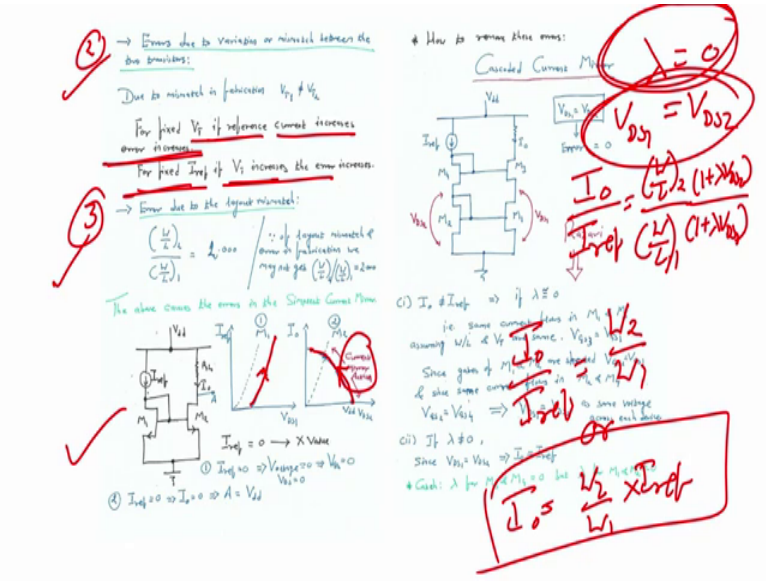

And that is why for a fixed V T if reference current increases, error increases or for fixed reference current if V T increases error increases, correct that is the second error that is the error number 2.

First error was error due to let us clear the screen. So, it is easy for us to understand, first error in the simplest mirror circuit is error due to finite lambda, second error is error due to variation or mismatch between 2 transistor, the third error is due to due to layout mismatch. So, if you guys have learn circuit designing, you will use cadence right, and then you when you design it you will see the there is a mismatch in the layout and design layout, then again there is an error right.

So, for example, if I want W by L of 2 divided by W by L of 1 equals to 2 right, because of the mismatch in layout, I will not have I may not get this particular value, and this will also generate in an error right. So, this all 3 errors are the errors in the simplest mirror current, this errors are the errors in the simplest current mirror.

So, this is just a current mirror action, if you see right my M 1 and M 2 right, if errors are increases my VDS my I reference increases right, when my I reference increases my M 2

is already in saturation right, I need to go back towards the current I o right, it because it has to follow just to follow, and then this is when it is increasing this in this one this is increasing in this direction, this is your current mirror action.

So, how we can reduce these 3 errors, this 1,2 and 3 then there is a technique called cascading current mirror right. So, what we want we want either our lambda equals to 0, or VDS 1 let us say VDS 1, should be equals to VDS 2 right, because if I see my equation, my I o reference, I o by I reference equals to nothing but, right equals to nothing but W by L, of 2 divided by W by L of 1, into 1 plus lambda VDS 2 divided by 1 plus lambda VDS 1..

So, to get I o by I reference equals to W 2 by W 1, or I o equals to W 2 by w1 into I reference, I should have I should have either lambda equals to 0 or VDS 1 equals to VDS 2, right I should have this 2 points, but I have nothing in simplest mirror currents in simplest current mirror circuit, I cannot have lambda equals to 0, and VDS1 equals to VDS 2, particularly when your VDS1 is not equals to VDS 2.

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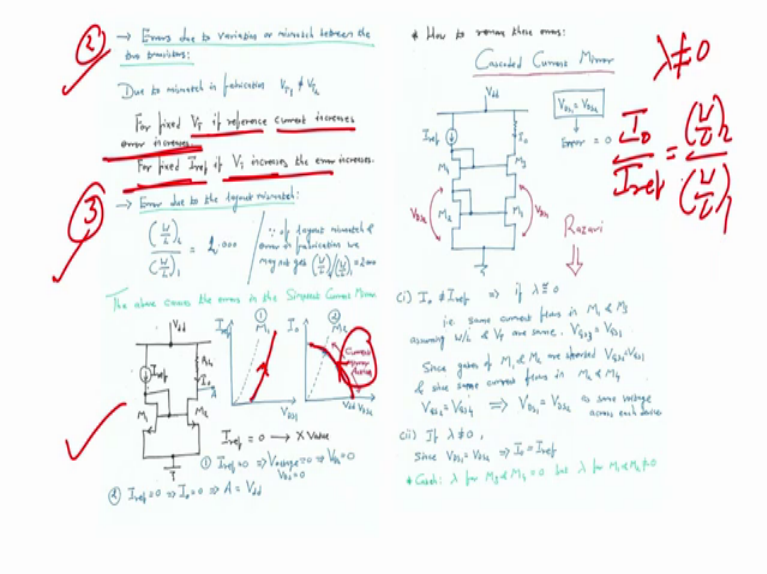

Particularly when your lambda is not equals to 0 right, then you cannot have this particular value where your I o by I reference, will be W by L of 2 divided W by L of 1 this we cannot right this we cannot have.

So, what can we do, we can use cascoded current mirror.

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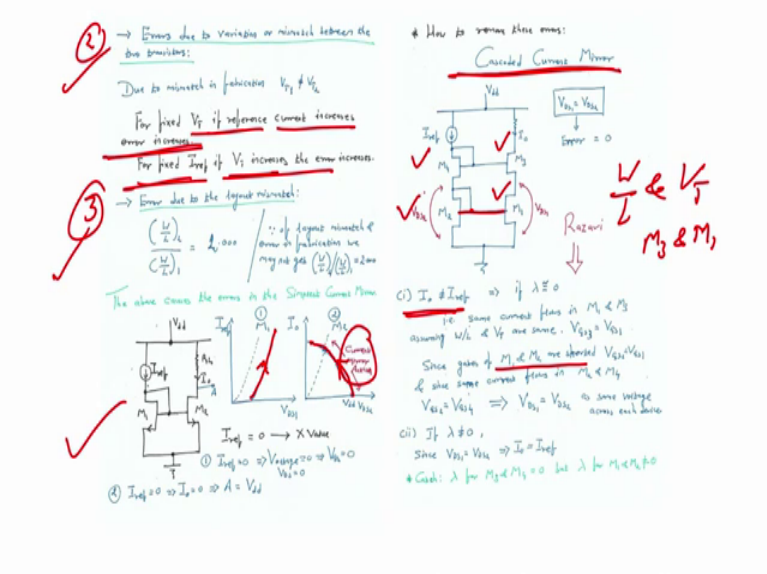

In cascoded current mirror, what we use? We use 4 MOSFETs M 1, M 2, M 3, M 4, we use 4 MOSFETs and we connect the drain to the gate like this, this drain to the gate like this, and then this gates are connected, this one is connected like this, M 3 and M 4 are in series, M 2 and M 4 are also in cascoded condition all right..

Now, you can see here, that if I have VDS1 equals to VDS 2; that means, this VDS 2 and 1 and 2 here, if my VDS1 equals to VDS 2, my error would be 0. So, cascoded current mirror where studied by 2 different groups, one is Razavi where he proposes that, if I o is not equals to I reference if lambda equals to 0, let us let us consider this particular condition I o is not equals to I reference, because if lambda equals to 0, that is same current flows is M 1 and M 3, same current flows is M 1 and M 3, assuming W by L and V T are same VGS 3, equals to VGS 1 correct, what it says? Is that if I consider my M 1 and M 3 all right M 3 and m1 all right.

And I assume that my threshold voltage of M 3, W by L a and threshold voltage of M 3 and M 1 is same right, threshold voltage an W by L ratio are same or threshold voltage is same and W by L ratio is same, of what M1 and M 3 in this case, since VGS 3 you see VGS 3 right is equals to VGS1, a since gates of M1 and M 2 are shorted, right since M1 and M 2 are shorted; that means, that VGS 2 should be equals to VGS1 right, and the same since same current flows in M 4 and M 2; that means, that VGS 2 equals to VGS 4 right..

So, first is when we V T equals to V T and W by L are same that.

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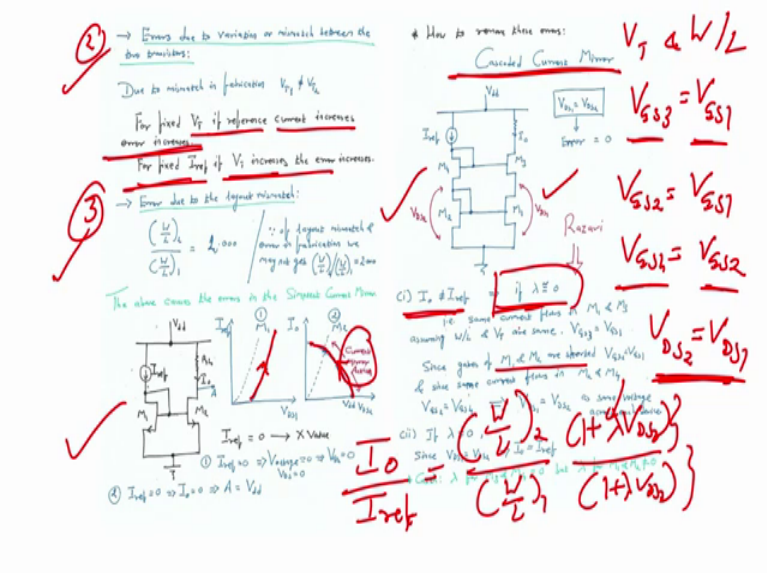

Means that VGS 3 equals to VGS1, because my V T and W by L V T and W by L are same right, W by L are same. So, VGS 3 equals to VGS1, all right now if VGS 3 equals to VGS1, since the gates for M1 and M 2 are shorted; that means, that VGS 2 will be equals to VGS1.

Now, since same current flows in M 4 and M 2; that means, that VGS 4 is equals to VGS 2, if this is the condition; that means, my VDS 2 would be equal to VDS1, and here we have considered lambda equals to 0, then if this is the condition, what will happen? My error will be not there why because my equation I o by I reference right, you have seen this equation correct this one. So, I o by I reference is nothing but W by L of 2 W by L of 1, 1 plus lambda VDS of 2 1 plus lambda VDS of 1 right, VDS 2 equals to VDS1 condition is satisfied lambda equals to 0, we have assumed here; that means, our error would be 0..

So, if lambda is not equals to 0, in that case, what will happen? In that case we will see here that.

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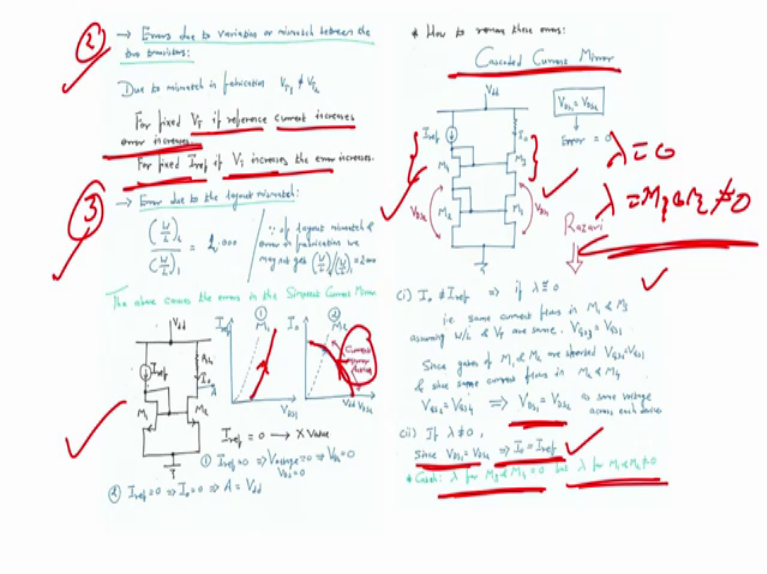

VDS one equals to VDS 2, implies I o equals to I reference right, but the catch is here the catch is, lambda for M 3 and M 4 is 0, but for M1 and M 2 is not equals to 0.

So, what we say is for if lambda is not equals to 0, then VDS1 equals to VDS 2 implies I o equals to I reference. So, both these condition is to remove the error, but here what we are assuming is that, lambda 4 M 3 and M 4 is 0, M 3 and M 4 lambda equals to 0, while lambda for M1 and M 2, M1 and M 2 is not equals to 0, this is not correct right either lambda for all the transistor should be 0, all lambda for all the transistor should not be equal should not be equal to 0.

So, this is the catch when we calculate, the that whether the error is not there using the using the method proposed by Razavi using the method proposed by Razavi alright. So, what we can do?

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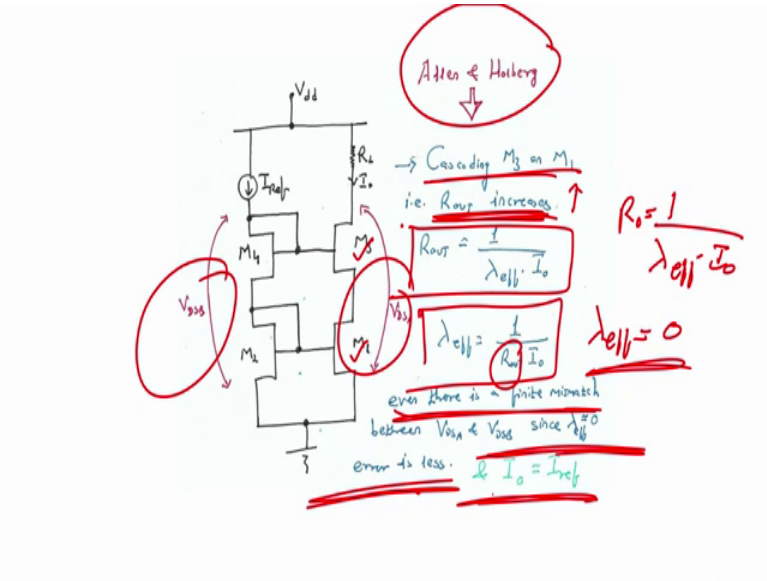

We can see another method that is proposed by Allen and Holberg. So, here what they propose is, let us consider that the cascoding M 3 on M1 this if I cascode M 3 on M1; that means, my R OUT increases right, because I am cascoding M 3 on M1 right, see if I cascode this MOSFET M 3 on M1, my R OUT would increase right that is shown.

Now, what is my formula for R OUT we have seen R OUT equals to R OUT equals to 1 by lambda into I o right, R OUT equals to 1 by lambda effective into I o correct. So, if that is the formula, lambda effective would be nothing but 1 by R OUT into I o, now R OUT is what R OUT is extremely high; that means, my lambda effective would be close to 0.

So, even there is a finite mismatch between VDS1 or VDS N VDS b, since lambda effective equals to 0, my error is less, and my I o will be equals to I reference, you got it very easy right super easy and this is it make sense when we discuss like this, when we discuss in terms of what Allen Holberg is proposing, it makes more sense because here if I cascade M 4 on M 3 m M 4 and M 2 or M 3 on M1.

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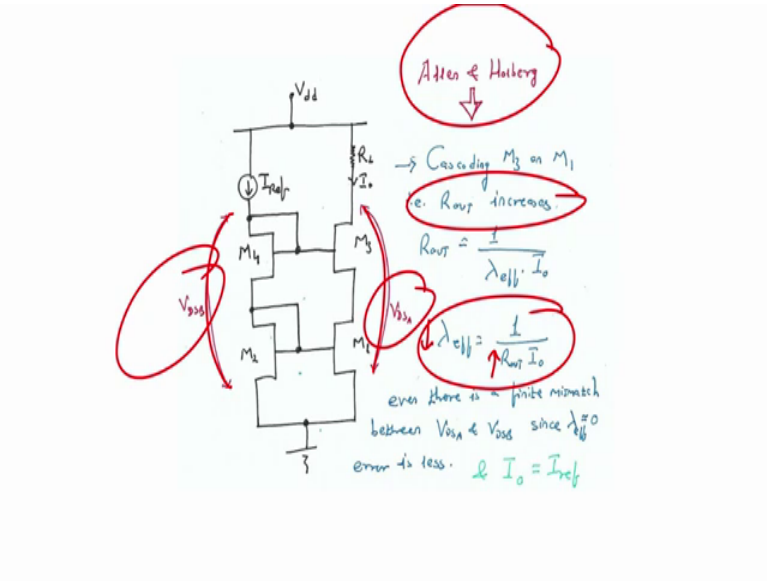

My R OUT would increase, my since my R OUT is related to my lambda in this particular fashion which is inversely proportional, I can see that increasing in R OUT with decrease in lambda, and that is my overall error would decrease, even there is a finite mismatch between my VDSA and VDSB; that means, Allen or Holberg propose that by using the cascoded kind of current mirror, we can reduce the error generated in the simplest mirror current in the simplest current mirror circuits right.

The errors in the simplest current mirror circuits can be reduced by using, cascoded current mirrors all right. So, this is end of application of current mirror, I just wanted to show you to you that how we can use MOSFET for a particular application that is the current mirror..

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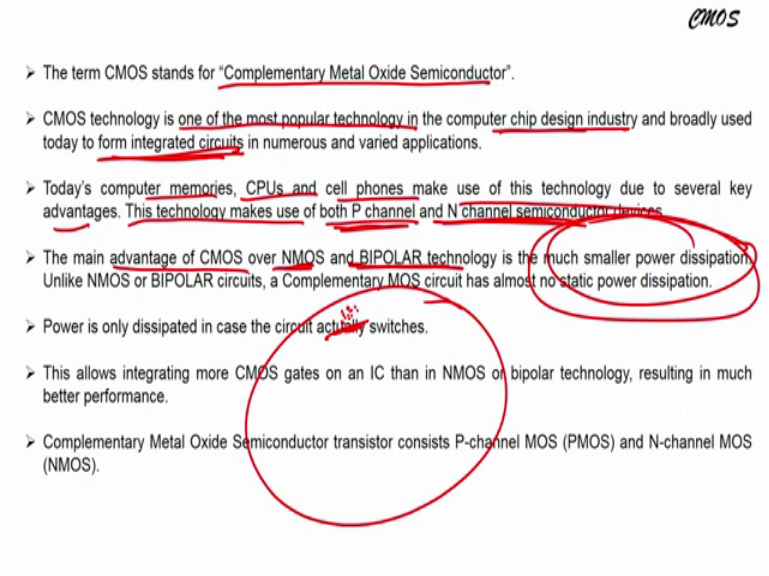

Let us go to the another point and that is your complementary metal oxide semiconductor right, and we will not go too much detail into this, but we will just see how this CMOS can be used as an invertor. So, CMOS stands for complementary metal oxide semiconductor, CMOS technology is one of the most popular technology in the computer chip design industry, and broadly used today form to form integrated circuits.

So, whenever you see an indicator circuits, most of the cases you will find CMOS right, this today's computer memories CPU cell phones make use this technology due to several key advantages, this technology make use of both P and N channel semiconductor devices, when you connect P channel and N channel MOSFETs, you will get complementary metal oxide semiconductor..

Now, the main advantage of CMOS over NMOS or bipolar transistor is, much smaller power dissipation, and that is very important, because we are going to reduce the number of components, or increase the number of components on a single wafer right, reduce the size of component and the increase the number of component on the single wafer, when you going to do that when you going to reduce the size the power consumption also get subsequently reduced, that is possible by using the CMOS technology compared to bipolar transistor or NMOS technology.

Power is only dissipated in case the circuit actually switches. So, power is not dissipated if circuit is ideal, only when it switches from one state to another state the power is

dissipated, this allows indicating more CMOS gates on an IC, then in NMOS or bipolar technology resulting in a better performance right, because only when it operates then only the our power is dissipated and that is why you can have more gates compared to bipolar NMOS.

Complementary metal oxide semiconductor transistor consist of, P channel MOSFET and N channel MOSFET.

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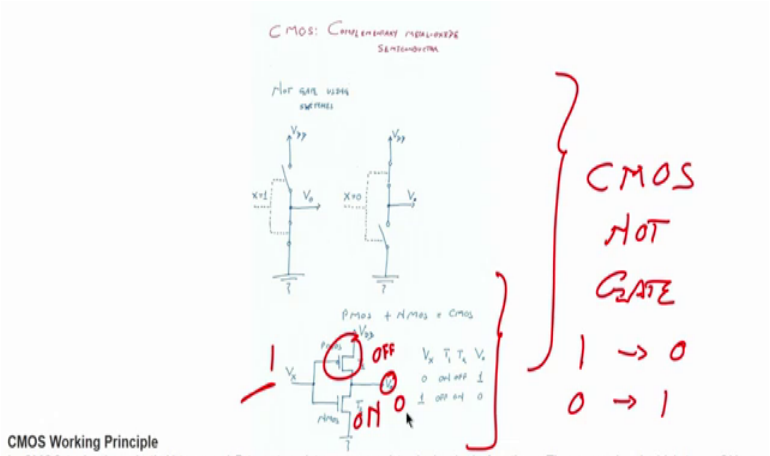

CMOS Working Principle

In CMOS technology, both N-type and P-type transistors are used to design logic functions. The same signal which turns ON a transistor of one type is used to turn OFF a transistor of the other type. This characteristic allows the design of logic devices using only simple switches, without the need for a pull-up resistor.

In CMOS logic gates **a collection of n-type** MOSFETs is arranged in a pull-down network between the output and the low voltage power supply rail (Vss or quite often ground). Instead of the load resistor of NMOS logic gates, CMOS logic gates have a collection of p-type MOSFETs in a pull-up network between the output and the higher-voltage rail (often named Vdd).

So, you can see here, we have P channel MOSFETs and N channel MOSFET. So, if you see is as not gate, if I want to use this as a not gate that is my CMOS as a not gate right, not gate you know if I apply 1 my output is 0 if I apply 0 my output is 1 right.

How can I operate then you see here, see there is a switch right there is a switch? So, you see here that if vdd is my voltage this is ground. So, if I have s equals to 1, this will be open my output would be 0, if my s equals to 0 this closes and my output would be one. So, this is how I can see the change..

Let us see here in this particular circuit, when I apply vx equals to 1 right, what happens? Vx equals to 1, my this is PMOS right this is PMOS. So, this will not conduct, and that is why this will be my transistor t 1 would be off, and t 2 would be on and; that means, that my output voltage will nothing but nothing but 0, but if I have reverse of this; that means, that if I apply vx equals to 0.

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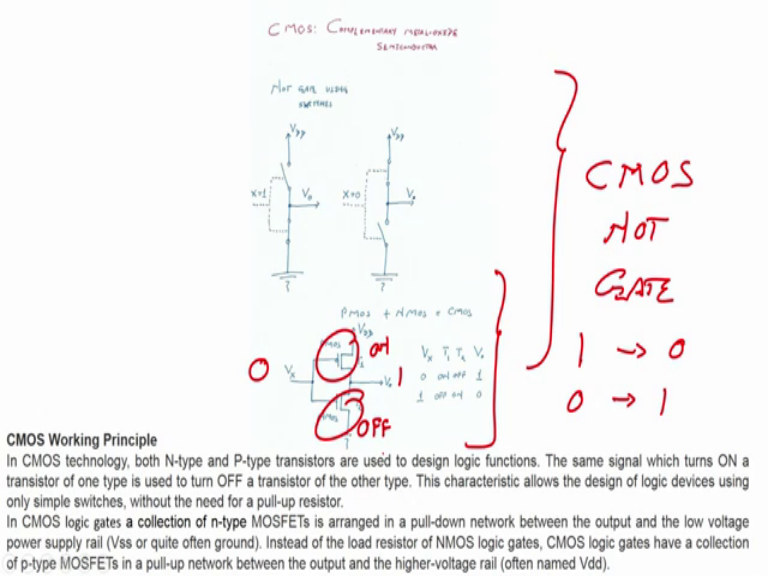

Then what will happen, this will conduct right this will not conduct so; that means, this is my t 2 would be off, t1 would be on and that my; that is my output would be 1.

Now, what is this, this is nothing but PMOS and NMOS connected together, PMOS and NMOS connected in series right. So, if this is the in this way if I can if I have the circuit, I can use it as a not gate. So, in CMOS technology both N type and P type transistors are used to design logic functions, the same signal which turns on 1 transistor will turn off, the another one will turn off, the another transistor type you can see right if I apply 1.

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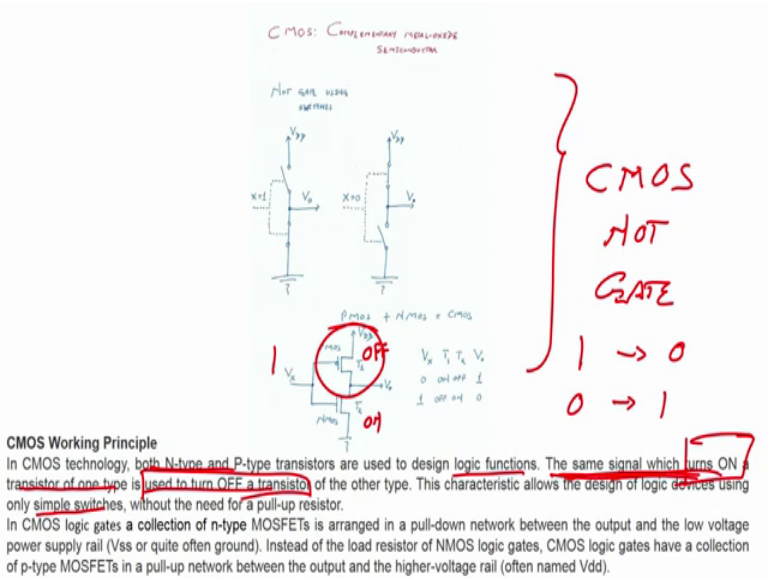

If I apply 1 this is off while this is on right, see the same signal which turns on 1 transistor, will turn off the another one will turn off the another transistor.

This characteristic allow the design of logic gates using only simple switches without need of pull up resistors, right when we do not require pull-up resistors. Here in CMOS logic gates a collection of N type MOSFETs is arranged in a pull-down network, between output and the low voltage supply right instead of load resistor of NMOS logic gates, CMOS logic gates have a collection of P type MOSFETs in a pull-up network between output and higher voltage right, here we instead of using the load resistors as a as a pullup resistors, we can use P type MOSFET as a part of in a part of pullup network right..

So, here this is how the CMOS is design, it is how it is connected and we will not go too much detail into CMOS, we have to just understand that if you are given a CMOS and if you are asked to form a not gate, you can use a not gate by just in by just attaching PMOS to N mos, and the advantage of CMOS is at one time only it will only dissipate the power when it is in the on state, when it is switches between the on state and off state, otherwise it will not dissipate the power that is the advantage of CMOS over the over the bipolar transistors.

So, with this what we have seen we had in the today's module, what we have seen, we have seen P channel we have seen depletion type, MOSFET we have seen the transfer characteristics, then we have also seen the application of the current mirror, and how what are the errors in the simplest current mirror. Then we have seen that can we reduce the error in the current mirrors that are there, and then what was a proposed idea the proposed idea is that we can use we can use a cascoded current mirror, to reduce the errors in the simplest current mirror, this current mirror were proposed by 2 groups one is from Razavi.

Another is from Allen or Holberg, and we found that the in the Razavis model, we had to assume 2 transistor lambda equals to 0, another 2 transistor lambda is not equals to 0, which will not work, that is why we had to consider Allen and Holberg where it make sense that if you if you attach transistors in the fashion in the cascoded current mirror, then your R OUT will increase, and since R OUT is proportional inverse proportional to lambda, that is why your lambda will decrease if R OUT is increase; that means, your

error would be close to 0, even there is a final difference between your voltage and error across the transistors I reference and I o; that means, that this particular model which is proposed by Allen and Holberg makes more sense to understand, how the errors are reduced in the simplest current mirror right.

Now, in the next class we will start understanding what are the operational amplifiers, and what are the characteristics of the operational amplifier all right. So, I will see you in the next class, and we will start understanding the operational amplifiers, which is also call the Op-Amps also call the Op-Amps.

So, look at the things that I have taught you today, if you have any questions feel free to ask me the courses designed in such a way that, you get the understanding and the idea of how the Op-Amps how the MOSFETs and IC s are fabricated as at the at the same time, we will touch the base of few of the topics..

So, that it helps you to cover most of the topics, in your analog circuit domain, there is another course which is advance version than what I am teaching right now, but what I thought is let us start with something which is more to which covers not only basics, it also covers the experiment point of view. So, we will also see lot of experiments as a part of this particular course. So, I will finish this module at this particular point, and I will see you in the next class till then you take care. Bye.