

Integrated Circuits, MOSFETs, OP-Amps and their Applications
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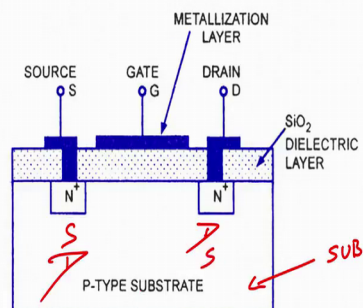
Lecture - 12
Operation of Enhancement type MOSFET

So, welcome to this module, in the last module what we have seen we have seen how we can design the process flow for a MOSFET right and I hope you have seen that lecture and you now have a basic idea if you are given a MOSFET, and if you are asked to design the process flow for fabricating the MOSFET you can fabricate the or at least process the design right.

And also with the earlier lecture now you are at least able to design the process flow for several devices right, it can be a bus sensor, it can be a gas sensor right same way it can be a micro heater right. So, the things becomes very easy once you learn the process flow and the recipe correct recipe for the particular process flow.

Now, in this module let us see further how can we understand the characteristics of a MOSFET, and how can apply the MOSFET as a current mirror that will we will we will be looking at.

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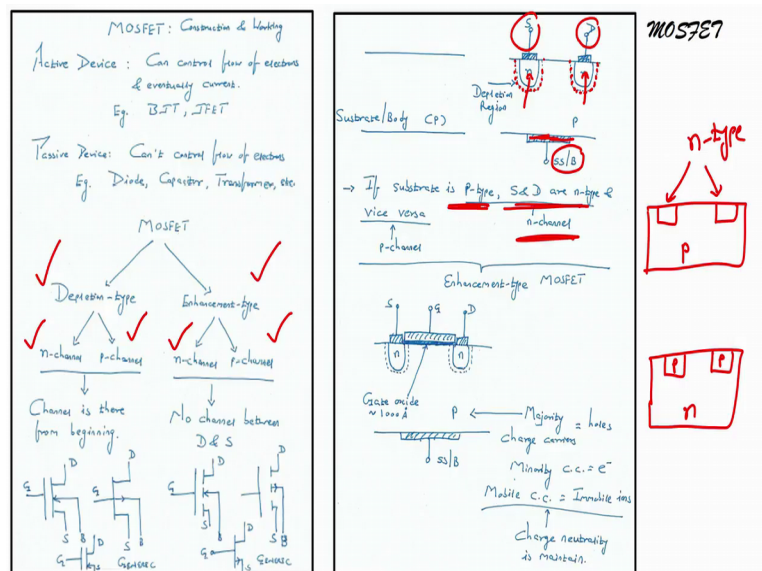


· N-Channel E-MOSFET Structure

So, if you come back to the screen what you see is the MOSFET that we have already seen this schematic which is your n channel enhancement type structure. And we already know n channel enhancement type structure as a P type substrate right is the substrate and then you have source, you have drain, it can be like this it can be in in a different way also the same the same thing does not matter it does not matter whether you consider this is source you consider this drain that does not matter ok.

So, it has source it has drain it has gate right and then we have to understand how this MOSFET will operate.

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So, let us understand the construction working of the MOSFET, the we know that what are active devices the active devices can control the flow of electrons and eventually the current for example, BJT, jFET MOSFETs these are all active devices passive devices are which cannot control the flow of currents and or flow of electron and these are diode capacitors right. So, these are examples of passive devices when we discussed about MOSFET or when we anyone discussed about MOSFET, generally the MOSFET is divided into 2 types one is your depletion type MOSFET, another one is your enhancement type MOSFET ok.

And then when we talk about depletion type, MOSFET then we further understand that there is a n channel depletion type there is p channel depletion type. There is n channel enhancement type there is p channel enhancement type. Now when we talk about

depletion type MOSFET, the channel is already there in the beginning, when you talk about enhancement type MOSFET there is no channel between source and drain what does that mean that right now what we have seen, we have seen this structure this structure is there a channel is there a channel, there is no channel there is no channel. So, this is your enhancement type MOSFET.

But if there is already existing channel between the source and drain, if there is a channel existing between source and drain then it is a depletion type MOSFET. So, from the beginning without applying gate to gate to source voltage, without applying drain to source voltage if there is a channel in the beginning its a depletion type, if there is no channel it is your enhancement type. So, remember these things remember these things ok.

You already know the in a this symbol for the depletion type, n channel depletion type, p channel depletion type enhancement type, n channel enhancement type p channel. now the basic difference here if you see here that the drain gate n source these are not connected right means there is a channel is not there. The channel is not there in depletion type the channel is already existing.

So, easy way of understanding whether is enhancement type or depletion type is, when you are given a the this symbol for the transistor then you can understand if there is a break like source drain and gates are source and drain is not connected, source and drain is not connected it is your enhancement type. Source and drain is connected in this particular fashion you can see here right then it becomes your depletion type, because channel is present in depletion type channel is absence in the enhancement type this is another way of understanding the or recognizing the type of MOSFET.

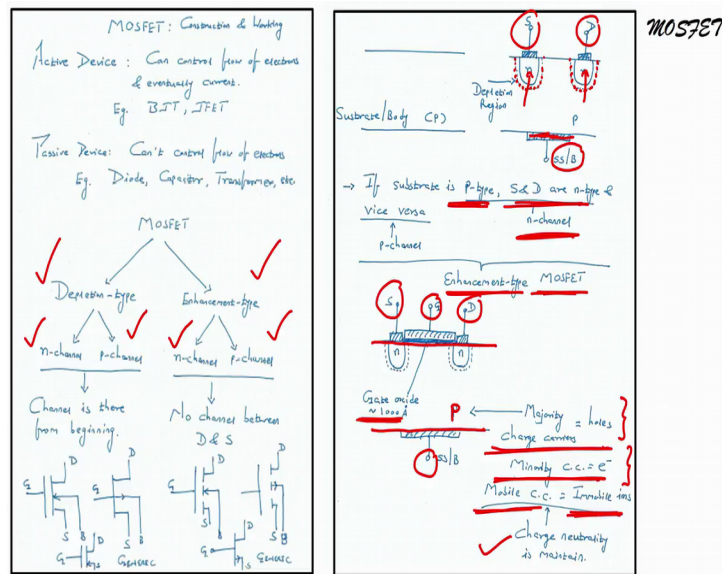
Now, you see substrate body right substrate body is P type and if I diffuse or if I dope the n channel into the P type, then this becomes my source and drain and because there is a p because there is a n there will be creation of this depletion region, there will be creation of depletion region as we can see from the schematic on the slide.

And you can see here there is a connection for the base or is connected for the substrate, connection for the base connection for the substrate connection for source connection for drain. Now this substrate P type source and drain are n type, then this n channel and the substrate is n type right source and drain are of P type what does it mean? If my substrate

that is my silicon right my silicon. If my silicon is P type then my source and my drain these both are n type if my channel is n type let us say my substrate is n type my source and drain are P type that is another way of understanding it another way of understanding it

So, see n type and P type I am talking about substrate, not talking about the channel n channel MOSFET is different now enhancement type MOSFET.

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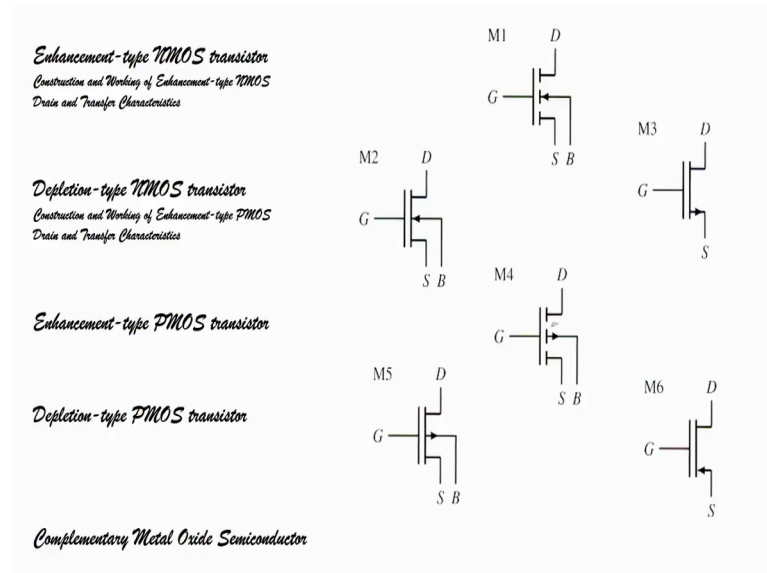
If talk about enhancement type MOSFET; let us see how the enhancement type MOSFET looks like.

So, what we see here is you see here this is the substrate, the substrate is P type right; that means, the majority carriers are holes right minority carriers are electrons, mobile charge carriers equals to in mobile ions right that is why the charge neutrality would be maintained easy right what is that P type majority are holes minority are electrons.

Now, for mobile charge carrier is equal to the in mobile ions so; that means, our charge neutrality will be maintained correct. Now you have source you have drain you have connection for source, you have connection for drain you have connection for a gate you have connection for your base or substrate right and you can see here the gate oxide is only 100 nanometre 1000 angstrom. So, here the gate oxide is extremely thin this is your enhancement MOSFET because you cannot see any channel any channel present

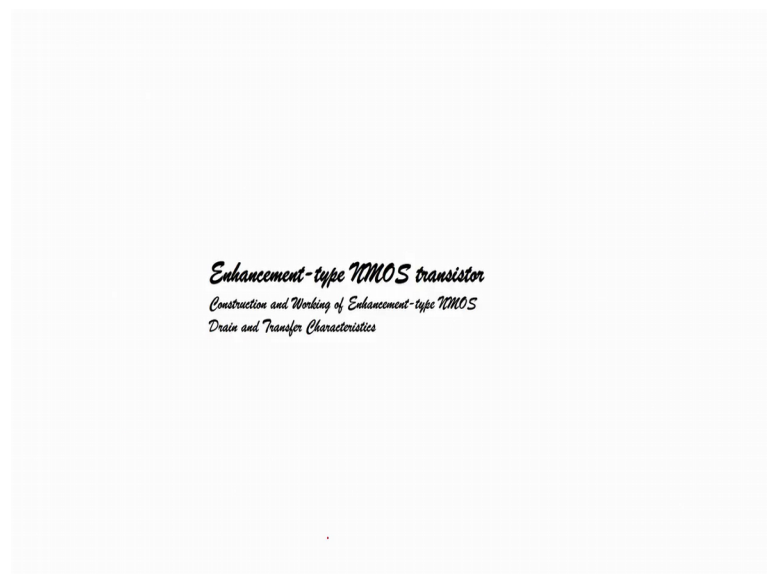
between your source and drain there is no channel between your source and drain easy. So, let us go to the next slide.

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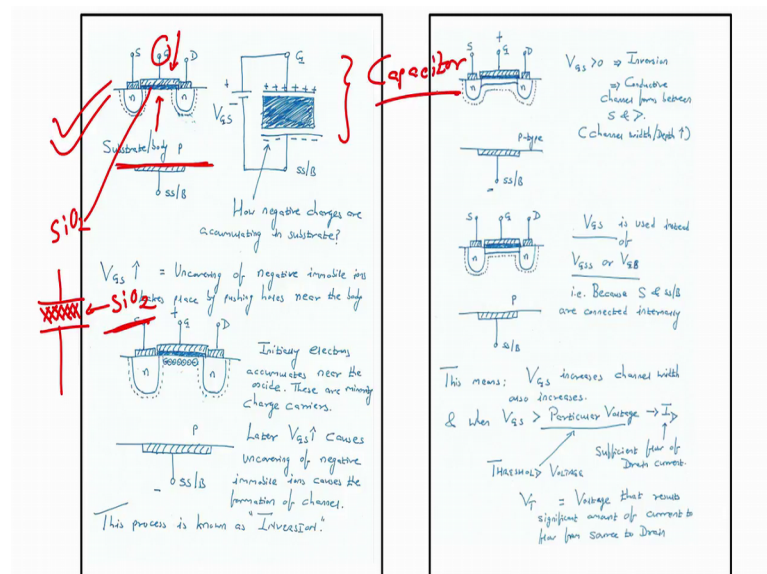
Now, whatever I have told you earlier is same thing, enhancement type transistors then see how the enhancement type transistors looks like, how the depletion type transistors looks like, how the enhancement type p mos transistor looks like, how the depletion type p mos transistor looks like and then we will also see the complementary metal oxide semiconductor ok.

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So, let us first talk about enhancement type n mos transistor.

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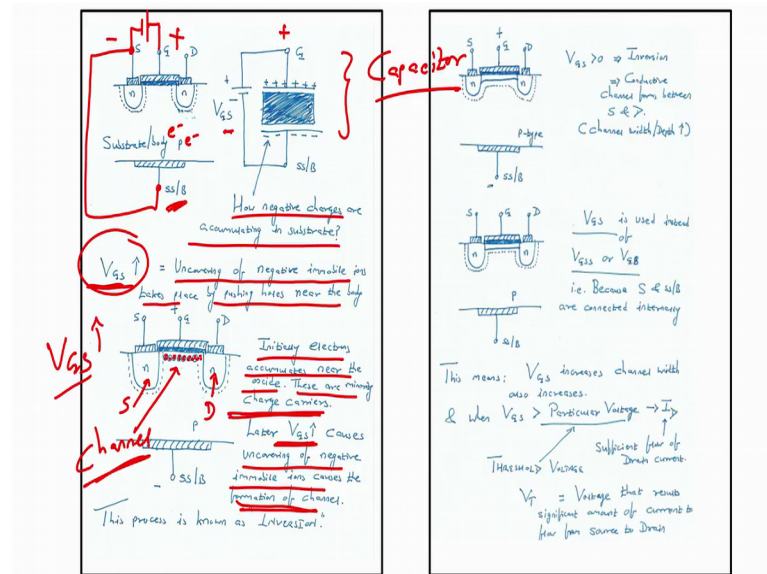


So, if you see this particular schematic, what does it show? It shows that you have a substrate and the type of wafer is P type, in that you have diffused n channel source and drain right and then you have a gate separated by a tinder of oxide and gate is a metal right.

So, now what will happen there is a metal here, there is conduction in this region and this is your oxide right this is your oxide; that means, it looks like you have 2 conducting plates separated by an insulating material and this insulating material is your silicon dioxide. It looks like when we when we see this particular figure this one, it looks like if you see gate right and if you see this body, and if you see this oxide looks like there is 2 conducting plates separated by a dielectric material. So, when you have 2 conducting plate separated by dielectric material it becomes your capacitor, that is the definition of a capacitor.

So, in this particular case you see the charge carriers if I apply VGS; that means, like this and apply negative gate positive gate is positive source is negative.

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Then in this case my gate would be positive, source would be negative right and I am connecting this thing to the source, again let me just write it down here. So, you can see clearly my source is negative gate is positive applying source to gate, gate to source voltage or source to gate voltage.

And I am connecting my substrate to the source I am connecting my substrate to the source, in this case this will be the connection, in which I can see that there is a positive charge there is a negative charge, negative charge, how it comes here because when I apply positive charge here then the minority carriers from P type, minority carriers from the P type that are electrons present that will come here towards the gate. It will get attracted towards the gate because gate is positive with respect to substrate right with respect to substrate gate is positive voltage. So, it is why negative charges would be like here and formation of channel would be there formation of channel would be there ok.

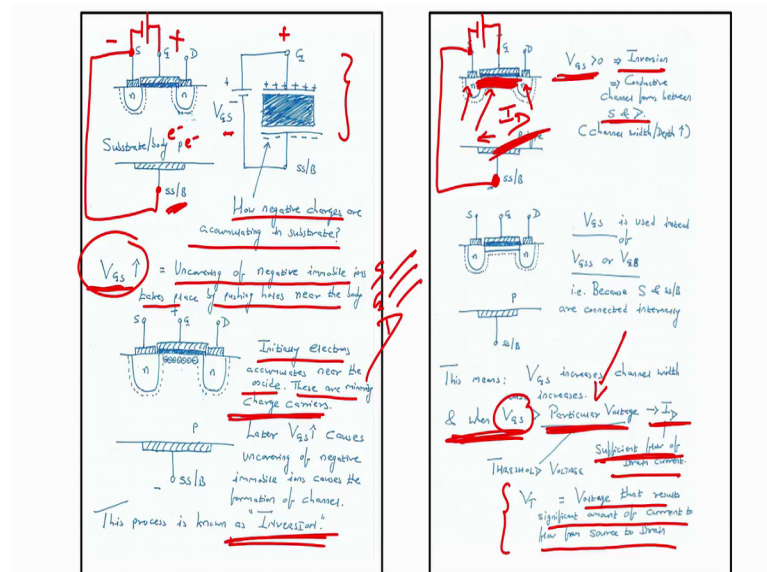
Now, there is a question, how negative charges accumulating in the substrate negative charges accumulating substrate, because you see here we have given a detail understanding here you can see the detail understanding, VGS when you increase on uncovering of negative mobile ions take place by pushing holes near the body right uncovering of the electrons that is here, we will take place right negative mobile ions is here electrons by pushing holes near the body. In this case initially electrons accumulates near the oxide, you can see the electrons accumulating near the oxide right when your

VGS is increasing; that means, your gate is more positive than compared to source your electrons that is the negative mobile ions will start accumulating towards the gate these are minority charge carriers these are your minority charge carriers ok.

Now, later VGS if we increase, if we keep on increasing VGS it causes uncovering of negative mobile ions right which forms the channel finally, it forms the channel if I keep on increasing VGS then lot of electrons will be accumulated here, and then it will form a channel between my source and my drain, there will be a formation of what we call channel, when my VGS I keep on increasing the gate to source voltage VGS easy right.

This process when the channel is formed on increasing VGS this process this process is called inversion. We have all studied this if not this, is the this process is called inversion got it easy. Now let us see further.

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Now, VGS is greater than 0; that means, inversion is there conductive channels forms between source and drain right this is conductive channel is formed between source and drain you can see.

And in this case when VGS is used instead of VGSS or VGB right we are using always VGS why we are not using VGSS because here see substrate is there right here the substrate is there, here the source is there right and we have connected the substrate and source like this we apply negative to source positive to gate, but we always say VGS we

never say V_{GS} or V_{GB} because source and substrate are connected internally. I have told you earlier also I have repeating it here, source and substrates are connected internally that is why you will find MOSFET ICs with only 3 terminals, only 3 terminals source gate and drain ok.

So, when this means that V_{GS} increases channel gate also increases correct. If I keep on increasing V_{GS} my channel width will also keeps on increasing right. So, when V_{GS} is increased below greater than particular voltage my current I_D is sufficient to for when my V_{GS} is greater than particular voltage, this voltage is greater than V_{GS} is greater than particular voltage what will happen? There will be sufficient flow of current sufficient flow of drain current why because now my electrons from source cannot reach to drain using the channel here. So, there can be flow of current I_D . So, this particular voltage right above which when V_{GS} reaches when V_{GS} reaches is called your threshold voltage all right. So, threshold voltage the V_{GS} should always cross in this particular case, we are talking about n channel MOSFETs n channel enhancement type MOSFETs when V_{GS} is increased greater than threshold voltage, then only I will be able to see that there is a sufficient flow of drain current easy.

That so let us see what is V_T . V_T is your threshold voltage voltage that results significant amount of current to flow from source to drain right this what we have seen that that is a minimum voltage that V_{GS} has to cross. So, that we can see that sufficient amount of current is flowing from source to drain right and this is your current I_D this is your current I_D ok.

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$V_{GS} > V_T \Rightarrow I_D \uparrow$
 V_{DS}
 $D +$
 $S -$
 V_{GS}
 $S +$
 $S -$

$V_{DS} = 0$
 $V_{GS} \rightarrow V_{GS}$
 Another reason of connecting source to substrate is to avoid too many bias potential.

If we have to find effect of voltage on depletion layer then find out V_{SD} .
 Using KVL: $V_G - V_{GS} + V_{DS} = V_D$
 $V_G - V_D = V_{GS} - V_{DS}$
 $V_{SD} = V_{GS} - V_{DS}$

Case 1: $V_{DS} = 0V$
 $V_{SD} = V_{GS} - V_{DS}$
 $\Rightarrow V_{SD} = V_{GS}$
 \Rightarrow Width of depletion region will be uniform.
 $V_T = 1V, V_{GS} = 2V = V_{SD}$
 Width of channel = Excess voltage = $V_{GS} - V_T$
 $= 2V - 1V = 1V$
 Similarly, $V_{GS} = 3V = V_{SD}, V_T = 1V$
 Excess voltage = $3V - 1V = 2V$

Case 2: $V_{DS} \neq 0V$ & $V_{DS} > 0V$
 $V_{SD} = V_{GS} - V_{DS}$
 Since $V_{DS} \uparrow$ is increasing
 $V_{SD} \downarrow$ reduces which implies drain is becoming more true than gate.
 \Rightarrow Depletion region is not uniform

Now, if I have V_{GS} greater than V_T , then what will happen my I_D will keep on increasing what is the case? Here the case is you see V_{DS} right drain is positive with respect to source. So, what will happen? When my gate is positive with respect to source drain is positive with respect to source, the drain will start attracting the electron from this source, but before the formation of before the flow of electron can happen initially there is no channel, but because the gate is at positive voltage compare to the source that is why there is a formation of channel and this formation of channel will help the electron from the source to move towards the drain creating in a drain current I_D .

So, as I keep on increasing V_{GS} my I_D will keep on increasing. So, another one is why we had to connect this source to substrate what is the reason of connecting source to substrate internally right. So, another reason of connecting source and substrate is to avoid to many bias potential, that if I do not apply. So, if I do not connect internally source to substrate, I do apply a bias potential. So, to avoid this. So, many bias potential I am using I am not applying I am internally connecting I am internally connecting the source and substrate all right or you can see that when you have I_C , the source and substrates are internally connected to avoid too many bias potential ok.

Next is if we find effect of voltage V_{DS} , on depletion layer. What will happen the effect of voltage V_{DS} on this depletion layer next find out V_{GD} right because we had to understand what is the difference in the what is the voltage that is developed between

gate and drain what when we had to find the effect of voltage VDS. So, if I want to find the effect of voltage VDS on depletion layer, I had to find what is the voltage across gate and drain all right. So, if I take this example if I take this schematic, which is right in front of you guys and I want to find this VGD then I had to use a Kirchhoffs voltage law.

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Left Panel:

Schematic of a MOSFET with gate voltage V_{GS} , drain voltage V_{DS} , and source voltage $V_{SS}=0$. The depletion region is shown between the gate and the channel. A KVL loop is drawn around the gate, channel, and drain regions.

Another reason of connecting source & substrate is to avoid too many bias resistors.

If we have to find effect of voltage V_{DS} on depletion layer then find V_{GD} .

Using KVL: $V_G - V_{GS} + V_{DS} = V_D$

$V_G - V_D = V_{GS} - V_{DS}$

$V_{GD} = V_{GS} - V_{DS}$

Right Panel:

Case 1: $V_{DS} = 0V$

$V_{GD} = V_{GS} - V_{DS}$

$\Rightarrow V_{GD} = V_{GS}$

\Rightarrow Width of depletion region will uniform.

$V_T = 1V, V_{GS} = 2V = V_{GD}$

Width of channel = Excess voltage = $V_{GS} - V_T$

$= 2V - 1V = 1V$

Similarly, $V_{GS} = 3V = V_{GD}, V_T = 2V$

Excess voltage = $3V - 2V = 1V$

Case 2: $V_{DS} \neq 0V$ & $V_{DS} > 0V$

$V_{GD} = V_{GS} - V_{DS}$

Since $V_{DS} \uparrow$ (is increasing)

$V_{GD} \downarrow$ which reduces which implies drain is becoming more like the gate.

\Rightarrow Depletion region is not uniform

When I use Kirchhoffs voltage law what will happen. So, we go from here right VG from here VG right then we go here this 1 minus VGS then we go here, here in this direction all right from here we go this way. So, VG minus VGS plus VDS plus VDS equals to VD right.

So, VGS VG minus VGS plus VDS equals to VD, if I rearrange the term we have VG minus VD equals to VG minus VD equals to VGS minus VDS what is VG minus VD VG minus VD is nothing, but 5 VGD right that is way; that means, my voltage at the gate minus voltage at the drain is nothing, but my voltage across gate and drain that is why I can find the relation between VGD and VDS, that is VGD equals to VGS minus VDS this is something that I have found all right.

Now, I want consider 3 different cases, let us see the first case first case when you consider case one VDS equals to 0 volts, VDS equals to 0 volts in this case my VGD my VGD is my VGS minus VDS we have found here right we have found let us say equation one. So, we have found from equation one that VG VGD is nothing, but VGS minus VDS right, but my VDS here is what case one VDS is 0 volt VDS is 0 volt. So, I

can write VGD should be equals to VGS because my VDS is 0 volt right; that means, width of depletion region will be uniform correct.

Now, if I my threshold voltage is one volt VGS is 2 volt then my VGD will be also be 2 volt. So, width of channel width of channel will be the excess voltage an excess voltage is nothing, but VGS minus V T which is my 2 minus 1 is one volt very easy right.

See what is a condition here; condition here is if I have a threshold voltage which is one volt and if I have a gate to source voltage which is 2 volt right.

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$V_{gs} > V_t \Rightarrow I_D \uparrow$

$V_{ds} = 0$

$V_{gs} = V_{gs}$

KVL

Another reason of connecting source & substrate is to avoid body effect.

If we have to find effect of voltage on depletion layer then find V_{gd} .

Using KVL: $V_g - V_{gs} + V_{ds} = V_g$

$\rightarrow V_g - V_{gs} = V_{gs} - V_{ds}$

$\rightarrow V_{gd} = V_{gs} - V_{ds}$

Case 1: $V_{ds} = 0V$

$V_{gd} = V_{gs} - V_{ds}$

$\Rightarrow V_{gd} = V_{gs}$

\Rightarrow Width of depletion region will be uniform

$V_t = 1V, V_{gs} = 2V = V_{gs}$

Width of channel = Excess voltage = $V_{gs} - V_t$

$= 2V - 1V = 1V$

Similarly, $V_{gs} = 3V = V_{gs}, V_t = 1V$

Excess voltage = $3V - 1V = 2V$

Case 2: $V_{ds} \neq 0V$ & $V_{ds} > 0V$

$V_{gd} = V_{gs} - V_{ds}$

Since $V_{ds} \uparrow$ as increasing V_{ds} which reduces V_{gd} which implies drain is becoming more like the gate.

\Rightarrow Depletion region is not uniform

Sorry and I want to measure the width of the channel, width of channel is nothing, but whatever the excess voltage is there right then only the channel will form right. What is excess voltage here VGS minus V T, VGS minus V T is what? VGS minus V T is one volt because of this one volt excess voltage there will be a formation of the channel this will be the width of the channel.

Similarly, if I have VGS equals to 3 volt right then an V T equals to one volt in this case my excess voltage will be 2 volts and there will be my width of the channel correct. So, case one we have considered when VDS equals to 0 volt. Let us see case number 2 case number 2 is VDS is not equals to 0 volt in that case what will happen and VDS is greater than 0 volt, not a not only it is not equal to 0 it is greater than 0. So, in this case VGD this equation is again equation number one right this one use this equation. In this case since

VDS increases because VDS is greater than 0 right VGD volt decrease correct if VDS increases VGD would decrease and this VGD reduces which implies that drain is becoming more positive than gate. If drain is becoming more positive than gate then depletion region will not be uniform easy very easy right.

See again let us see this condition this condition, see so easy. You have this VGD equals to VGS minus VDS, but if I keep on increasing VDS and what will happen if I keep on increasing VDS my VGD will keep on decreasing right easy. Now when if I VGD keeps on decreasing; that means, my drain is drain is becoming more positive, VDS is becoming more positive right and VGD is going down so; that means, drain is because VGD is nothing, but VGD is VG minus VD right VGD is nothing, but VG minus VD. If my VGD VG d is going down; that means, my drain voltage is getting positive becoming more positive than gate in this case depletion region is not uniform this case depletion region is not uniform.

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Case 3: $V_{DS} = V_{GS} - V_D$ ←
 $V_{GD} = V_{GS} - V_{DS}$
 $\Rightarrow V_{GD} = V_{GS} - V_{GS} + V_D$
 $\Rightarrow V_{GD} = V_D = V_T$
 \Rightarrow Channel width will become narrower & this happens only near Drain.
 This condition is called "pinch-off" & Voltage is called V_{DSsat}

Drain & Transfer Characteristics of Enhancement-Type MOSFET
 Output Voltage = V_{DS} (Control Variable = V_{GS})
 Output Current = I_D
 Drain characteristics: I_D vs V_{DS} for various values of V_{GS}
 V_T and constant K is already given.
 # Case 1: $V_{GS} > V_T$ "pinch-off" condition
 $V_{effective} = V_{GS} - V_T$
 $V_{DS} = 0 \Rightarrow I_D = 0$ | $\uparrow V_{DS} \Rightarrow I_D \uparrow$ | $\downarrow V_{DS} \Rightarrow I_D \downarrow$
 when $V_{DS} = V_{DSsat} \Rightarrow I_D = I_{Dsat}$

Let us consider then case number 3. In this case what we see we see that VDS is equals to VGS minus VC. Now this is another case right in this case if VGS equals to VGS minus VD, then we have this formula again equation number one which was VGD equals to VGS minus VDS because substitute value of VDS which is right over here, then I have VGD equals to VGS minus VGS plus VD this is gone. So, VGD is equals to

V_D and this is nothing over to threshold voltage; that means, the channel width will become narrower and this happens only near the drain correct.

What you understood is that from this equation if I consider this particular case, then I have then I have $V_{DS} = V_T$ right.

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Case 3: $V_{DS} = V_{GS} - V_{DS}$
 $V_{DS} = V_{GS} - V_{DS}$
 $\Rightarrow V_{DS} = V_{GS} - V_{DS}$
 $\Rightarrow V_{DS} = V_T$
 \Rightarrow Channel width will become narrow & this happens only near Drain.
 This condition is called "pinch-off" voltage is called V_{DSsat}

Drain & Transfer Characteristics of Enhancement-Type MOSFET
 Output Voltage = V_{DS}
 Output Current = I_D
 Drain characteristics: I_D vs V_{DS}
 Various levels of V_{GS}
 V_T and constant K is already given.
 # Case 1: $V_{GS} > V_T$ "pinch-off" condition
 $V_{effective} = V_{GS} - V_T$
 $V_{DS} = 0 \Rightarrow I_D = 0$
 $V_{DS} = V_{GS} - V_{DS} \Rightarrow I_D = I_{Dsat}$

And in this case what will happen? Because my V_{DS} is equals to V_T the channel width will become narrower, and this will happen near the drain and you can see here the channel width near the drain will become narrower when this becomes narrower; that means, that my volt my current is kind of the rig is constant my current rig is like constant right

And this particular voltage is called pinch off voltage. As if I am pinching of when you pinch something it stops flow its remains there right. So, this looks like we have pinched off towards increasing increasing, sometimes a pinch off voltage require and it starts saturating. So, it is also called V_D saturation right write voltage is also called V_D saturation or V_D set.

So, when V_D set will occur? V_D set will occur when you reach condition V_{DS} requires to V_{GS} minus V_T . So, we have seen 3 different cases case one was V_{DS} not equals to 0 right second case was V_{DS} is not equals to 0 and greater than 0 third case is V_{DS} equals to V_{GS} minus V_D ok.

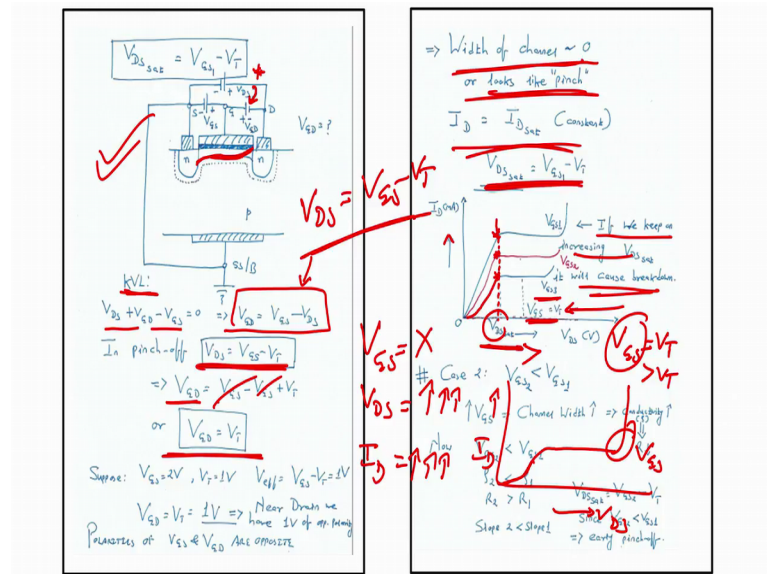
Now, if I want to understand, what is the drain and transfer characteristics of an enhancement type MOSFET I want to understand what is the drain and transfer characteristics of an enhancement type MOSFET let us see let us see. Now we know that output voltage is V_{DS} output current is I_D , and control variable is V_{GS} because if I keep on increasing V_{GS} my current increases correct. So, control variable is my V_{GS} now drain characteristic is I_D versus V_{DS} for various levels of V_{GS} that is we have to see.

Now, V_T and constant k is already given; that means, that we already know what is value of threshold voltage is already there, now what we had to do is consider different cases right first case is that V_{GS} is greater than V_T . When your gate to source voltage is greater than the threshold voltage what will happen? Effective v effective is nothing, but $V_{GS} - V_T$ right we know that $V_{DS} = 0$ implies current equals to 0 right when we applied V_{DS} equals to 0.

That means if I do not apply anything here if I apply 0 voltage here, you see in the left side right then the current will be 0 it will not flow right if I increase V_{DS} my current will start increasing right. So, and it will increase until a voltage, which is my pinch off voltage that we already seen right and my current will become constant my current will become constant, the pinch off voltage is nothing, but my V_{D} saturation this is easy right

Case one V_{GS} greater than V_T V effective is $V_{GS} - V_T$, $V_{DS} = 0$, $I_D = 0$, V_{DS} increases I_D increases and $V_{DS} = V_{D}$ saturation that is my pinch off voltage.

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In this particular condition if my VD saturation are VDS is VGS minus V T what will happen let us see ok.

So, here if I apply Kirchhoff voltage law for this particular circuit what will I have? VDS we start from here VDS and in direction like this. So, VDS plus VGD minus VGS equals to 0 implies VGD is VGS minus VDS. This is similar condition right in pinch off voltage in pinch off VDS is VGS minus V T we know that right in pinch off VGS minus V T right. So, in pinch off my voltage across drain and source VDS would be equals to VGS minus threshold voltage, then my pinch off will occur in this particular condition I have VGD equals to. So, I have substitute this value in this particular equation ok.

So, VGD a is equal to VGS minus VGS plus V T this gone VGD is nothing, but my threshold voltage V T right. So, width of channel looks like is reach 2 0, width of channel it goes on decreasing. So, from here it will go on decreasing it will decreasing and then it will reach here, what you can see here on the left side, left side what I have drawn you see right it looks like it is approaching 0, and that is why I D would be I D saturation.

Now, you see VD set equals to VGS minus V T we know that right.

So, if I apply if I keep on increasing my VDS, I can see change in my I D I keep on increasing my VDS you see again see change in my I D right, but that cannot reach that also has to depend on my VGS right. So, I have VGS equals to 1, VGS 2, VGS 3, 2 VGS

equals to threshold. So, above this value where V_{GS} is greater than threshold value V_T above the value here the bottom. Where V_{GS} equals to V_T as well as V_{GS} is greater than V_T my current can start flowing we have seen this in the first slide right; that means, on increasing voltage, I can see change in increasing current or depending on how much V_{GS} we are applying. So, if I keep on increasing my V_{GS} I can see the higher current we can obtain, and this particular region you will see that there is a saturation or pinch off region right.

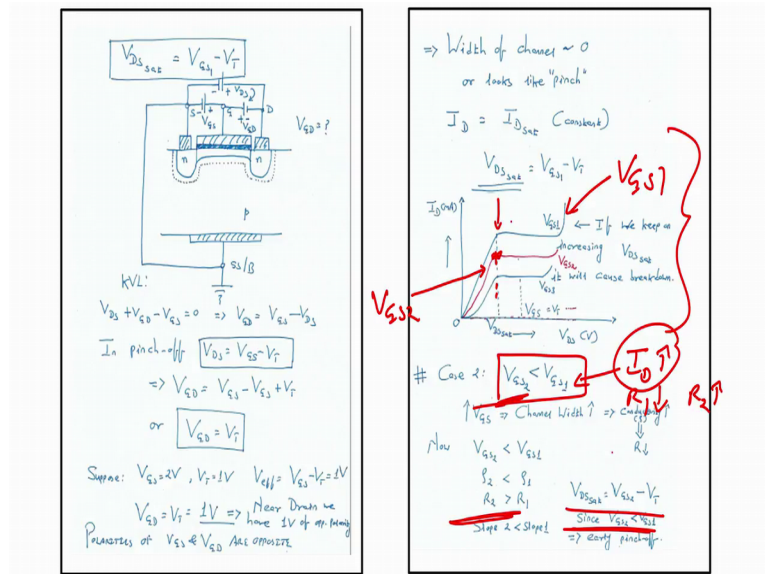
So, if you keep on increasing V_D saturation, if I keep on increasing this V_D saturation right it will cause a breakdown. For a particular value of V_{GS} let us say V_{GS} is let us say some constant x right we have V_{DS} we have I_D . So, if I keep on increasing V_{DS} what I will see is that, my current keeps on increasing this is V_{DS} this is I_D . If I keep on increasing my V_{DS} , if I keep on increasing my V_{DS} then what I will see I will see the change in the current depending on the gate flow voltage.

And then it will keep saturating V_{GS} it will reach here still I keep on increasing V_{DS} still I keep on increasing V_{DS} , then suddenly you will see that it starts breakdown. It suddenly the current shoots up and this is my breakdown condition all right and my MOSFET can be damaged.

So, what we understand is that for a constant V_{GS} we can apply V_{DS} , but you see exceed certain voltage of V_{DS} we may see the breakdown effect. So, now, let us see another case, we have seen the first case right where we have considered where we have considered that V_{GS} is greater than V_T .

Let us consider second case where $V_{GS 2}$ is less than $V_{GS 1}$.

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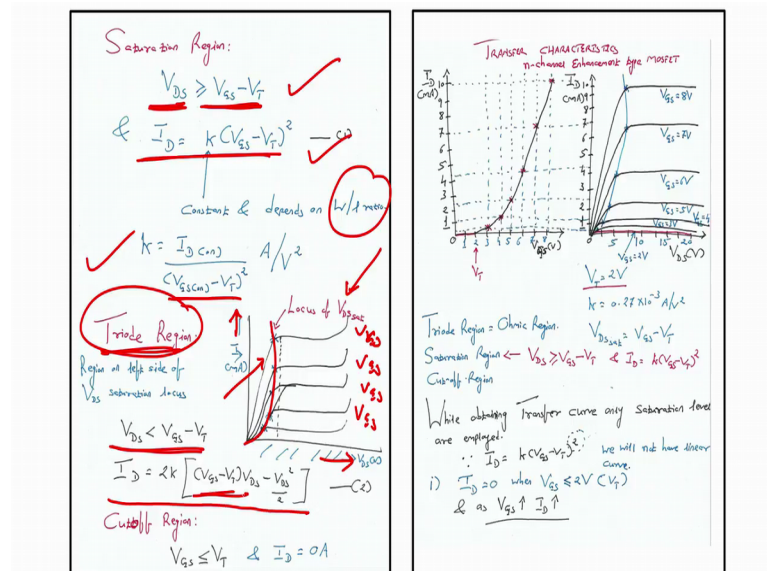
VGS 2 which one VGS 2 this red colour here, this the line which is shown by brown colour or red colour is VGS 2 and this line is your VGS 1. So, let this case consider VGS 2 is less than VGS 1; that means, channel and VGS VG s is channel width right if I increase channel width my conductivity would increase, or my resistance would decrease.

Now, when VGS is less than VGS two; that means, my resistivity at 2 is less than resistivity of 1 or R 2 is greater than R1 right. So, what will I have VDS equals to VGS minus V T and that then we have nothing, but since VGS is less than VGS 1 that is why slope 2 is less than slope 1 and early pinch off will occur early pinch off will occur.

Let us see once again what does that mean that, if I have this particular equation where my VGS 2 is less than VGS 1; that means, I see that the resistance at 2 is greater than resistance at one right, because the gate to source voltage is more; that means, that what will I see is current at VGS 1 would be higher because resistance at one is lower compared to resistance at 2 is higher that is resistance, because of VGS 2 resistance would be higher compared to resistance that is when the current would be higher in case where I am applying VGS 1 and when I am applying VGS 2 my current would be less you can see here from the graph also that for different value of VGS I have different value of current right this VDS since VGS is less than VGS 2.

So, what will happen early pinch off. So, you can see here my pinch off happens early compared to VGS.

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Now, if there is a saturation region, what is situation region. So, when my VDS is extremely high I told you right when we reach VDS extremely high, greater than VGS minus V T, and my I D equals to k times VGS minus V T volts square then what will I have? My k is nothing, but this particular value now we are not interested in deriving the equations not in detail deriving equations. So, right now you just understand that if this is the equation given to you what you can understand from the given equation that is the idea not to really derive the equation we will see one 2 derivations later, but right now if you are given the equation from the equation can you understand what is a drain characteristics if I change the drain to source if I change gate to source voltage, how the overall things would happen, how the performance of the MOSFET is going to change that is the idea ok.

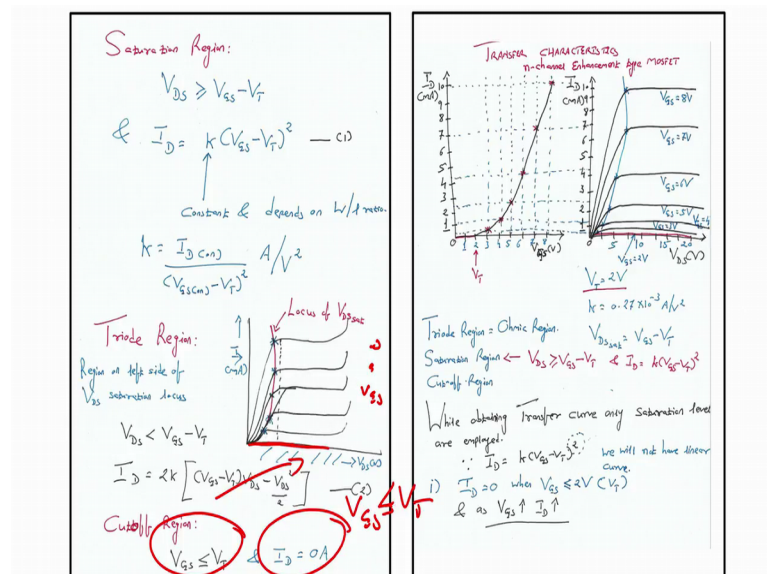
So, we go back to the screen what we see is, the saturation region saturation region VDS greater than VGS minus V T I D equals to k times VGS minus V T square k is constant and depends on the w by l ratio. W by l ratio is of channel ratio then and I have k equals to constant k equals to I D on upon VGS on minus V T on V T volt square which is given in ms per volt square.

Now, I want to see triode region triode region right the region on the left side. So, if I if you consider this particular graph, consider this particular graph what you see voltage VDS versus current ID voltage, VDS versus current ID, what we see that it keeps on increasing for different value of VGS right for different value of VGS you can see different current.

Here what we see here what we see is that if you see the pinch off voltage, if the and if you draw line which interconnects a pinch off voltage back to here, everything on the left side of the VDS saturation is your triode region is your triode region ok.

And VDS is less than VGS minus V T. So, we can write ID equals to 2 times k VGS minus V T into VDS minus VDS volts square by 2 right we can write ID equals to 2 times k VGS minus V T into VDS minus VDS square by 2, what if we consider cut off region where is the cut off region where is the cut off region here yes you got it correctly where is it? It is right over here it is in this region.

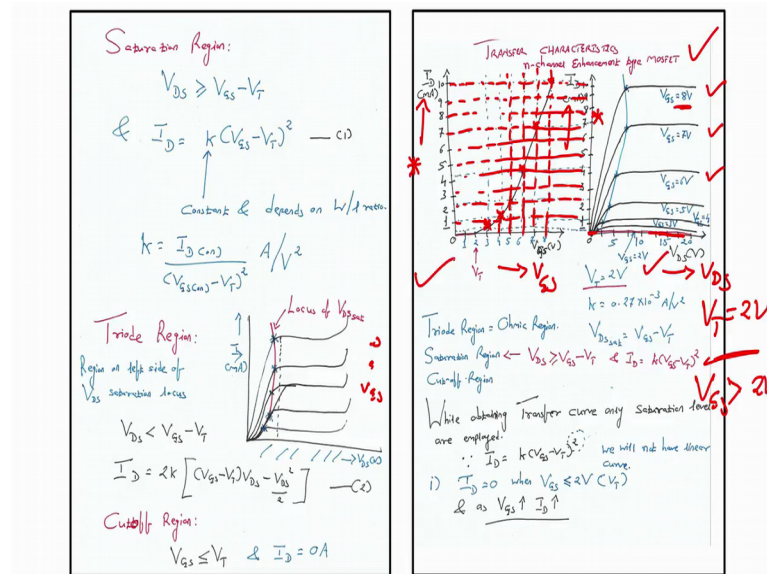
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So, when VGS is extremely less than V T, or less than equal to VT we have current ID equals to 0 you can see here the current is 0 right because my VGS is equals to threshold voltage or is less than threshold voltage ok.

Now, let us see the transfer characteristics of the n channel MOSFET. So, what we see here? You see this one right side see the right side ok.

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What I have I have VDS and I have current here ID current here ID now this graph you already know right for different value of VGS. So, assume that my threshold voltage VT equals to 2 volts, I am assuming VT equals to 2 volts then my gate to source voltage; that means, my VGS should be greater than 2 volts should be greater than 2 volts right. So, what I see here right VGS equals to 2 volts, 3 volts, 4 volts, 5 volts, 6 volts, 7 volt, 8 volt for increasing VGS I can see increasing my in my drain current depending on increasing of my drain to source voltage this is the graph this is the graph right.

If I want to draw the transfer characteristics very easy you have to draw ID versus VGS ID versus VGS that is the plot that you have to draw right now you write down early of VGS from 0 to how much you applied 8 volts you applied. So, 0 1 2 3 4 5 6 7 8 right.

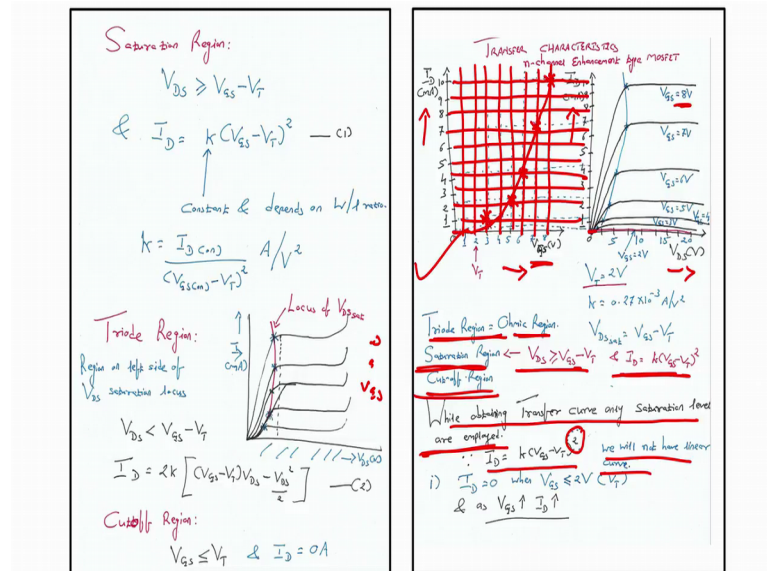
Then what you do then what you do is connect this VGS value this 0 value right where is 0 0 is connected here where is one. So, if you see VGS equals to 4 volts right. So, 4 volts we had to 4 volts is here right, where is 5 volts 5 volts is here right where is 6 volts 6 volts is here right. So, if I connect if I connect like this you see either current here right.

I have current here I have current in both the directions in x sorry I have current in both the plots in y direction here and here I have current right. So, I am just joining current line ten with ten 9 with 9 sorry 9 with 9 8 with 8 7 and see 7 then we have 6 we have 5 4 right we have 3 we have 2 and we have one right I have joined the current axis because both y axis are ID this is easy.

Now, what I had to do? I had to just find out the voltage. So, voltage VGS equals to 3 volts for VGS equals to 3 volts right, where is it VGS equals to 3 volts somewhere here for VGS equals to 4 volt somewhere here 6 volts here, 8 volts here, 9 volts here or 7 volts here. So, now, I can I had to just join lines like this see. So, easy if you know ID versus VDS you can find ID versus VGS. If you know ID versus VDS you can easily find transfer characteristics of ID versus VGS right easy very easy right.

So, again if you want to understand quickly what we have done; what we have done here that we have drawn the ID versus VDS plot. Now I am drawing ID versus VGS plot for drawing ID versus VGS plot.

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First thing I will do is correct the current lines in both the plots like this right. This I had done now what I will do I will I will draw line from one volt onward 1 volt, 2 volt, 3 volt 4 volt, 5 volt, 6 volt, 7 volt and 8 volt what is this volts? This is my VGS now this much is easy.

Now, what I had to do I have to see VGS equals to 3 volts right for VGS equals to 3 volts my current is one. So, I will just put a mark here then another one VGS equals to 5 volts my current is about 2. So, I will mark it here, which is equals to 6 volts my current is about 4 right 4 or yeah its 4. So, will I again put a mark here then my VGS equals to 7 volts my current is about 7 milliamperere. So, I am marking about here, when my VGS is 8 volts my current is about 10 milliamperere. So, I am marking again here, now if I join

this all the marks if I join all the marks like this, I have my characteristics I have my transfer characteristics easy very easy right very easy.

Now, in triode regions is nothing, but your ohmic region, saturation region you know V_{DS} is greater than $V_{GS} - V_T$ and I_D equals to k times $V_{GS} - V_T$ volts square and then there is cut off region. So, while obtaining transfer account only saturation regions are saturation levels are employed, because I_D equals to k times $V_{GS} - V_T$ volts square. So, we will not have any linear curve, we will not have any linear curve. So, this is your transfer characteristics of the n channel MOSFET.

Now, in the next module we will see what is the depletion type mos transistor. Depletion type mos transistor then we will continue the next class right now what we have seen we have seen that if you are given a n channel MOSFET and enhancement type MOSFET, how the MOSFET will operate how can we understand the different cases, when we apply different drain to source voltage, what about the drain transfer characteristics for the enhancement type MOSFET.

How we can derive this drain transfer characteristics curve, and when we consider different value of V_{DS} when we consider different value of V_{GS} and what are the saturation voltage is what are the cut off voltages what are the what is the triode region and how can we plot the transfer characteristics if you are given the I_D versus V_{DS} plot then we know that I_D versus V_{DS} plot in enhancement type, can be generated by applying different gate to source voltages. So, we can have I_D versus V_{GS} plot and we can connect the current line.

And then we can draw vertical lines for the gate source voltage and then you can see for gate to source voltage in my I_D versus V_{DS} , what is my current according to that I will put the current in my I_D versus V_{GS} plot this is how I derive my transfer characteristics for the enhancement type MOSFET ok.

So, now you have not only seen that how you can fabricate a n channel enhancement type MOSFET or n channel MOSFET you also know you also know when I says when I talk about fabrication, it is not actual fabrication not experimental way, but at least you are seen on theory that how you can design the process flow for fabricating a MOSFET. And then we moved onto the to this particular lecture, where now you have seen how the enhancement type MOSFET would behave and what are the transfer characteristics.

Next time a next lecture what we are going to see, we are going to see the depletion type n mos transistor and again we will see the construction to the drain characteristics.

So, this is not and this will not be next lecture it will be part of the same lecture, but a next module. So, till then you just look at the things that I have taught you, and I will see you in the next module take care, bye.